DART Device
Advanced E3/DS3 Receiver/Transmitter
TXC-02030

DATA SHEET

FEATURES

- Single LIU for E3 and DS3
- Meets 'cross-connect frame' mask requirements
- Adaptive equalization for 0 - 900 ft of cable for DS3, 0-1300 ft for E3
- Input dynamic range of 30 dB (35 mVp - 1.1Vp)
- Meets E3/DS3 jitter requirement standards
- Optional HDB3 or B3ZS line encoding/decoding
- Line and terminal side E3 or DS3 AIS insertion
- Full loopback capabilities
- Coding violation and excessive zeros monitors
- Loss of signal detection (per T1/M1 Spec)
- On-device transmit line buffer/filter for DS3; E3 square-wave output
- Receive and transmit power-down modes
- Dejitter PLL/dejitter buffer using external VCXO
- Meets all relevant ANSI and ITU-T standards
- Single +5 volt, ±5% power supply
- 80-pin low profile plastic quad flat package

DESCRIPTION

The Dual-market Advanced E3/DS3 Receiver/Transmitter (DART) device performs the receive and transmit line interface functions required for transmission of E3 (34.368 Mbit/s) or DS3 (44.736 Mbit/s) signals across a coaxial interface.

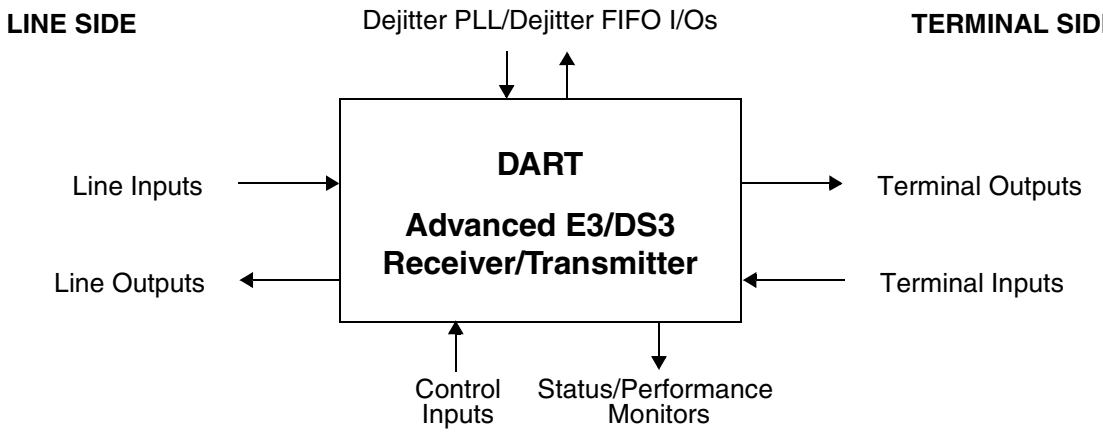
The DART operates from a single +5 volt supply with a minimum number of external components. Performance monitoring, loopbacks, E3/DS3 AIS generation, dejitter FIFO, dejitter PLL, PRBS diagnostic circuits and HDB3/B3ZS encoding/decoding functions are included.

A single-device solution for interfacing E3 or DS3 signals to DSX cross-connect frames, the DART meets all applicable ANSI, BellCore and ITU-T interconnection specifications for a wide range of system applications.

Specifications include, but are not limited to ANSI T1.102-1993, ANSI T1.404-1994, GR-499-CORE, ITU-T G.703, G.751, G.755, G.823, and ETSI TBR24.

APPLICATIONS

- Multiplexers
- E3/DSX and performance monitoring cross-connects
- Fiber optic and microwave radio terminals
- High speed DSU
- Any E3/DS3 transmission application



PRELIMINARY information documents contain information on products in the sampling, pre-production or early production phases of the product life cycle. Characteristic data and other specifications are subject to change. Contact TranSwitch Applications Engineering for current information on this product.

Document Number:
PRELIMINARY TXC-02030-MB
Ed. 2A, April 2000

TranSwitch Corporation • 3 Enterprise Drive • Shelton, Connecticut 06484 • USA
Tel: 203-929-8810 • Fax: 203-926-9453 • www.transwitch.com

TABLE OF CONTENTS

*Please note that TranSwitch provides documentation for all of its products. Customers who are using a TranSwitch Product, or planning to do so, should register with the TranSwitch Marketing Department to receive relevant updated and supplemental documentation as it is issued. They should also contact the Applications Engineering Department to ensure that they are provided with the latest available information about the product, especially before undertaking development of new designs incorporating the product.

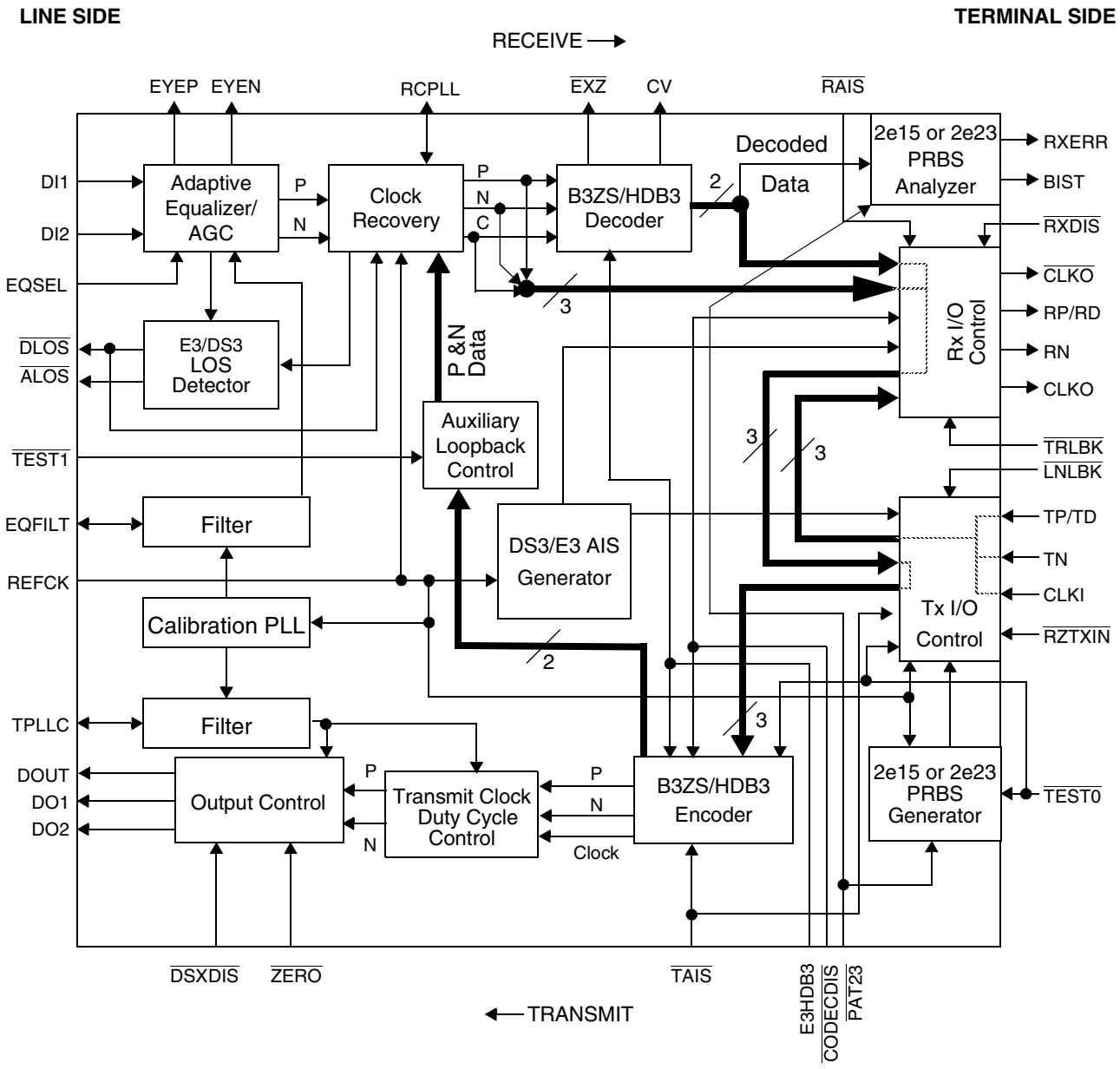
LIST OF TABLES

Table **Page**

LIST OF FIGURES

BLOCK DIAGRAM

A block diagram of the DART device is provided in Figure 1 below.



Note: Thick and dashed lines show parts of loopback paths.

Figure 1. Simplified DART Block Diagram

BLOCK DIAGRAM DESCRIPTION

The DART is designed to send and receive E3 and DS3 signals across coaxial cables. In addition to the basic receiver, clock recovery and transmitter functions the DART has several additional functions which increase its usefulness in designs. The additional functions are encoder/decoder (optional use), PRBS generator, PRBS analyzer, AIS generator, Loss of Signal detection, three different loopbacks, dejitter PLL (in conjunction with an external VCXO) and a 52-bit dejitter buffer. The latter two optional functions are especially useful for repeaters or when performing loop timing.

Due to the complexity of the DART, Figure 1 shows a simplified block diagram which does not include the dejitter PLL/dejitter buffer paths. The figure shows the device operation when the dejitter circuits are not being used.

Figure 2 shows the receive section of the DART, which includes the terminal side dejitter circuits. The dejitter PLL can be used independent of the dejitter buffer when in the receive path. Received data can be either encoded NRZ or unencoded PN rail data. The PRBS analyzer output is valid in all modes as are the CV and $\overline{EXZ}$ signals.

Figure 3 shows the transmit section of the DART, which includes the dejitter circuits. Transmit data can be either unencoded NRZ or encoded PN rail data. The dejitter PLL cannot be used independent of the dejitter buffer when in the transmit path.

Comparing Figures 2 and 3 we see that the dejitter buffer can be used in either the receive or transmit direction with either NRZ or PN data.

In the receive direction the FIFO will contain the decoded-one-bit NRZ data and any code violations (CVs) that occur for $\overline{CODECDIS}$ high. The CV should be aligned with the data bit that generated the coding violation. When $\overline{CODECDIS}$ is low the FIFO contains the encoded PN data from the receiver.

The dejitter PLL can be used in the receiver path without using the dejitter FIFO. The FIFO is gated off in this mode. The dejittered clock will be available at the VCXO output. The receive terminal side outputs will be the normal, jittered outputs that are outputs when the dejitter circuits are not used.

In the transmit direction the FIFO will contain both TP and TN data. In the NRZ mode the TN input must be tied low as the FIFO always accepts TP and TN data when the DART is in the transmit dejitter mode.

Figures 4 through 9 illustrate the various data paths for the four different dejitter modes. Tables 1 and 2 show the control pin settings for the various modes of operation.

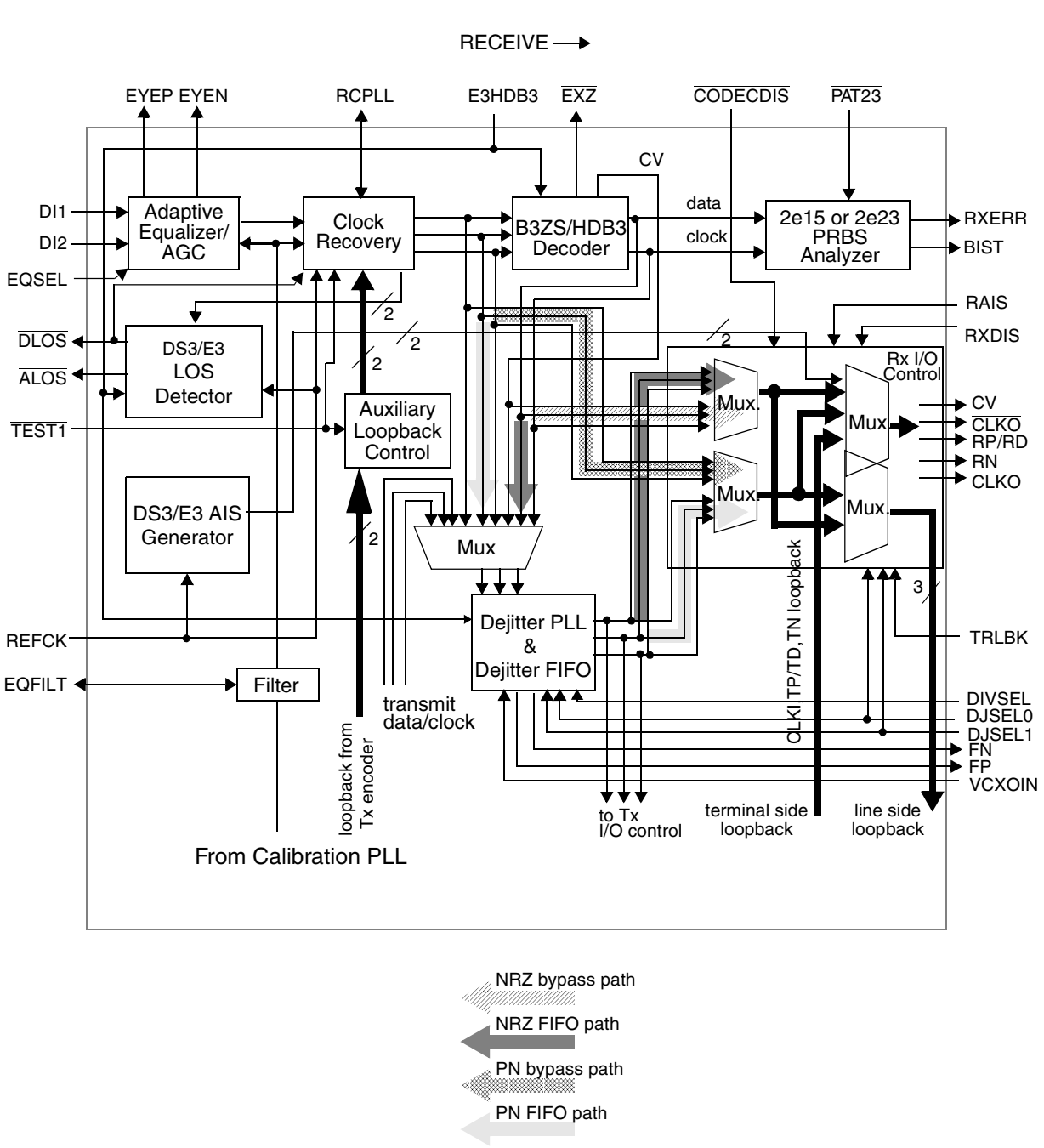


Figure 2. Block Diagram of DART Receive Section

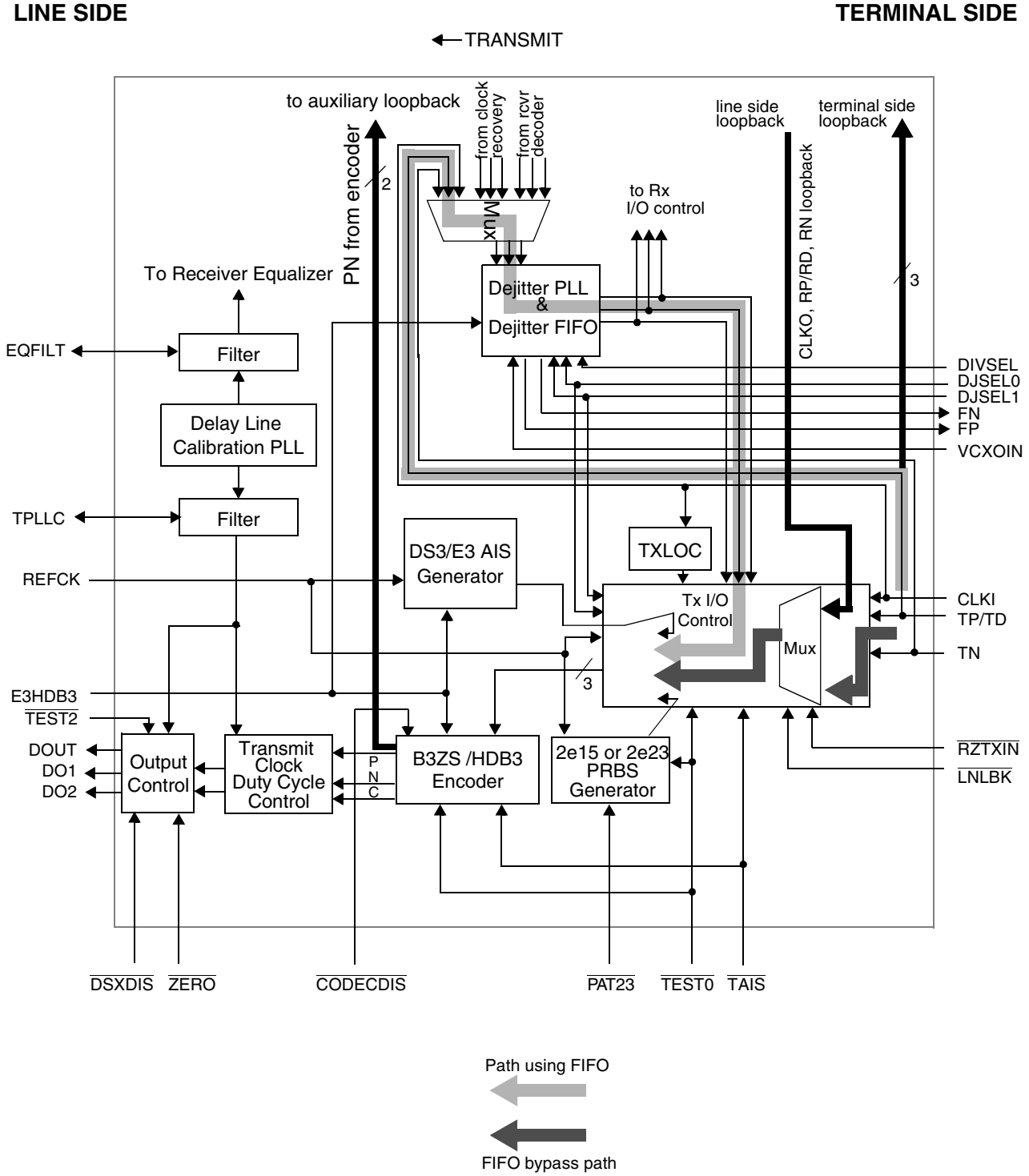


Figure 3. Block Diagram of DART Transmit Section

RECEIVER FUNCTIONS

Adaptive Equalizer/AGC

The Adaptive Equalizer/AGC block in the DART receiver is used to recover CMOS level PN rail data from the bipolar B3ZS (or HDB3) encoded input pulses. The AGC in the DART has a dynamic range of 30 dB (35 mV to 1.1 V). Adaptive equalization is included to restore the integrity of the signal after it has been attenuated by the frequency-dependent loss of up to 900 feet of coaxial cable (1300 feet for E3). The buffered, equalized and AGC'd differential receiver signals are provided as outputs on the EYEP and EYEN pins. Internally, this signal is sliced at approximately fifty percent of the peak voltage to generate CMOS-level P and N data.

Differential inputs DI1 and DI2 are provided to allow optimum performance of the device in noisy environments. Alternatively, single-ended operation can be used in less critical environments or where the use of a transformer is not desired (the input signal can be AC-coupled via a capacitor). When the differential mode is used, the peak AC voltage measured between DI1 and DI2 is a maximum magnitude of 1.1 volts. For single-ended operation, the voltage measured at DI1 (DI2) relative to the DC bias voltage at DI2 (DI1) is a maximum of ±1.1 peak volts. Since the DART has a sensitive receiver, the 4 dB attenuator shown in Figures 31 and 35 must be used. For input levels larger than 1.1 V peak, a step-down transformer or resistive attenuation should be used (see Figure 35 for suggested attenuator topology - the circuit may be modified to give the desired attenuation). The EQSEL pin should be held low to select an amplitude-controlled equalizer.

Clock Recovery

The PLL-based Clock Recovery block is used to recover a CMOS level clock from the equalized and sliced input pulses. The filters are internal. When $\overline{\text{DLOS}}$ is high and $\overline{\text{TEST1}}$ is high (data is present), CLKO is the clock recovered from the data. When $\overline{\text{DLOS}}$ is low and $\overline{\text{TEST1}}$ is high, CLKO is equal to the reference clock (REFCK). When $\overline{\text{TEST1}}$ is low or $\overline{\text{TRLBK}}$ is low, CLKO is equal to the transmit input clock CLKI.

B3ZS/HDB3 Decoder

The B3ZS/HDB3 Decoder block decodes the B3ZS (or HDB3) encoded line signal and detects coding errors and excessive zeros in the incoming data stream. An active-high pulse is generated on the CV output whenever the input signal violates the B3ZS (or HDB3) encoding sequence for bipolar violations or contains three (four) or more consecutive zeros. An active-low pulse is generated on the $\overline{\text{EXZ}}$ output when a string of three (four) or more consecutive zeros is detected and it remains low until a one is detected. When in NRZ mode, the CV signal is timed to occur at the terminal-side receiver output at the same time as the bit violating the coding. The CV is approximately 9 cycles after the errored data in the eye pattern monitor. The $\overline{\text{CODECDIS}}$ control input is used to bypass the decoder NRZ outputs with PN data at the receiver terminal side outputs; the decoder is always operating so CV and $\overline{\text{EXZ}}$ are always valid. E3HDB3 high will select HDB3 encoding and decoding.

Rx I/O Control

The Rx I/O Control block multiplexes the appropriate signals to the receiver terminal side outputs. The output NRZ data formats include:

1. B3ZS (or HDB3) decoded output recovered from the line (RP/RD contains recovered data; RN is held low). This mode is referred to as NRZ mode. $\overline{\text{CODECDIS}}$ high enables the codec.
2. Encoded outputs from the Clock Recovery block (RP/RD contains positive data; RN contains negative data). This mode allows an external device to perform the encoding/decoding functions. $\overline{\text{CODECDIS}}$ low enables this mode. This is referred to as PN rail mode.
3. Loopback signals from the transmitter terminal side inputs are looped through the digital logic when $\overline{\text{TRLBK}}$ is low. The receiver and clock recovery are bypassed. Data can be either NRZ or PN data.
4. AIS DS3-framed format signals when $\overline{\text{RAIS}}$ is low and E3HDB3 is low.
5. AIS alternating ones (E3 format) when $\overline{\text{RAIS}}$ is low and E3HDB3 is high.

6. Loopback data from the transmit terminal side inputs are encoded PN data which is looped to the receiver terminal side outputs through the Clock Recovery block, when $\overline{\text{TEST1}}$ is low. The data input into the transmit terminal side inputs can be unencoded NRZ data or encoded PN data.

See the AIS and Loopback Control Signal Arbitration table (Table 6) for further clarification.

Outputs CLKO and $\overline{\text{CLKO}}$ provide true and inverted clocks for all formats.

The $\overline{\text{RXDIS}}$ signal forces the RP/RD and RN outputs to a low state.

LOS Detector

The LOS Detector block generates active low outputs which indicate the absence of the line side input signal(s). The $\overline{\text{DLOS}}$ output goes low when a string of 175 ± 75 consecutive zeros occurs on the line. This output is reset to high when the detected ones density is in the range of 28 to 33% (or > 33%) for 175 ± 75 pulses for B3ZS or 20 to 25% (or > 25%) for 175 ± 75 pulses for HDB3. The $\overline{\text{ALOS}}$ output goes low when the detected ones density is below 28% for 175 ± 75 pulses for B3ZS or below 20% for 175 ± 75 pulses for HDB3. $\overline{\text{ALOS}}$ is reset to high when the ones density is greater than 33% for B3ZS, or greater than 25% for HDB3, for 175 ± 75 pulses. Between 28 and 33% for B3ZS, or between 20 and 25% for HDB3, the $\overline{\text{ALOS}}$ output may toggle between the active and reset states.

The LOS Detector block always uses the receiver outputs which are based upon the receiver inputs DI1 and DI2. When $\overline{\text{TRBLK}}$ is low the Clock Recovery block is still recovering the clock from the receiver inputs. Therefore the $\overline{\text{DLOS}}$ and $\overline{\text{ALOS}}$ signals are still valid. When $\overline{\text{TEST1}}$ is low the Clock Recovery block will recover the clock from the internally looped transmitter inputs. In this state $\overline{\text{DLOS}}$ and $\overline{\text{ALOS}}$ will be active but may no longer meet the limits given above.

The $\overline{\text{DLOS}}$ signal meets ITU-T Rec. G.775 for the loss of signal indication. The $\overline{\text{ALOS}}$ signal is a stricter indication of line degradation and there is no standard related to this function. $\overline{\text{DLOS}}$ requires a large number of consecutive zeros to give a loss of signal indication. An occasional “1” data bit can prevent the activation of $\overline{\text{DLOS}}$ even though the data is highly errored. In contrast, the $\overline{\text{ALOS}}$ signal monitors the data to ensure the data stream has the proper number of ones (ones density), as required by the B3ZS (or HDB3) coding algorithm. For this reason, $\overline{\text{ALOS}}$ is a stricter indicator of the status of a transmission impairment. The $\overline{\text{ALOS}}$ and $\overline{\text{DLOS}}$ outputs may not be reliable if the input cable at the receive interface is left disconnected. This effect is layout dependent. If the data cycles on and off at a slow rate $\overline{\text{ALOS}}$ and $\overline{\text{DLOS}}$ may become stuck off (high) and the receiver output clock (CLKO) will also be running at a slow rate.

TRANSMITTER FUNCTIONS

Tx I/O Control

The Tx I/O Control block multiplexes the appropriate signals for use by the transmitter. The selectable formats include:

1. Unencoded Non-Return-to-Zero (NRZ) input data (TP/TD contains unencoded data, TN must be grounded). This is referred to as NRZ mode which is selected when $\overline{\text{CODECDIS}}$ is high.
2. B3ZS (or HDB3) encoded PN input data (TP/TD contains positive data, TN contains negative data). $\overline{\text{CODECDIS}}$ pin held low enables this mode (PN rail mode).
3. B3ZS (valid for DS3 only) encoded Return-to-Zero (RZ) input data (TP/TD contains positive data, TN contains negative data). The transmit encoder and transmit clock duty cycle control circuits are bypassed. The RZ pulses must contain input pulses that have the correct pulse width. This mode is enabled when $\overline{\text{RZTXIN}}$ is held low. CLKI should be tied low to gate the transmit logic off and $\overline{\text{CODECDIS}}$ should be tied low.
4. Looped-back clock and data from the receiver (to the internal transmitter input) when $\overline{\text{LNLBK}}$ is low. Looped data can be either NRZ or PN data. In the NRZ mode the data will first be decoded and then re-encoded. Code violations in the data stream will be lost in the decoding/encoding process. In contrast, the PN mode passes the received data to the transmitter unaltered.

5. AIS DS3-framed format signal when $\overline{TAIS}$ is low and E3HDB3 is low. The encoder is automatically enabled when $\overline{TAIS}$ is low.
6. AIS alternating ones (E3 format) signal when $\overline{TAIS}$ is low and E3HDB3 is high.
7. B3ZS (or HDB3) unencoded, unframed $2^{15}/2^{23}$-1 PRBS generator output when $\overline{TEST0}$ is low with the exception of $\overline{LNLBK}$ and RZ format. The state of the $\overline{CODECDIS}$ pin does not affect the encoding of the generator output. When $\overline{TEST0}$ is set low, the encoder is enabled to ensure that correctly coded data is always transmitted.

The AIS and Loopback Control Arbitration table (Table 6) provides further clarification.

The CLKI pin is the input clock for the formats described in 1, 2 and 7 above. When $\overline{RZTXIN}$ is low, the CLKI signal is ignored and should be tied low. When $\overline{LNLBK}$ is active, CLKI is also ignored but does not have to be tied low. For transmitting AIS, the reference clock REFCK is used exclusively. The duty cycle requirement for CLKI and REFCK is (50 ± 10)% with a frequency accuracy of the nominal bit rate ± 20 ppm. The frequency accuracy of REFCK can be relaxed to the nominal bit rate ± 100 ppm if the transmit AIS function is not used.

Transmit Clock Duty Cycle Control Circuit

The Transmit Clock Duty Cycle Control circuit relaxes the duty cycle requirement for both REFCK (when using the transmit AIS function) and CLKI. Instead of the usual ± 5% duty cycle tolerance, the duty cycle tolerance of the DART clocks is ± 10%. This allows using a less expensive oscillator and eases the board design.

B3ZS/HDB3 Encoder

The B3ZS/HDB3 Encoder block encodes the input NRZ mode data so as to be compliant with ANSI Specification T1.102A (ITU-T Rec. G.703 for E3). Figure 25 gives examples of B3ZS encoding (HDB3 is similar). The $\overline{CODECDIS}$ control pin can be used to disable the encoding function of this block so that the PN rail data is passed through unchanged. $\overline{CODECDIS}$ must be low when $\overline{RZTXIN}$ is low.

When $\overline{TAIS}$ is low and $\overline{TEST0}$ is high the encoder is disabled and the AIS signal is passed to the output.

When $\overline{TEST0}$ is low the encoder is enabled and the output of the PRBS data generator is encoded and passed to the output.

The AIS and Loopback Control Signal Arbitration table (Table 6) provides further clarification.

Transmitter Output Control Block

DS3 Shaped Output

The Output Control block contains the pulse shaping circuitry required to transform the B3ZS encoded data into pulses that meet the mask templates and power requirements for DS3 line rates. An internal line driver is included which enables the DART to drive this signal directly from DOUT into the 75 ohm load of the output cable. The $\overline{ZERO}$ pin should be held low for all cable lengths.

When the $\overline{DSXDIS}$ pin is high the DOUT transmitter output is enabled. DOUT is a single-ended output which meets the DS3 mask template. An internal transversal filter is used to create this output.

E3 Square-Wave Output

Transmit outputs DO1 and DO2 are rectangular CMOS level pulses, generated in conjunction with external passive components, that produce level-translated E3 transmit mask-compliant versions of the input digital signal(s). The AVDDTX pins set the amplitude of these waveforms. The amplitudes will have little variation with V_{DD} if the AVDDTX supply voltage used is produced by a three-terminal voltage regulator. The square wave outputs need external load resistors as shown in Figure 31, “External Components, Pin Connections and Power/Ground”. An external transformer is required to translate the DO1 and DO2 signals to the appropriate +/- polarity (bipolar) waveform. When using the DO1 and DO2 outputs, power dissipation is minimal in the transmitter when no data is being transmitted.

Waveform Control Pins

When $\overline{\text{DSXDIS}}$ is high, the DOUT output is enabled. When $\overline{\text{DSXDIS}}$ is low, the DO1/DO2 outputs are enabled. Figure 26 shows idealized transmitter waveforms for both output modes.

TRANSMITTER CALIBRATION PLL

The calibration PLL calibrates an internal delay line by locking to the REFCK signal. The resulting control voltages are filtered and used in delay lines in other parts of the device.

An external capacitor connected from TPLLC to the proper analog ground is required for filtering the internal calibration PLL control voltages. The filtered voltages are used to calibrate the transmitter transversal filter circuit (see Figure 31 and Note 7). The transmitted pulse width can be changed by adding an external resistor from TPLLC to either AVDDTX (which narrows the pulse) or AGNDTX (which widens the pulse).

LOOPBACKS AND AIS INSERTION

The loopback control signals enable input signals of the DART to be looped back on both the line side and terminal side. The AIS and Loopback Control Signal Arbitration table (Table 6) illustrates the various control signals and related DART outputs.

Internal Digital Transmit Terminal Side Loopback

When $\overline{\text{TRLBK}}$ (terminal loopback) is low, the TP/TD, TN and CLKI inputs are directly looped back to the RP/RD, RN and CLKO pins via the Rx I/O Control Block (all-digital signal path). The normal transmit path is active in this state. The state of $\overline{\text{CODECDIS}}$ does not affect the terminal loopback path.

Internal Analog Receive Line Side Loopback

When $\overline{\text{LNLBK}}$ is low and $\overline{\text{CODECDIS}}$ is high, the DI1/DI2 signals are looped back to the DOUT or DO1/DO2 outputs via the Adaptive Equalizer/AGC, Clock Recovery, B3ZS/HDB3 Decoder, Rx I/O Control, Tx I/O Control, B3ZS/HDB3 Encoder and Output Control blocks. Since the data will be processed through the decoder then re-encoded in this mode, any receiver code violations will not be propagated to the transmitter output.

When $\overline{\text{LNLBK}}$ is low and $\overline{\text{CODECDIS}}$ is low, the DI1/DI2 signals are looped back to the DOUT or DO1/DO2 outputs via the Adaptive Equalizer/AGC, Clock Recovery, Rx I/O Control, Tx I/O Control and Output Control blocks. The decoder and encoder data paths are bypassed in this mode, but the CV and $\overline{\text{EXZ}}$ signals are valid and the normal receiver path is active. Received data will propagate to the transmitter output with no alteration.

The above two loopbacks may be operated independently or simultaneously. It should be noted that when $\overline{\text{TRLBK}}$ is active, the CV, $\overline{\text{DLOS}}$, $\overline{\text{EXZ}}$ and $\overline{\text{ALOS}}$ output signals will still respond to the line input data signals applied at pins DI1 and DI2 and will be valid signals. As stated previously, the normal receive path is active during $\overline{\text{LNLBK}}$.

Internal Analog Transmit Terminal Side Loopback

For the DART device, when $\overline{\text{TEST1}}$ is low and $\overline{\text{CODECDIS}}$ is high, the transmit terminal input data will loop back through the Encoder, Auxiliary Loopback Control, Clock Recovery, Decoder and Rx I/O Control blocks as shown in Figures 4 through 11. When $\overline{\text{TEST1}}$ is low and $\overline{\text{CODECDIS}}$ is low, the transmit terminal input data will loop back through the auxiliary loopback control, clock recovery and Rx I/O control blocks, as shown in Figures 4 through 11. When $\overline{\text{TAIS}}$ is active low at the same time as $\overline{\text{TEST1}}$ is active low, AIS will loop through this path and be provided at the output on the receiver terminal side.

DS3/E3 AIS Generator

The DS3/E3 AIS Generator block generates a DS3 (E3) alarm indication signal (AIS) compliant with Bellcore Specification TR-TSY-000191 (ITU-T Rec. G.775) on the line or terminal sides of the device. The AIS outputs are selected with $\overline{\text{TAIS}}$ or $\overline{\text{RAIS}}$. This block generates DS3 or E3 format AIS only. AIS will override the loop-

back commands. The reference clock REFCK is used to generate both AIS (framed for DS3) and PRBS transmitted data. The required duty cycle for REFCK is (50 ± 10)% and the frequency accuracy is the nominal bit rate ± 20 ppm (as required by the standards). The transmit clock duty cycle control circuit will generate a transmit clock from REFCK that has the proper duty cycle.

TESTABILITY

$2^{15}/2^{23}$-1 PRBS Generator

The $2^{15}/2^{23}$-1 PRBS (Pseudo-Random Binary Sequence) Generator and PRBS Analyzer blocks provide diagnostic capability. When the $\overline{\text{TEST0}}$ pin is low, the output of the PRBS generator is driven through the Tx I/O Control, B3ZS Encoder and Output Control blocks to either DOUT when $\overline{\text{DSXDIS}}$ is high, or DO1/DO2 when $\overline{\text{DSXDIS}}$ is low. The encoder is always enabled when $\overline{\text{TEST0}}$ is low, regardless of the state of the $\overline{\text{CODECDIS}}$ pin. The analyzer works in either NRZ mode or PN mode.

$2^{15}/2^{23}$-1 PRBS Analyzer

The PRBS Analyzer monitors the output of the B3ZS/HDB3 decoder block. If the output signal conforms to the correct $2^{15}/2^{23}$-1 pattern the BIST output will go high. The PRBS Analyzer always functions, regardless of the state of the $\overline{\text{TEST0}}$ pin. Whenever a valid $2^{15}/2^{23}$-1 pattern (this pattern can contain a significant number of errors and still be valid) appears at the receiver outputs the BIST pin will go high. The BIST signal operates as a PRBS synchronization indicator for the incoming received data. The RXERR output of the device goes high whenever a received bit is in error for the selected PRBS pattern and the BIST pin is high.

The analyzer runs regardless of the state of the $\overline{\text{CODECDIS}}$ pin, since the PRBS analyzer is supplied with decoded data by the Decoder at all times. The Generator/Analyzer combination can be used in conjunction with both external and internal line-side loopbacks for diagnostic purposes. The combination of both $\overline{\text{TEST0}}$ and $\overline{\text{TEST1}}$ pins being low sends signals through all of the data path blocks in the device. This is particularly useful for manufacturing test.

Setting the $\overline{\text{PAT23}}$ pin low selects the 2^{23}-1 pattern operation. Setting the $\overline{\text{PAT23}}$ pin high selects the 2^{15}-1 pattern operation.

INPUT REFERENCE CLOCK

A TTL level input clock at the E3 or DS3 rate must be applied to the REFCK input for the DART device to operate. This will typically be supplied by a local oscillator on the board. The tolerance required is ± 100 ppm for operation when the DS3 AIS generator is not used. To generate a valid AIS transmit signal a frequency tolerance of ± 20 ppm is required. The required duty cycle is (50 ± 10)%. REFCK can be the same signal as CLKI, if CLKI is driven from a local card oscillator. If loop timing is being performed REFCK can be the same signal as CLKI, if a provision is made to multiplex between the local card oscillator and the dejittered recovered clock; the logical “or” of $\overline{\text{ALOS}}$ and $\overline{\text{DLOS}}$ should be part of the mux control logic. When these signals are active, it may indicate the recovered clock is inaccurate and the local card oscillator should be used.

DEJITTER FIFO/DEJITTER PLL OPERATION

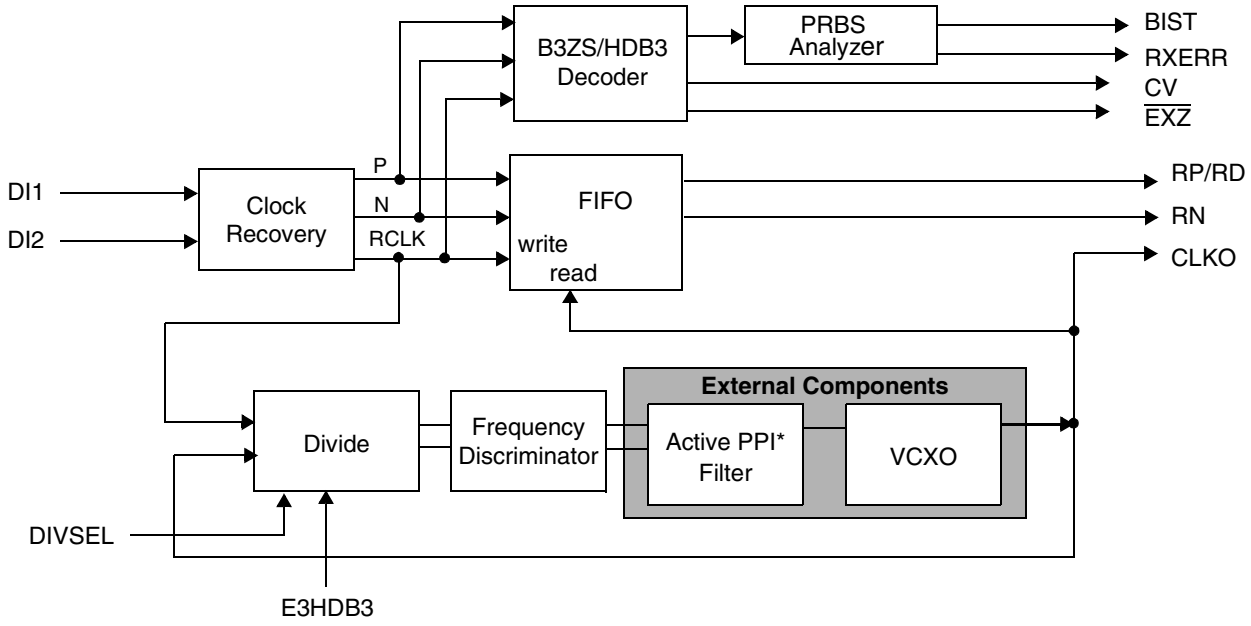
The data paths and operation of the Dejitter PLL and Dejitter FIFO portions of the DART device are shown in Figures 2 through 11. Figures 2 and 3 show the block diagrams of the DART receive and transmit sections, respectively, with dejitter circuits included. Figures 4 through 11 show the simplified Dejitter PLL/FIFO data paths for each operating mode of the DART device. Note that use of the $\overline{\text{LNLBK}}$ pin is invalid when in the dejitter mode and PN mode (see Figure 4). The VCXO interface diagrams in Figures 33 and 34 show the external component connections for the DART dejitter PLL. TranSwitch Application Note AN-525, “Dejitter Circuit for Data Transmission Using the Recovered Clock”, Document No. TXC-02050-AN2 can be used as an aid in the design of a recovered clock dejitter only circuit, which is shown in Figures 6 and 7.

There are four distinct modes of operation of the Dejitter PLL/Dejitter Buffer. The first mode involves dejittering both the recovered clock and receive data. In this mode either P and N data is dejittered or NRZ data (i.e. RP/RD) and associated CVs are dejittered. Figures 4 and 5 show these paths. The second mode involves dejittering the recovered clock. In this mode the dejitter FIFO is gated off. The dejitter PLL uses the recovered clock to allow recovered clock dejittering. This is shown in Figures 6 and 7. The third mode involves dejittering both the transmit clock and the transmit data. Both TP/TD and TN are fed into the FIFO regardless of the state of $\overline{\text{CODECDIS}}$. TN should be tied low when the NRZ mode is being used. Figures 8 and 9 show the data paths for CLKI, TP/TD and TN dejittering. The dejitter FIFO and dejitter PLL are bypassed in transmit dejitter mode if $\overline{\text{LNLBK}}$ is active (low). The looped recovered clock and data signals will not be dejittered. The fourth mode bypasses both dejitter circuits. Figures 10 and 11 show the data paths when the dejitter circuits are not used.

Figures 33 and 34 show a simplified block diagram of the dejitter circuits in the DART and the associated external circuits. It can be seen from these figures that the phase detector is a simple exclusive-or gate. The logic block preceding the exclusive-or gate contains logic that performs frequency acquisition to ensure that the dejitter PLL will lock to the correct clock frequency under all frequency offset conditions.

The active filter is necessary when using the FIFO because any static phase offset in the PLL loop will cause the FIFO fill level to be offset from the nominal half-full level. For this reason the external operational amplifier used should have a low input-offset voltage. The active filter can also be used when dejittering only the recovered clock. However, since static phase offsets are not important in this mode, the passive external RC filter can be used. When operating in transmit dejitter mode, the transmission will stop if the VCXO stops (the VCXO output is being used as the transmit clock in this mode).

Tables 1 and 2 that follow Figure 11 show the functions of the dejitter control pins.



*Note: PPI is an abbreviation for Proportional Plus Integral

Figure 4. Receive Side Dejitter FIFO Using PN Data (DJSEL0=0, DJSEL1=0)

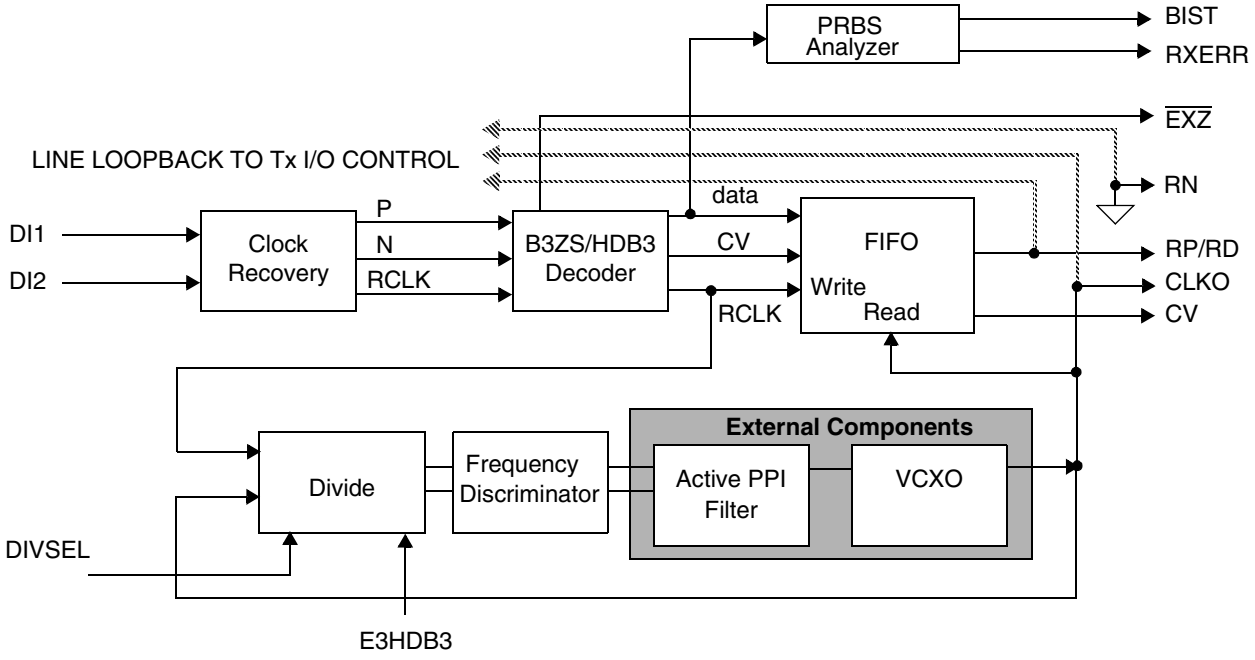


Figure 5. Receive Side Dejitter FIFO Using NRZ Output (DJSEL0=0, DJSEL1=0)

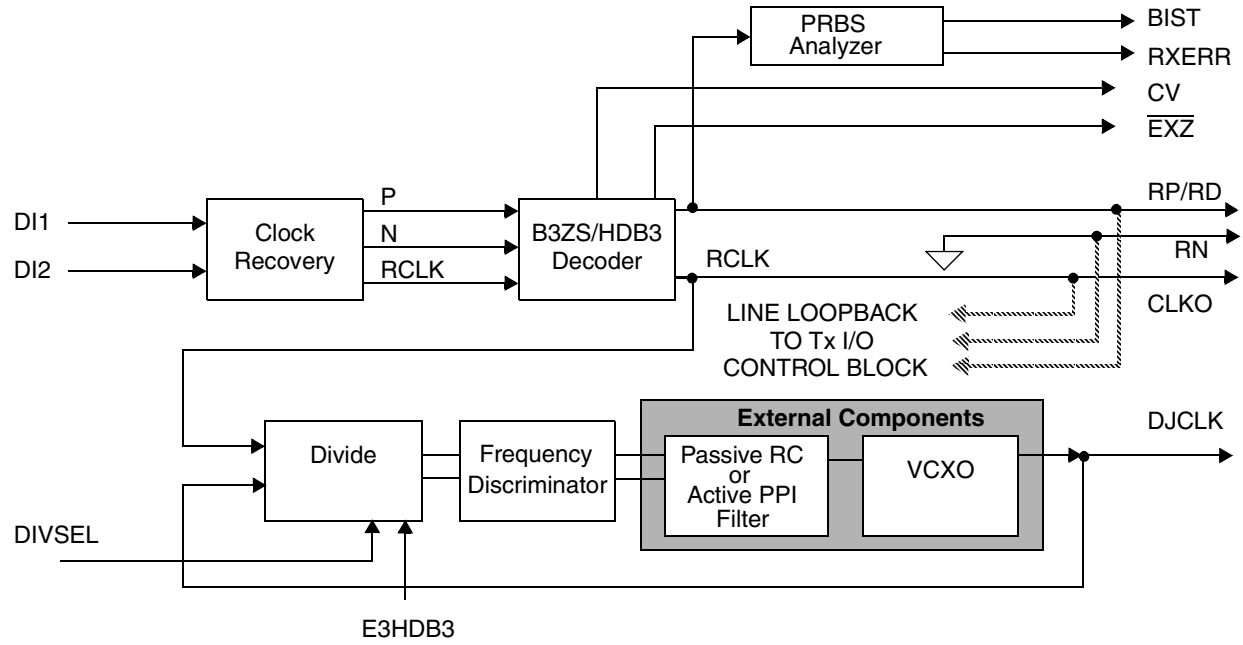


Figure 6. Receive Side Clock Dejitter Only; NRZ Mode (DJSEL0=0, DJSEL1=1)

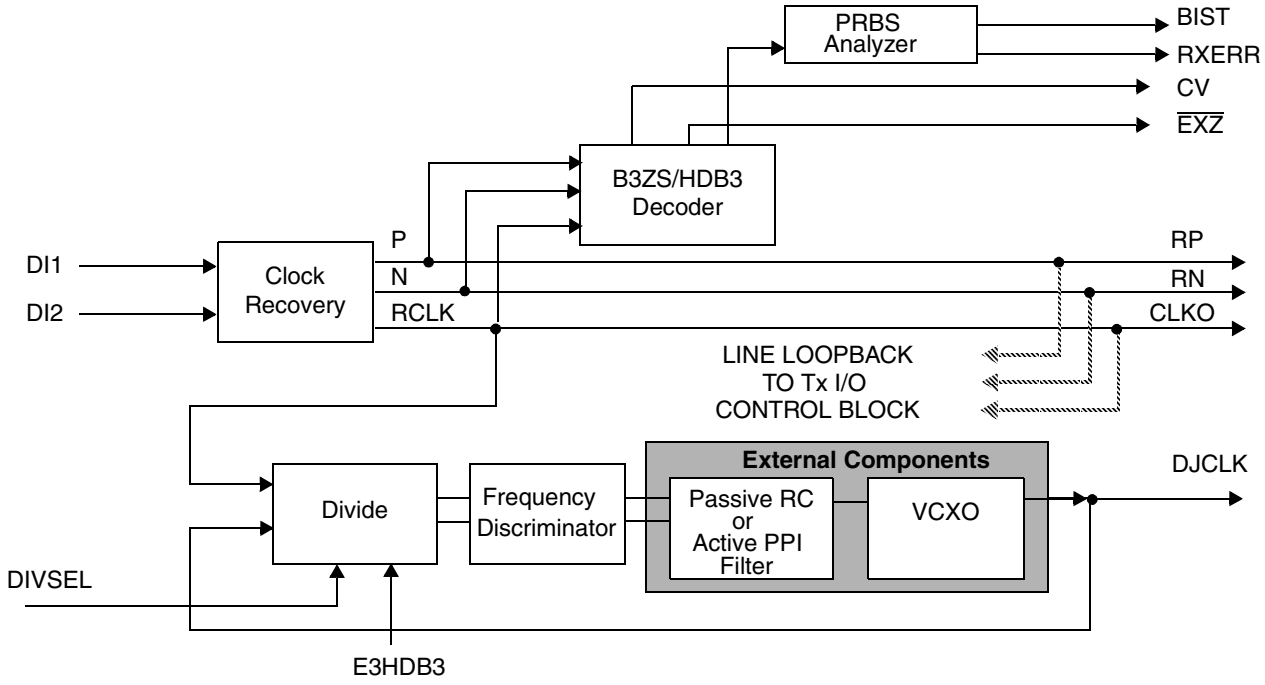


Figure 7. Receive Side Clock Dejitter Only; PN Mode (DJSEL0=0, DJSEL1=1)

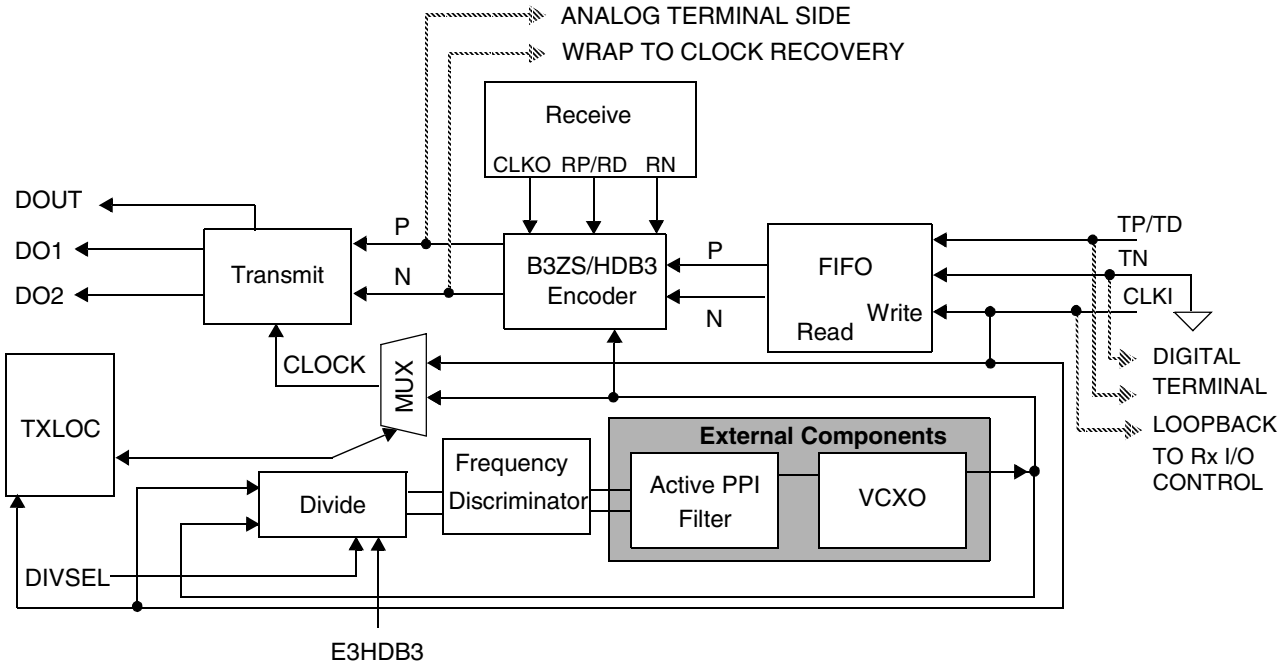


Figure 8. Transmit Side Dejitter FIFO; NRZ Mode (DJSEL0=1, DJSEL1=0)

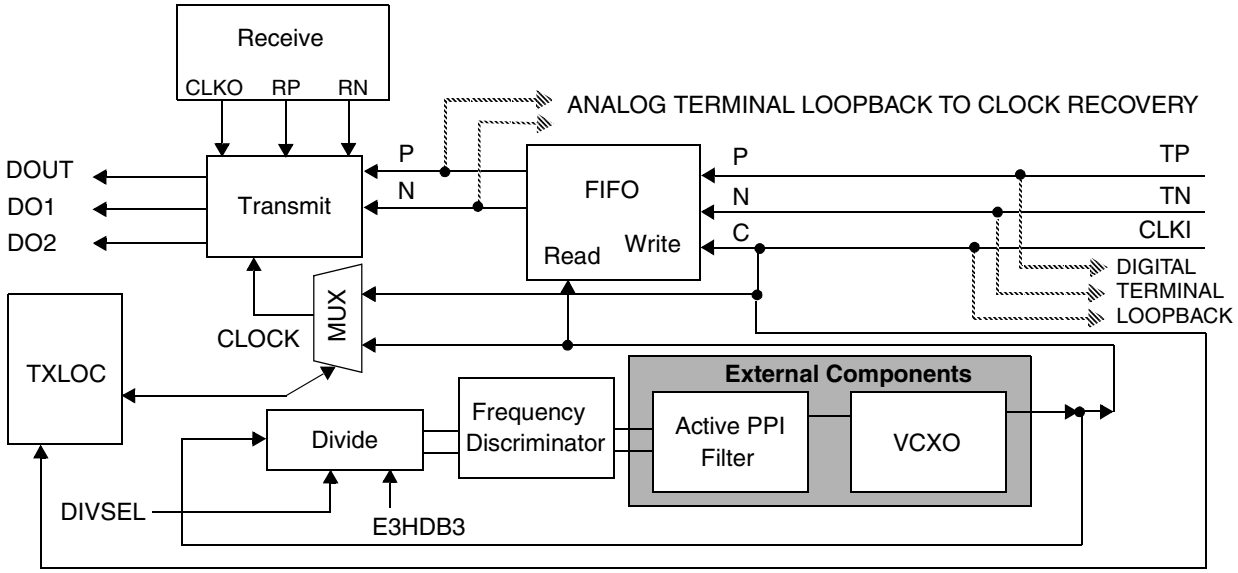


Figure 9. Transmit Side Dejitter FIFO; PN Mode (DJSEL0=1, DJSEL1=0)

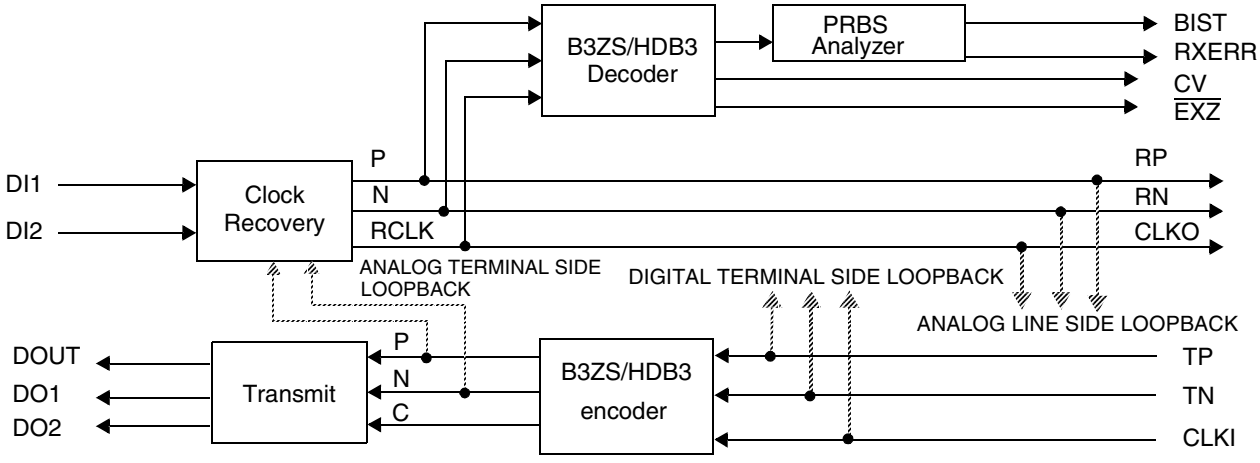


Figure 10. Normal Operation; PN Mode (DJSEL0=1, DJSEL1=1)

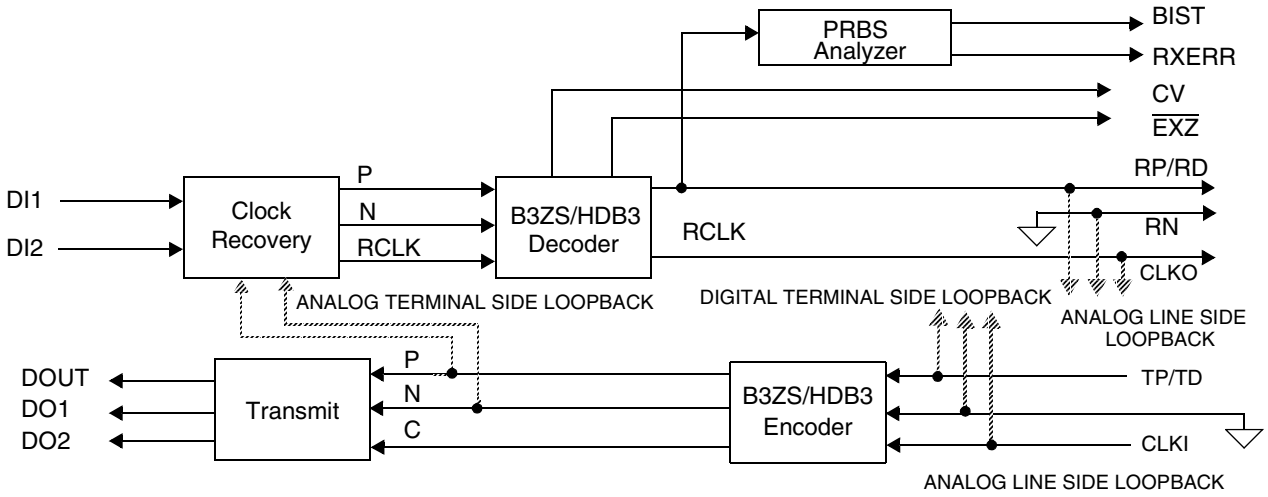


Figure 11. Normal Operation; NRZ Mode (DJSEL0=1, DJSEL1=1)

Table 1. Dejitter Control Signals

$\overline{\text{CODECDIS}}$	DJSEL0	DJSEL1	Dejitter FIFO Inputs/Outputs	Dejitter PLL Reference Clock Source	Device Outputs
1	0	0	RP and CV	RCLK	Dejittered CLKO, RP and CV
0	0	0	RP and RN	RCLK	Dejittered CLKO, RP and RN
X[1]	0	1	FIFO gated off	RCLK	Normal, jittered outputs[2]
1	1	0	TP and TN[3]	CLKI	Dejittered Transmit Data
0	1	0	TP and TN	CLKI	Dejittered DOUT or DO1and DO2
X[1]	1	1	FIFO gated off[4]	PLL gated off[4]	Normal, jittered outputs

Notes:

1. X = don't care.
2. The normal data paths are enabled. The dejittered recovered clock is the output of the VCXO. CLKO is the normal, jittery recovered clock signal.
3. Tie TN low in NRZ mode.
4. All dejitter circuits are disabled. All dejitter data paths are bypassed.

Table 2. Dejitter PLL Divide Control

E3HDB3	DIVSEL	Dejitter PLL Internal Divide-By
0	0	1024
0	1	2048
1	0	512
1	1	1024

Note: The dividers are located directly before the frequency discriminator in both the reference clock path and the PLL feedback path.

From the table above it is seen that the Divide Factor (N) is controlled by the DIVSEL and E3HDB3 pins. The PLL open gain is inversely proportional to the divide factor; the divide factor is application dependent. The divide factor in combination with the VCXO gain and the external filter frequency response is used to determine the stability, transient response, and bandwidth of the dejitter PLL. The greatest variability of the these three factors is the VCXO gain. Attention should be paid to the VCXO minimum and maximum frequency deviation range which is not often specified by the VXCO manufacturer. A conservative number should be used for the VCXO gain to ensure the design goals are met.

The PLL behavior is described by the following equations:

VCXO gain = Kvx/s = [(Deviation_range * Center Frequency * 2 * pi) / 4] / s.

Phase Detector gain = Kpd = [5, 10]/(2 * pi * N); 10 for differential filter, 5 for single-ended filter.

Active Filter Transfer Function = LF(s) = [1 / (s* R1 * C1) + [R2 / (s * R1 * R2 * C2) + R1]; single-ended version of the differential filter shown in Figure 33. The block diagram of the Dejitter PLL is shown in the Figure 12.

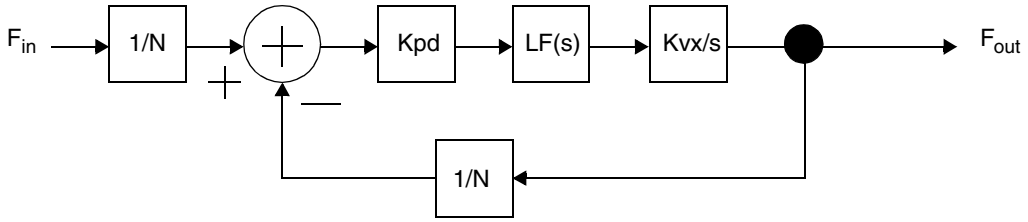


Figure 12. Dejitter PLL Block Diagram

From the block diagram the following equations can be derived.

The Dejitter PLL open loop transfer function = Loop(s) = Kpd * LF(s) * Kvx/s.

The Dejitter PLL closed loop transfer function = PLL(s) = (Loop(s) / (1 + Loop(s))).

For well-behaved operation the open loop frequency response must have less than 135 degrees of phase shift when the loop gain crosses the unity gain line of the Bode response. There are two primary sources of phase shift. The first is the VCXO (1/s) and the second is the external filter (LF(s)). Application note AN-525 goes into greater detail for designing a dejitter PLL using a passive filter. Changes to the design equations of AN-525 when using an active filter are straightforward. There are MATLAB and Mathcad routines to help in designing the Dejitter PLL for a specific application. Contact the TranSwitch applications group for additional information and the analysis tools.

Figure 13 shows the measured results of the DART Dejitter PLL at DS3 using the external filter values shown in Figure 33. The upper curve of the figure shows the jitter on the input signal to the DART; for the receiver the jitter is into DI1/DI2 and for the transmitter the jitter is on TP/TD and CLKI. The upper curve is actually the receiver jitter tolerance curve.

The lower curve shows the measured dejitter PLL output jitter. For the receive side the jitter was measured at the receiver terminal side. For the transmitter the jitter was measured at the transmitter line side.

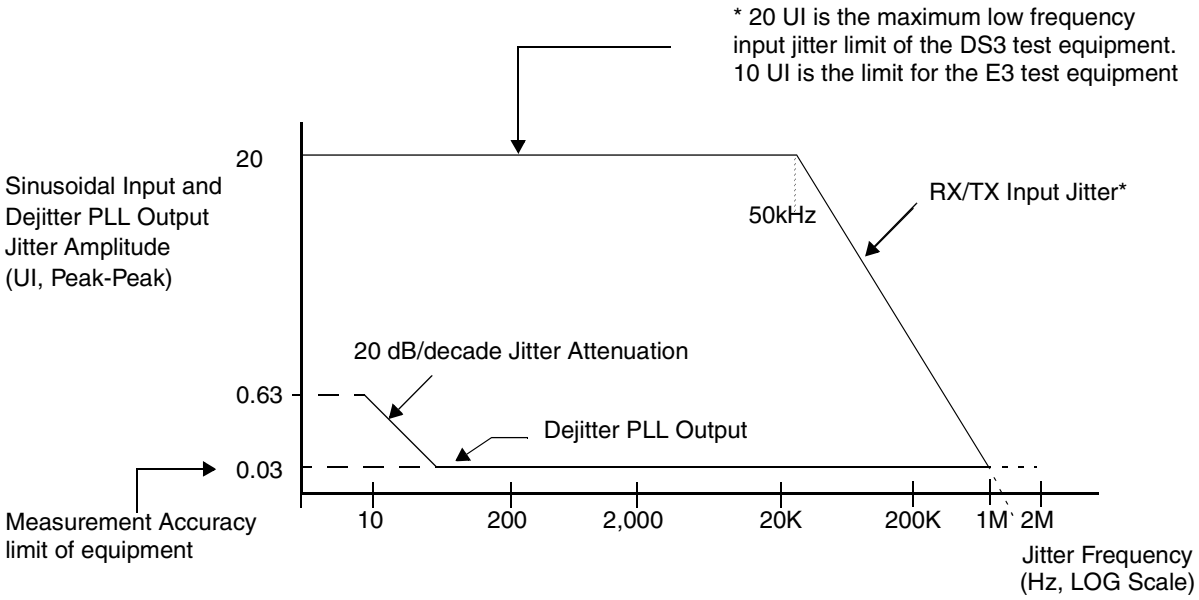
From the figure we see that at the beginning measurement frequency of 10 Hz (lowest measurement frequency of the equipment) the measured output jitter is 0.63 UI for input jitter of 20 UI. The measured output jitter decreases at 20 dB/decade until it reaches a level of 0.03 UI for the receiver; 0.03 UI is the measurement accuracy of the test equipment. The measured output jitter level for the transmitter is 0.04 UI; 0.04 UI is the generated jitter of the transmitter with a jitterless input clock.

The dejitter PLL output jitter measurements were taken at three different frequency offsets. The frequencies

were 44.736 MHz and 44.736 MHz +/- 40 ppm. The supply voltage was varied from 4.7 to 5.3 volts. The measurement temperatures were -40 ^{o}C, 25 ^{o}C, and 85 ^{o}C. The output jitter curve shown represents the worst case measurement for the test conditions.

No failures to phase lock were experienced for any of the tests performed and there were no cycle slips.

It should be noted that the VCXO is the biggest source of variability of the PLL response and particular attention should be paid to its characteristics.



Notes: Unit Interval (UI) = 1/(DS3 System Clock Frequency).
Test conditions: V_{DD}=5V +/- 0.5V, T_A=-40^{o}C, 0^{o}C, 85^{o}C, B3ZS coding, 2^{15}-1 data pattern.
Dejitter Clock Frequency Offset from DS3 Nominal = -40ppm, 0ppm, 40ppm.

Figure 13. Measured Output Jitter of Dejitter PLL at DS3 (E3 results better or equal to)

PIN DIAGRAM

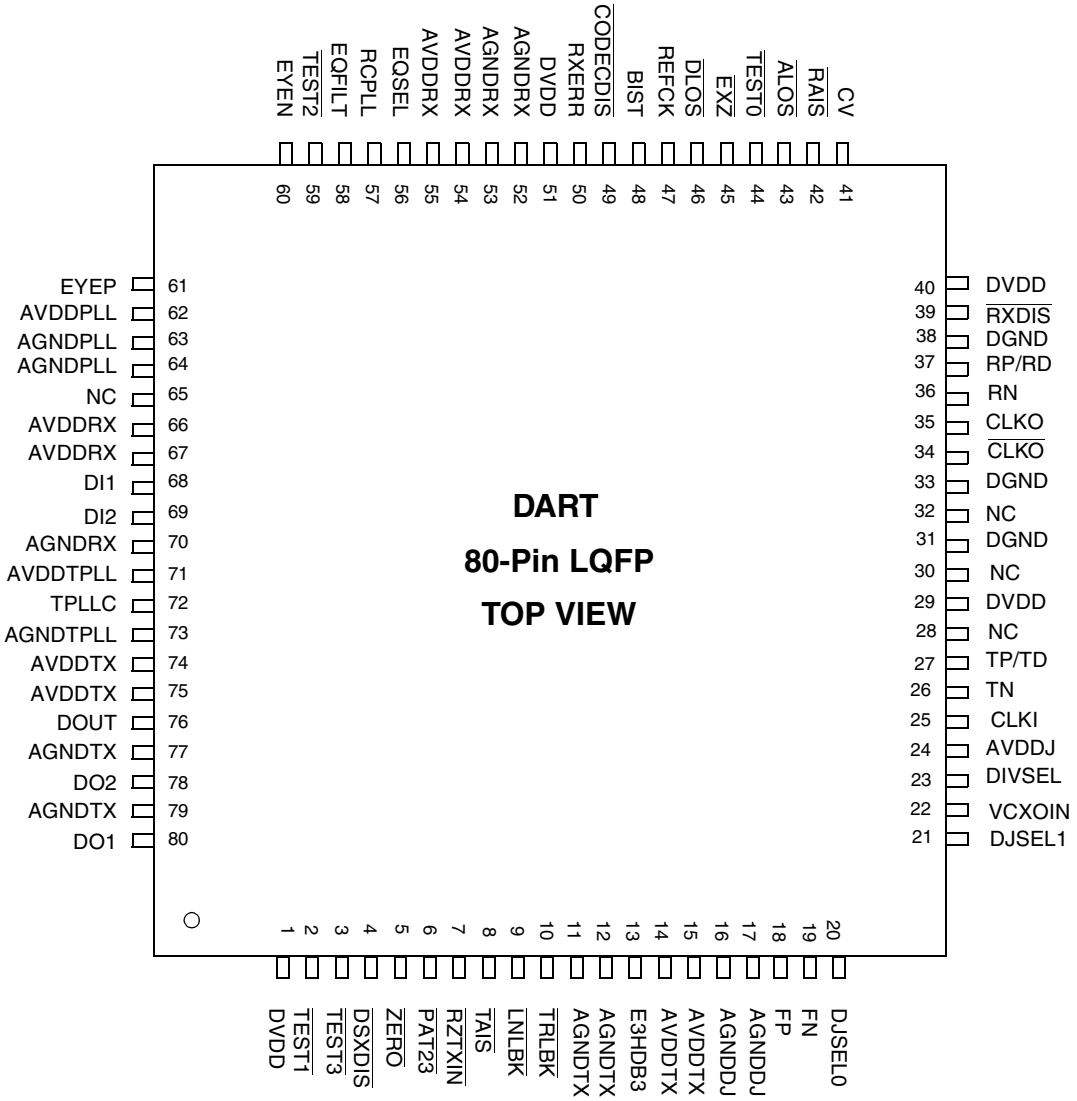


Figure 14. DART TXC-02030 Pin Diagram

PIN DESCRIPTIONS

The following tables describe the 80 pins (leads) of the DART device, grouped by functional category.

POWER SUPPLY AND GROUND

Symbol	Pin No.	I/O/P*	Type	Name/Function
AVDDTX	14 15 74 75	P		**Analog VDD Transmit:** + 5 volt supply ± 5%.
AVDDRX	54 55 66 67	P		**Analog VDD Receive:** + 5 volt supply ± 5%.
AVDDTPLL	71	P		**Analog VDD Transmit PLL:** + 5 volt supply ± 5%.
DVDD	1 29 40 51	P		**Digital VDD:** + 5 volt supply ± 5%.
AVDDPLL	62	P		**Analog VDD Receive PLL:** + 5 volt supply ± 5%.
AVDDJ	24	P		**Analog VDD Dejitter:** + 5 volt supply ± 5%. Leave as NC (No Connect) if the dejitter function is not being used. Use a separate power filter as shown in Figures 31, 32, 33, and 34.
AGNDTX	11 12 77 79	P		**Analog Ground Transmit:** 0 volt reference.
AGNDRX	52 53 70	P		**Analog Ground Receive:** 0 volt reference.
AGNDTPLL	73	P		**Analog Ground Transmit PLL:** 0 volt reference.
DGND	31 33 38	P		**Digital Ground:** 0 volt reference.
AGNDPLL	63 64	P		**Analog Ground Receive PLL:** 0 volt reference.
AGNDDJ	16 17	P		**Analog Ground Dejitter:** 0 volt reference.

*Note: I = Input; O = Output; P = Power

RECEIVE INTERFACE

Symbol	Pin No.	I/O/P	Type *	Name/Function
DI1	68	I	Analog	**Data In 1, Data In 2:** Line side inputs. For single-ended operation DI1 or DI2 must be AC-coupled to ground via a capacitor. For differential operation both inputs can be tied directly to a transformer.
DI2	69	I	Analog	
EYEP	61	O	Analog	**Positive Eye Pattern Monitor:** Monitors non-inverted AGC'd and equalized output from Adaptive Equalizer/AGC block.
EYEN	60	O	Analog	**Negative Eye Pattern Monitor:** Monitors inverted AGC'd and equalized output from Adaptive Equalizer/AGC block.
$\overline{EXZ}$	45	O	CMOS	**Excessive Zeros:** This pin is low for B3ZS coding when three or more consecutive zeros occur in the input data stream. This pin is low for HDB3 coding for four or more consecutive zeros in the data. Ignore when $\overline{DLOS}$ is active (low).
CV	41	O	CMOS	**Coding Violation:** This pin is high when incoming data violates B3ZS (or HDB3) coding for bipolar violations or when three (or four) or more consecutive zeros occur in the input data stream. Valid regardless of the state of $\overline{CODECDIS}$. Ignore when $\overline{DLOS}$ is active (low).
$\overline{DLOS}$	46	O	CMOS	**Digital LOS:** This pin is low when 175 ± 75 consecutive zeros appear in the incoming data stream. Cleared for B3ZS when ones pulse density is in the range of 28 to 33% (or > 33%) for 175 ± 75 pulses. Cleared for HDB3 when ones pulse density is in the range of 20 to 25% (or > 25%) for 175 ± 75 pulses. Valid regardless of the state of $\overline{TRLBK}$ **. May be invalid if the input cable at the receive interface is left disconnected (see LOS Detector section).
$\overline{ALOS}$	43	O	CMOS	**Analog LOS:** For B3ZS this pin is low when pulse density is < 28% for 175 ± 75 pulses. Cleared when pulse density is > 33% for 175 ± 75 pulses. $\overline{ALOS}$ may toggle between active and inactive when pulse density is between 28 and 33%. For HDB3 this pin is low when pulse density is < 20% for 175 ± 75 pulses. Cleared when pulse density is > 25% for 175 ± 75 pulses. $\overline{ALOS}$ may toggle between active and inactive when pulse density is between 20 and 25%. Valid regardless of the state of $\overline{TRLBK}$**. May be invalid if the input cable at the receive interface is left disconnected (see LOS Detector section).
RP/RD	37	O	CMOS	**Receiver Positive/Data:** Generates B3ZS (or HDB3) decoded NRZ, combined data ($\overline{CODECDIS}$ high) or positive rail data ($\overline{CODECDIS}$ low). Held low when $\overline{RXDIS}$ is low.

Symbol	Pin No.	I/O/P	Type *	Name/Function
RN	36	O	CMOS	**Receiver Negative:** Generates negative rail data when $\overline{\text{CODECDIS}}$ is low. Held low when $\overline{\text{CODECDIS}}$ is high and/or when $\overline{\text{RXDIS}}$ is low.
CLKO	35	O	CMOS	**Receiver Clock Out:** Receiver output clock.
$\overline{\text{CLKO}}$	34	O	CMOS	**Receiver Clock Out Inverted:** Receiver inverted output clock.
BIST	48	O	CMOS	**Built-In Self Test Output:** This pin is high when a valid unframed 2^{15}-1 PRBS or 2^{23}-1 PRBS pattern is detected. $\overline{\text{PAT23}}$ pin set low selects 2^{23}-1 PRBS. Valid for both decoded NRZ and PN rail data.
RXERR	50	O	CMOS	**PRBS Analyzer Error:** This pin is high when an invalid PRBS pattern bit is detected.
EQFILT	58	I	Analog	**Equalizer Filter:** Filter pin for adjusting equalizer control.
RCPLL	57	I	Analog	**Clock Recovery External Filter:** Pin for external clock recovery PLL filter adjustment. See Figure 31.
$\overline{\text{TEST3}}$	3	I	TTLp	**Test In 3:** TranSwitch use only. Tie to AVDDRX through a 2 kΩ resistor. See Figure 31.

Notes:

* See Input and Output Parameters section for digital Type definitions.

**For $\overline{\text{TRLBK}}$ low (active), this output signal responds to the receiver input at the DI1 and DI2 pins.

TRANSMIT INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
TP/TD	27	I	TTLp	**Transmitter Positive/Data:** Input pin for unencoded NRZ, combined data ($\overline{\text{CODECDIS}}$ high) or positive rail data ($\overline{\text{CODECDIS}}$ low).
TN	26	I	TTLp	**Transmitter Negative:** Input pin for negative rail data when $\overline{\text{CODECDIS}}$ is low. Must be tied low when $\overline{\text{CODECDIS}}$ is high.
CLKI	25	I	TTLp	**Transmitter Input Clock:** Transmitter clock input. The frequency accuracy of this input clock must be the nominal bit rate ± 20 ppm. The duty cycle must be (50 ± 10)%.
TPLLC	72	I	Analog	**Transmit FIlter Capacitor:** Capacitor pin for filtering calibration PLL voltages (see Figure 31 and following notes for proper connection).
DO1	80	O	Analog	**Data Out Positive:** The output on this pin is a rectangular positive pulse when $\overline{\text{DSXDIS}}$ is low. This pin is a low impedance to AGNDTX when $\overline{\text{DSXDIS}}$ is high.

Symbol	Pin No.	I/O/P	Type	Name/Function
DO2	78	O	Analog	**Data Out Negative:** The output on this pin is a rectangular negative pulse when $\overline{\text{DSXDIS}}$ is low. This pin is a low impedance to AGNDTX when $\overline{\text{DSXDIS}}$ is high.
DOUT	76	O	Analog	**Data Out:** The output on this pin is DSX filtered single-ended when $\overline{\text{DSXDIS}}$ is high. This pin is a high impedance when $\overline{\text{DSXDIS}}$ is low.

CONTROL/REFERENCE PINS

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{RAIS}}$	42	I	TTLp	**Receive AIS Enable:** This pin enables generation of framed DS3 AIS on the receiver outputs when E3HDB3 is low. This pin enables E3 alternating ones AIS when E3HDB3 is high (See Note below).This pin is active low.
$\overline{\text{RXDIS}}$	39	I	TTLp	**Receive Output Disable:** This pin forces the receiver RP/RD and RN outputs to a low state. This pin is active low.
$\overline{\text{TRLBK}}$	10	I	TTLp	**Terminal Loopback Enable:** This pin enables a digital loopback from the transmitter inputs to the receiver terminal side outputs via the Tx I/O Control block, the Loopback Controls block and the Rx I/O Control block. Transmitter output is in the normal condition. See the Loopback and AIS Insertion section for more thorough descriptions. This pin is active low.
$\overline{\text{LNLBK}}$	9	I	TTLp	**Line Loopback Enable:** This pin enables an internal line loopback from the DI1/DI2 inputs to the DOUT or DO1/DO2 outputs. See the Loopback and AIS Insertion section for more thorough descriptions. This pin is active low.
$\overline{\text{RZTXIN}}$	7	I	TTLp	**Transmit RZ Input Enable:** When this pin is low, the device accepts encoded return-to-zero pulses (properly timed and of correct width) on the transmitter TP/TD and TN inputs. CLKI and $\overline{\text{CODECDIS}}$ must be held low. This pin is active low.
$\overline{\text{CODECDIS}}$	49	I	TTLp	**Codec Disable:** When this pin is low, the device bypasses the internal encoder and decoder functions. The decoder remains functional, so that CV and $\overline{\text{EXZ}}$ are always valid. This pin is active low.
$\overline{\text{ZERO}}$	5	I	TTLp	**Transmit Zero Cable Enable:** Hold low for all cable lengths at DS3. This pin is a don't care for E3 operation using DO1 and DO2.
$\overline{\text{TEST2}}$	59	I	TTLp	**Test In 2:** TranSwitch use only. Tie to AVDDRX through a 2 kΩ resistor. See Figure 31.
$\overline{\text{TAIS}}$	8	I	TTLp	**Transmit AIS Enable:** This pin enables generation of framed DS3 AIS on the transmitter outputs when E3HDB3 is low. This pin enables generation of E3 alternating ones AIS when E3HDB3 is high. (See Note below). This pin is active low.

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{DSXDIS}}$	4	I	TTLp	**Transmit DSX Output Disable:** Disables DOUT output and enables DO1/DO2 differential square wave outputs. This pin is active low.
$\overline{\text{TEST0}}$	44	I	TTLp	**Test In 0:** This pin enables an internal PRBS generator (unframed 2^{15}-1 or 2^{23}-1 PRBS generator). Valid for NRZ or PN rail mode. The encoder is used whenever $\overline{\text{TEST0}}$ is active. See the Block Diagram Description, Testability section. This pin is active low.
$\overline{\text{TEST1}}$	2	I	TTLp	**Test In 1:** This pin enables an internal analog terminal side loopback from the TP/TD and TN signals to the receiver outputs. See the Block Diagram Description, Testability section. This pin is active low.
REFCK	47	I	TTLp	**Reference Clock Input:** Input reference clock at the system frequency required for device operation, namely 34.368 MHz for E3, 44.736 MHz for DS3. The required tolerance is the nominal frequency $\pm$ 20 ppm when AIS generation is required and $\pm$ 100 ppm otherwise. The duty cycle tolerance is (50 $\pm$ 10)%.
$\overline{\text{PAT23}}$	6	I	TTLp	**PRBS 2^{23} Select:** This pin, set low, selects a 2^{23}-1 pattern for the PRBS analyzer and generator. This pin, set high, selects a 2^{15}-1 pattern for the analyzer and generator. The encoder is enabled regardless of the state of $\overline{\text{CODECDIS}}$.
E3HDB3	13	I	TTL	**HDB3 or B3ZS Select:** This pin, set high, selects HDB3 encoding/decoding. This pin, set low, selects B3ZS encoding/decoding. This TTL pin has no internal pull-up resistor.
DJSEL0	20	I	TTLp	**Dejitter Block Control:** First of two control pins which control the dejitter buffer/dejitter PLL modes. See “Dejitter Control Signals” Table 1.
DJSEL1	21	I	TTLp	**Dejitter Block Control:** Second of two control pins which control dejitter buffer/dejitter PLL modes. See “Dejitter Control Signals” Table 1.
DIVSEL	23	I	TTLp	**Divide Select:** Selects the divisor in the divide-by block in the dejitter PLL. See “Dejitter PLL Divide Control” Table 2.
EQSEL	56	I	TTLp	**Equalizer select pin:** Set low to select the amplitude-controlled equalizer.

Note: DS3 AIS is defined as a valid M-frame with proper subframe structure. The data payload is a 1010 ... sequence starting with a 1 after each overhead bit. Overhead bits are as follows: F0=0, F1=1, M0=0, M1=1; C-bits are set to 0; X-bits are set to 1; and P-bits are set for valid parity.

MISCELLANEOUS PINS

Symbol	Pin No.	I/O/P	Type	Name/Function
FP	18	O	CMOS	**Filter Charge-pump Positive:** This pin provides a 2 mA driver output to the external dejitter PLL filter.
FN	19	O	CMOS	**Filter Charge-pump Negative:** This pin provides a 2 mA driver output to the external dejitter PLL filter.
VCXOIN	22	I	TTLp	**External VCXO:** This pin is used to input the dejittered clock from the external VCXO output.

NO CONNECTS

Symbol	Pin No.	I/O/P	Type	Name/Function
NC	28 30 32 65			**No Connect:** NC pins are not to be connected, not even to another NC pin, but must be left floating. Operation may be impaired or the device may be damaged if NC pins are connected.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.3	+7.0	V	Note 1
DC input voltage	V_{IN}	-0.3	V_{DD} + 0.3	V	Note 1
Ambient operating temperature	T_A	-40	85	°C	0 ft/min linear airflow
Storage temperature range	T_S	-55	150	°C	Note 1
Component Temperature x Time	TI		270 x 5	°C x s	Note 1
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	absolute value 2000		V	Note 3

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the “CAUTION” label on the drypack bag in which devices are supplied.
3. Test method for ESD per MIL-STD-883D, Method 3015.7.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance: junction to ambient		50		°C/W	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
I_{DD}		150	160	mA	Outputs terminated
P_{DD}		750	840	mW	Inputs switching, V_{DD}=5.25 for Max

INPUT AND OUTPUT PARAMETERS

Input Parameters for TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		V_{DD} + 0.3	V	
V_{IL}	- 0.3		0.8	V	
I_{IH}			- 10	µA	V_{DD} = 5.25V
I_{IL}			550	µA	V_{DD} = 5.25V
Input Capacitance			10	pF	

Note: All TTL input pins with the exception of the E3HDB3 pin have an internal pull-up resistor.

Output Parameters for CMOS

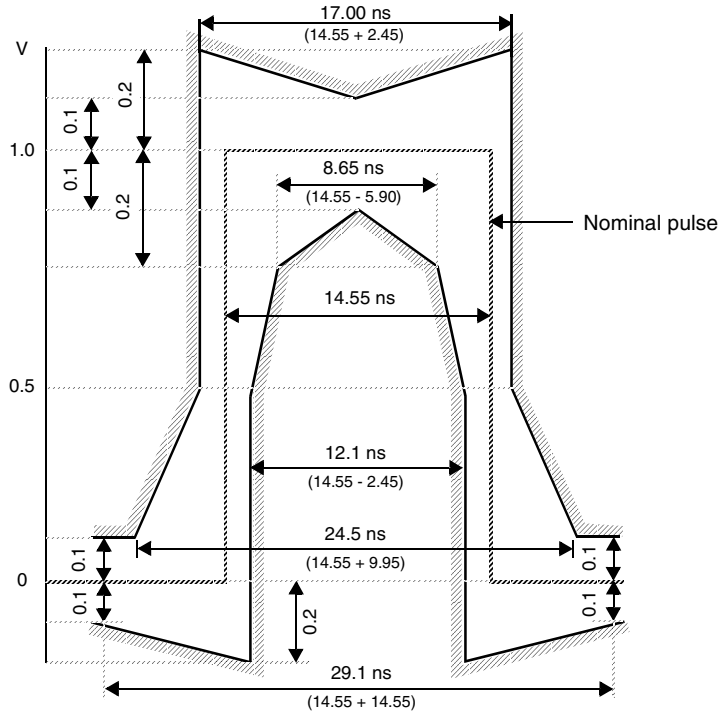
Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	4 mA source
V_{OL}			0.5	V	4 mA sink
I_{OH}			- 4.0	mA	V_{DD} = 4.75V
I_{OL}			4.0	mA	V_{DD} = 4.75V
t_{RISE}	1.7	2.7	4.2	ns	C_{LOAD} = 15 pF
t_{FALL}	1.9	2.8	4.1	ns	C_{LOAD} = 15 pF

Note: For driving traces greater than 2 inches or driving multiple loads, the DART digital outputs should be buffered.

TIMING CHARACTERISTICS

E3 LINE SIDE TIMING CHARACTERISTICS

The line side timing characteristics of the DART are designed so that the line output at the transformer output meets the pulse shape specified in ITU-T Rec. G.703 for 34368 kbit/s operation. The pulse mask is shown in Figure 15. Refer to ITU-T Rec. G.703 for further details regarding the pulse mask.

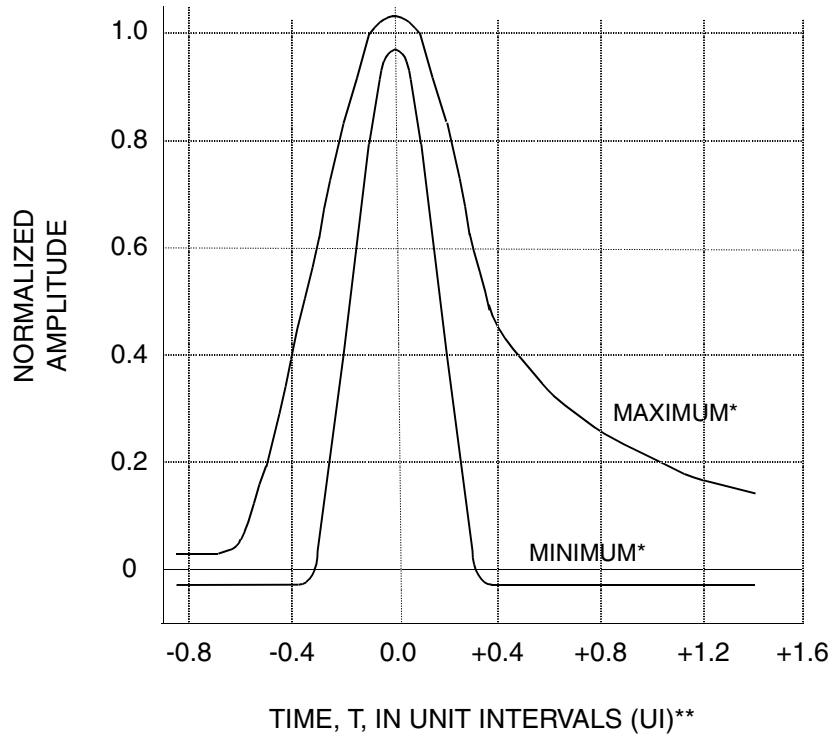


Reference: ITU-T Recommendation G.703

Figure 15. Pulse Mask at the 34368 kbit/s Interface

DS3 LINE SIDE TIMING CHARACTERISTICS

The line side signal characteristics are designed so that the output meets the requirements of Bellcore GR-499-CORE, Issue 1, December 1995. When terminated into a test load of 75 ohm ± 5% using ATT 734A coaxial cable the DART device will meet the DS3 interface isolated pulse mask defined below in Figures 16 and 17 for a cable distance of 0 to 450 feet. The pulse measurement is made using a Hewlett Packard HP54502A oscilloscope (or equivalent) in the average mode, which is described in the HP instruction manual for this instrument. The input to the DART device is a 2^{15}-1 pseudo-random binary sequence (PRBS) signal.



* Note: The DS3 curves shown are approximate representations of the equations in Figure 17.

**Note: UI = 1 / (System Clock Frequency).

Figure 16. DS3 Interface Isolated Pulse Mask

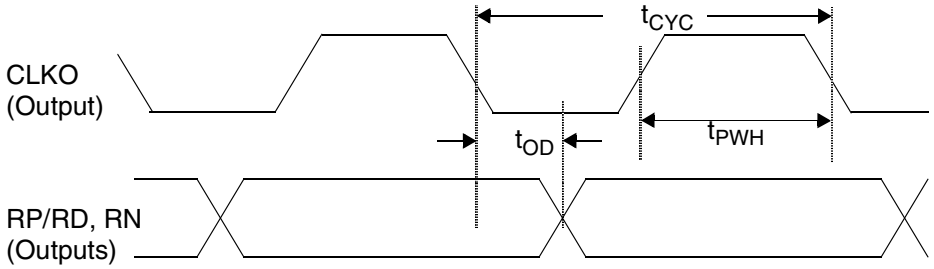
CURVE	TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
MAXIMUM (UPPER) CURVE	$-0.85 \le T \le -0.68$ $-0.68 \le T \le 0.36$ $0.36 \le T \le 1.4$	0.03 $0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.34}\right)\right]+0.03$ $0.08 + 0.407e^{-1.84(T-0.36)}$
MINIMUM (LOWER) CURVE	$-0.85 \le T \le -0.36$ $-0.36 \le T \le 0.36$ $0.36 \le T \le 1.4$	-0.03 $0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.18}\right)\right]-0.03$ -0.03

Figure 17. DS3 Interface Isolated Pulse Mask Equations

DIGITAL TERMINAL SIDE TIMING DIAGRAMS

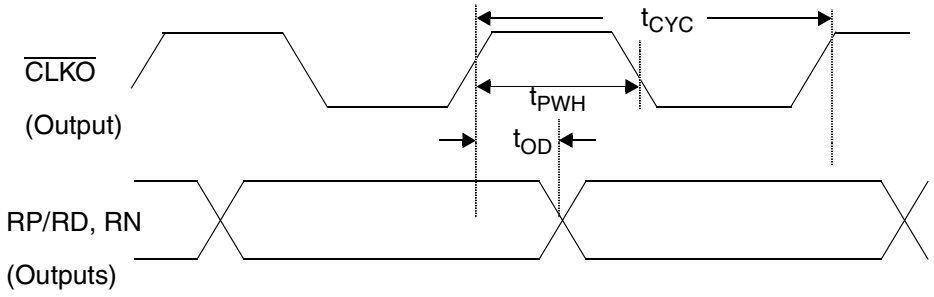
Detailed timing diagrams for the DART are illustrated in Figures 18 through 22, with values of the timing intervals in included tables. All output times are measured with a maximum 15 pF load capacitance. Timing parameters are measured at voltage levels of $(V_{OH} + V_{OL})/2$ for outputs or $(V_{IH} + V_{IL})/2$ for inputs.

Figure 18. Receiver CLKO to Data Output Timing



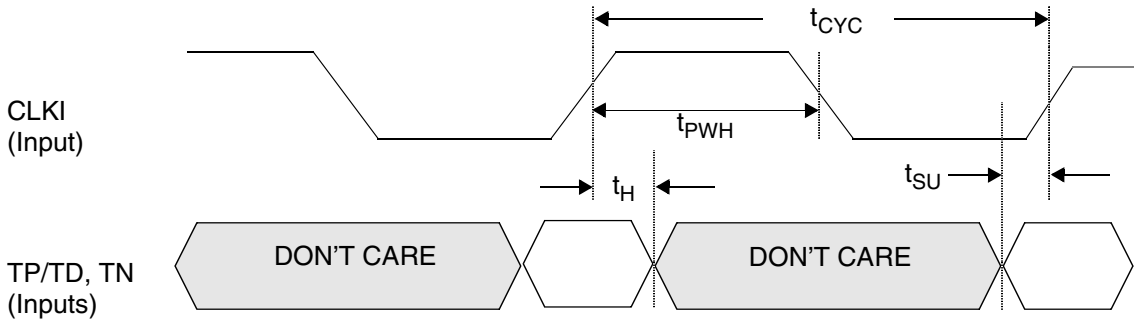
Parameter	Symbol	Min	Typ	Max	Unit
CLKO, E3 output clock period	t_{CYC}		29.097		ns
CLKO, DS3 output clock period	t_{CYC}		22.353		ns
Output clock duty cycle, t_{PWH}/t_{CYC}	--	45		55	%
RP/RD,RN data output delay after CLKO↓	t_{OD}	0.0		3.0	ns

Figure 19. Receiver $\overline{\text{CLKO}}$ to Data Output Timing



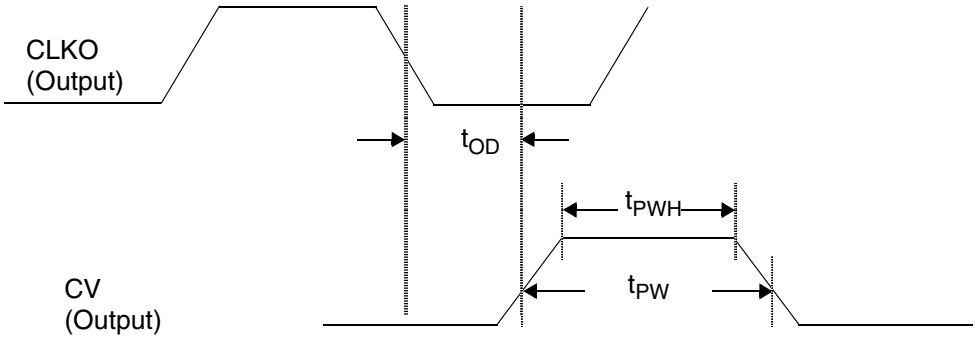
Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{CLKO}}$, E3 output clock period	t_{CYC}		29.097		ns
$\overline{\text{CLKO}}$, DS3 output clock period	t_{CYC}		22.353		ns
Output clock duty cycle, t_{PWH}/t_{CYC}	--	45		55	%
RP/RD,RN data output delay after $\overline{\text{CLKO}}$↑	t_{OD}	0.0		3.0	ns

Figure 20. Transmitter Input Timing



Parameter	Symbol	Min	Typ	Max	Unit
CLKI, E3 input clock period	t_{CYC}		29.097		ns
CLKI, DS3 input clock period	t_{CYC}		22.353		ns
Input clock duty cycle, t_{PWH}/t_{CYC}	--	40		60	%
TP/TD, TN data stable to CLKI↑ setup time	t_{SU}	1.0			ns
CLKI↑ to TP/TD, TN data stable hold time	t_H	2.0			ns

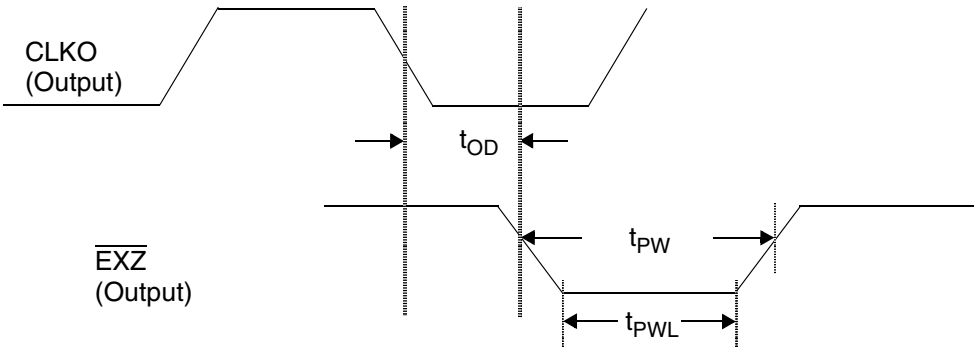
Figure 21. Coding Violation Pulse Timing



Parameter	Symbol	Min	Typ	Max	Unit*
CV pulse width	t_{PW}	0.9	1.0	1.1	UI
CV pulse high time (90% level)	t_{PWH}	0.8	0.9	1.0	UI
CV delay from occurrence of violation	t_D		9.0		UI
CV output delay after CLKO↓	t_{OD}	0.0		3.0	ns

*Note: UI = 1 / (System Clock Frequency)

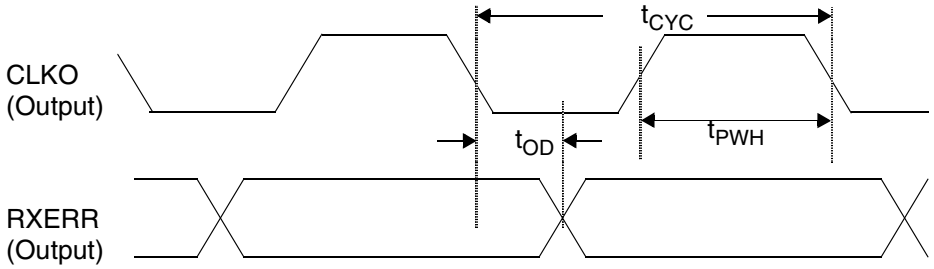
Figure 22. Excessive Zeros Pulse Timing



Parameter	Symbol	Min	Typ	Max	Unit*
$\overline{EXZ}$ pulse width	t_{PW}	0.9	1.0	1.1	UI
$\overline{EXZ}$ pulse low time (10% level)	t_{PWL}	0.8	0.9	1.0	UI
$\overline{EXZ}$ delay from occurrence of violation	t_D		7.0		UI
$\overline{EXZ}$ output delay after CLKO↓	t_{OD}	0.0		3.0	ns

*Note: UI = 1 / (System Clock Frequency)

Figure 23. Receiver CLKO to RXERR Output Timing



Parameter	Symbol	Min	Typ	Max	Unit
CLKO, E3 output clock period	t_{CYC}		29.097		ns
CLKO, DS3 output clock period	t_{CYC}		22.353		ns
Output clock duty cycle, t_{PWH}/t_{CYC}	--	45		55	%
RXERR output delay after CLKO↓	t_{OD}	9.0		14	ns

Table 3. Receiver and Transmitter Latencies

DART Delay (Non-Dejitter Mode)*			
Direction of Signal Flow	**NRZ Data**	**PN Data**	**CV (both modes)****
Rx In to Rx Out	9.3 ± 0.2 UI	3.3 ± 0.2 UI	9.3 ± 0.2 UI
Tx In to Tx Out	6.5 ± 0.3 UI	3.5 ± 0.3 UI	Not Applicable

* Note: When using the dejitter FIFO, typically an additional 26 UI of delay will be added (i.e., one-half the 52-bit FIFO).

**Note: The CV occurs at the output at the same time as the bit causing the coding violation. The bit violating the coding may not be the actual error bit, but is directly related.

OPERATION

RECEIVER LINE SIDE INPUT REQUIREMENTS

Parameter	Value
Interface Cable	AT&T 728A/734A coaxial (equivalent or better).
Bit Rate:	
E3	34.368 Mbit/s ± 20 ppm
DS3	44.736 Mbit/s ± 20 ppm
Line Code	B3ZS or HDB3
Input Signal Amplitude:	
Single-Ended Input	35 mVp - 1.1 Vp AC (measured relative to other pin used for DC bias, DI1 or DI2).
Differential Input	35 mVp - 1.1 Vp AC (magnitude of differential amplitude between DI1 and DI2).
Dynamic range	30 dB
Cable Length	0 - 900 feet; 1300 feet for E3 (for signals meeting the transmit masks).
Input Return Loss:	
E3	> 26 dB at 17.184 MHz with external 75 Ω resistor (effect of external transformer excluded).
DS3	> 26 dB at 22.368 MHz with external 75 Ω resistor (effect of external transformer excluded).
Input Resistance	> 5 kΩ
Signal-to-Noise Tolerance	No greater than either the value produced by adjacent pulses in the data stream or ±10% of the peak pulse amplitude, whichever is greater.
Input Jitter Tolerance	As defined by Figures 29 and 30
Signal Coupling	The input signal must be AC-coupled to the DART via a transformer or capacitor.
$\overline{\text{DLOS}}$ Input level	A “0” is defined as a signal amplitude ≤ 15 mVp at the receiver input.

INTERFERING TONE TOLERANCE

The DART will properly recover clock and present error-free output to the receive terminal side interface in the presence of a sinusoidal interfering tone signal as described in Tables 4 and 5:

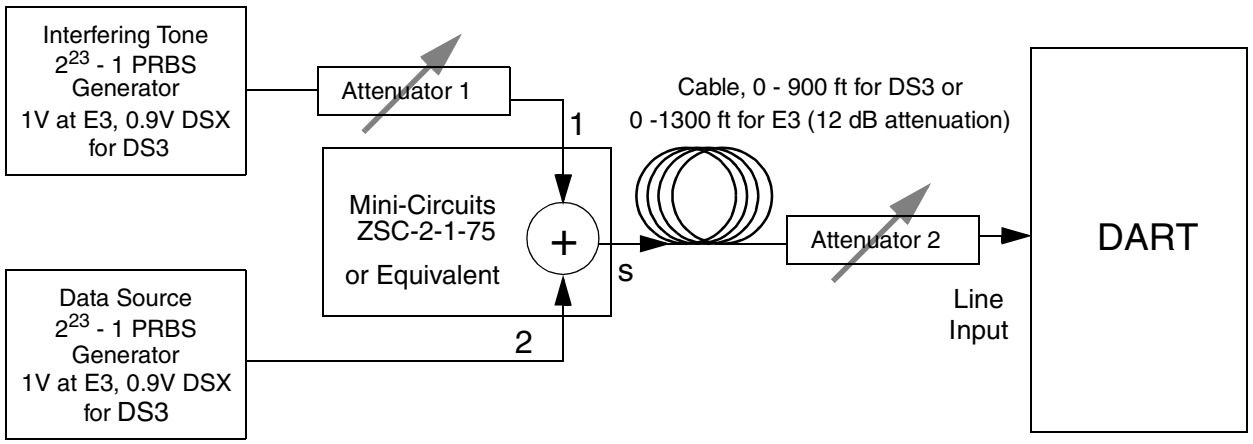


Figure 24. Interference Margin Test Configuration

Table 4. E3 Interfering Tone Tolerance

Test Number	Attenuator 2	Temperature Range	Attenuator 1 (see Note 2)
1	See Note 1	-40 to 85 °C	18 dB
2	0 dB	-40 to 85 °C	14 dB
3	12 dB	-40 to 85 °C	14 dB

Table 5. DS3 Interfering Tone Tolerance

Test Number	Attenuator 2	Temperature Range	Attenuator 1 (see Note 2)
1	See Note 1	-40 to 85 °C	18 dB
2	0 dB	-40 to 85 °C	14 dB
3	12 dB	-40 to 85 °C	14 dB

Notes:

1. Adjust attenuator 2 to deliver a 35 mV peak signal to the DART device with no interfering tone present.
2. Attenuator 1 value is the minimum attenuation of the interfering tone that yields no data errors. A 0 dB setting of attenuator 1 would provide interfering tone and data at the same amplitude.
3. See Figure 24 “Interference Margin Test Configuration” for test setup.

RECEIVER TERMINAL SIDE OUTPUT SPECIFICATIONS

Parameter	Value
Clock Recovery Jitter Peaking	1 dB maximum
Clock Recovery PLL Pull-in Time	< 100 µs
Sequences Reported as Coding Violations	++, --, B0V when coming after an odd number of ones, 00V when coming after an even number of ones, three or more consecutive zeros (excessive zeros) for B3ZS. ++, --, +0+, -0-, B00V when coming after an odd number of ones, 000V when coming after an even number of ones, four or more consecutive zeros (excessive zeros) for HDB3.

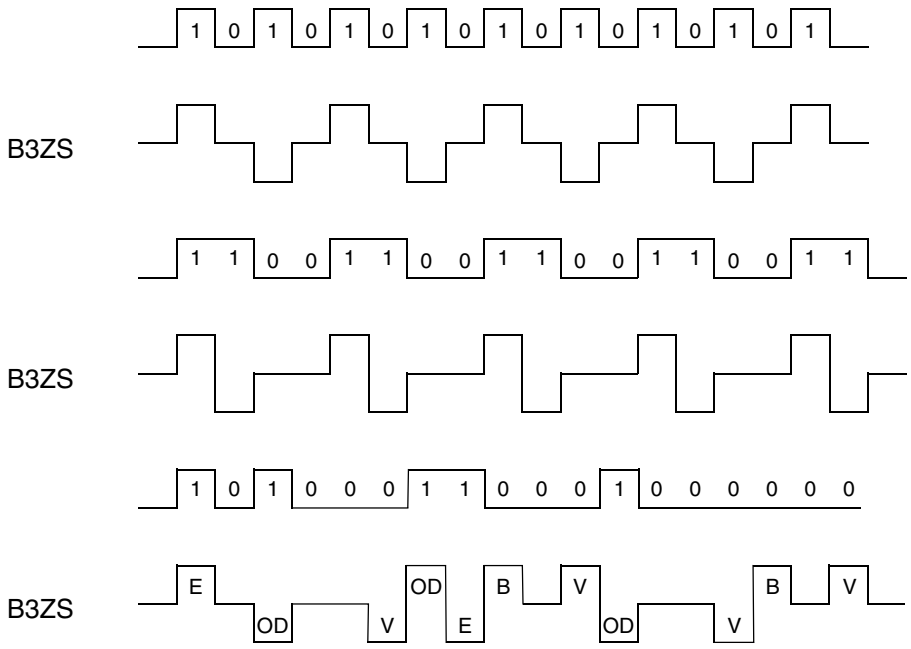
TRANSMITTER LINE SIDE OUTPUT SPECIFICATIONS

Parameter	Value
DO1/DO2 Output Characteristics (Note 1):	
Pulse Shape (E3)	As defined in ETS 300 689 Sec. 4.2.1.2 and ITU-G.703 measured at the transmitter 75 ohm load.
Amplitude	± 1 volts ± 8% measured at the transmitter 75 ohm load.
Output Power for E3	No specification for E3 output power.
Pulse Imbalance	Ratio of positive and negative pulse amplitudes: 0.90 - 1.10.
Pulse Symmetry	Output power at system frequency > 20 dB below the level at one-half the system frequency.
DOUT Output Characteristics, $\overline{\text{ZERO}}$ low (Note 1):	
Pulse Shape (DS3)	As defined by Figure 2 in ANSI T1.404-1994, ANSI T1.404a-1996, TIE1.2/93-004, with 0 to 450 ft of cable and as defined by Figure 9.8 in GR-499-CORE.
Amplitude	±0.75 Volts ± 10%
Pulse Imbalance	Ratio of positive and negative pulse amplitudes is 0.90 - 1.10.
Pulse Symmetry	Output power at system frequency is > 20 dB below the level at one-half the system frequency.
Output jitter (Note 2)	0.05 UI maximum with jitter-free input clock on CLKI or when in transmit side dejitter mode.
Output Power for DS3	Between -4.7 and +3.6 dBm for a framed AIS pattern in a wide-band power measurement. The measurement equipment should have a low-pass filter with a flat passband and a cutoff frequency of 200 MHz. The effects of a range of connecting cable lengths of 225 feet to 450 feet of coax must be included in the measurement. This measurement is defined in ANSI T1.102-1993 and ANSI T1.404-1994.
All Ones Output Power for DS3	Between -1.8 and +5.7 dBm for an all ones signal measured using a bandpass filter with a 3 dB bandwidth of 3 kHz ± 1 kHz centered at 22.368 MHz. This measurement is defined in ANSI T1.102-1993 and ANSI T1.404-1994.

Notes:

1. A 75 Ω ±5% output load is assumed in these specifications. Measurements are made at transmitter unless otherwise noted.
2. UI = 1 / (System Clock Frequency)

B3ZS PATTERNS



E = indicates even number of pulses since last violation (V).

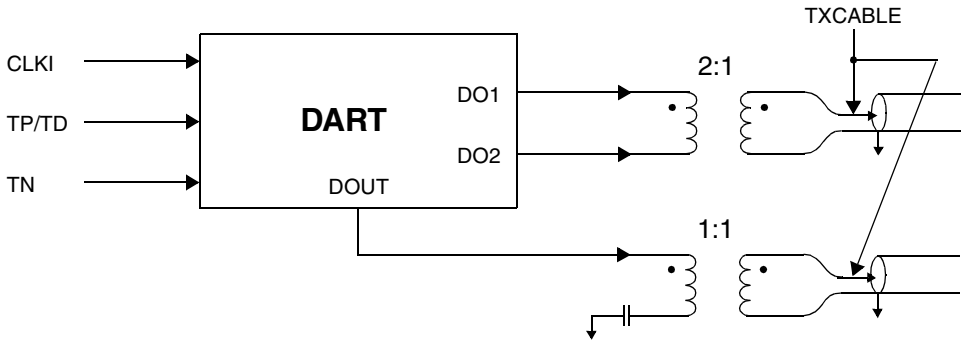
OD = indicates odd number of pulses since last violation (V).

V = inserted pulse, in intentional violation of alternating plus and minus pulses used for ones.

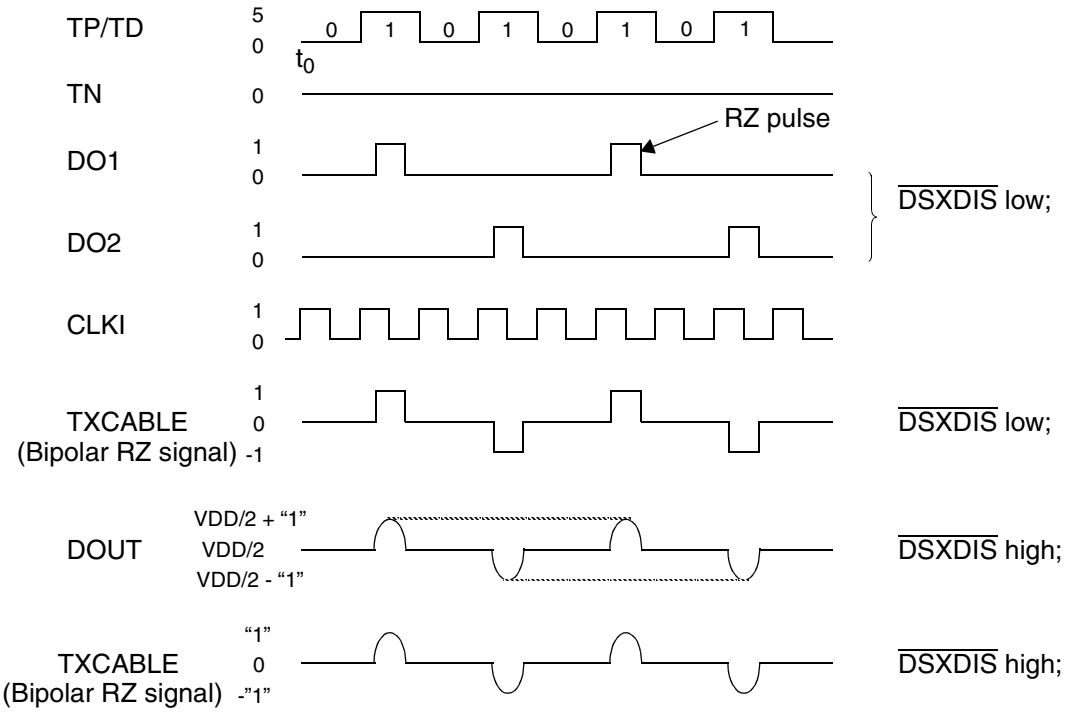
B = inserted pulse that follows the normal alternating bipolar coding scheme (i.e., polarity opposite to preceding pulse).

Note: Three consecutive zeros are replaced with B0V or 00V. The substitution choice is made so that the number of pulses between inserted violation pulses (Vs) is odd. Note that sequential violations are of opposite polarity, so the net charge on the transmission medium is zero.

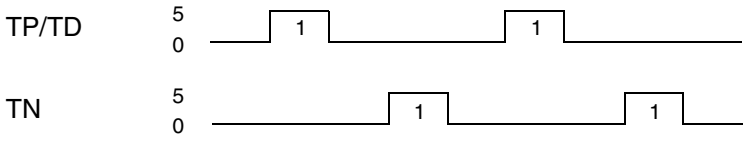
Figure 25. Examples of B3ZS Coding (HDB3 Similar)



Unencoded NRZ Data (0 1 0 1 0 .....)



Encoded NRZ P & N Data (0 1 0 1 0 ....)



DO1, DO2, DOUT, CLKI and TXCABLE are the same as in the unencoded NRZ case.

Figure 26. Examples of Idealized Transmit Input and Output Data Using B3ZS Coding

Table 6. AIS and Loopback Control Signal Arbitration

$\overline{\text{TEST0}}$	$\overline{\text{TEST1}}$	$\overline{\text{RAIS}}$	$\overline{\text{TAIS}}$	$\overline{\text{LNLBK}}$	$\overline{\text{TRLBK}}$	Rx Terminal Output	Tx Line Output
1	1	1	1	1	1	Normal	Normal
1	1	1	0	X	1	Normal	AIS
1	X	1	0	X	0	Digital Terminal Loopback	AIS
1	X	0	1	1	X	AIS	Normal
1	X	0	1	0	X	AIS	Line Loopback
1	X	0	0	X	X	AIS	AIS
1	1	1	1	1	0	Digital Terminal Loopback	Normal
1	1	1	1	0	1	Normal	Line Loopback
1	1	1	1	0	0	Digital Terminal Loopback	Line Loopback
1	0	1	1	1	1	Terminal Loopback*	Normal
0	1	1	X	X	1	Normal	PRBS
0	0	1	X	X	1	Terminal Loopback of PRBS*	PRBS
0	X	1	X	X	0	Digital Terminal Loopback*	PRBS

* Through Clock Recovery block for terminal transmit data.

Notes:

1. X = Don't care.
2. Digital terminal loopback means that the terminal side transmitter inputs are looped digitally, directly to the terminal side receiver outputs.
3. $\overline{\text{LNLBK}}$ low and $\overline{\text{CODECDIS}}$ high results in the received data being decoded followed by encoding before being transmitted. Code violations will be lost in the encoded, transmitted data.
4. $\overline{\text{LNLBK}}$ low and $\overline{\text{CODECDIS}}$ low results in the PN received data being passed to the transmitter output with no changes. Code violations will be preserved.

POWER-DOWN MODE

In order to reduce the current required by the DART when either the transmitter or the receiver is not used, the following power pins may be tied to ground:

Receiver-Only Operation: AVDDTX pins 14, 15, 74, 75.

Transmitter-Only Operation: AVDDRX pins 54, 55, 66, 67. AVDDPLL pin 62.

Current reduction in the Power-Down Mode is as follows:

Receiver-Only Operation: IDD is reduced by approximately 30 mA.

Transmitter-Only Operation: IDD is reduced by approximately 80 mA.

Note: Power must be provided to the AVDDTPLL pin in all three operational modes (Receiver and Transmitter, Receiver-Only or Transmitter-Only). Refer to Figure 31 and associated Note 7 for power supply connections.

JITTER TRANSFER AND GENERATION

Jitter Transfer

Transfer of jitter through an individual unit of digital equipment is characterized by the relationship between the applied input jitter and the resulting output jitter as a function of frequency. This standard does not apply to line interface units, as the recovered data is either re-transmitted with a local oscillator or is re-transmitted with the recovered clock that has been dejittered using a dejitter PLL. In short, the recovered clock is never used to directly transmit data. Studying the jitter tolerance curve highlights the reason why this is not possible. The receive PLL bandwidth is dictated by the jitter tolerance curve. This prevents the clock recovery circuit having the low bandwidth necessary for low jitter in the low frequencies necessary for transmitting.

The measurement made with the test setup shown in Figure 27 is for information only. The measurement of the jitter on CLKO is a measure of the characteristics of the clock recovery PLL, not how much jitter is transferred from the receiver input to the transmitter output.

For E3, ITU-T Recommendation G.823 further describes and defines jitter transfer.

For DS3, Bellcore Technical Reference GR-499-CORE, Issue 1, 1995 further describes and defines jitter transfer.

In a line-side looped back configuration (from the receive terminal side outputs, externally looped back to the terminal side inputs), in the absence of applied input jitter, the amount of jitter introduced by the DART device is a maximum of 0.065 Unit Intervals (UIs, where UI is 1/System Clock Frequency) of peak-to-peak jitter over a jitter frequency range of 20 Hz to 1 MHz (filter with high-pass of 10 Hz and a low-pass of 1.1 MHz).

The test arrangement illustrated in Figure 27 is recommended for performance of the jitter transfer test. This test is made by adding jitter to the line side data inputs (DI1 and DI2) and measuring the jitter at the terminal side receiver clock output (CLKO). Intrinsic test equipment jitter must be subtracted from the measurement. The receiver outputs (RP/RD, RN and CLKO) are looped back to the transmitter inputs (TP/TD, TN and CLKI) using cables. The transmitter is active to verify that there is no crosstalk between the transmitter and receiver.

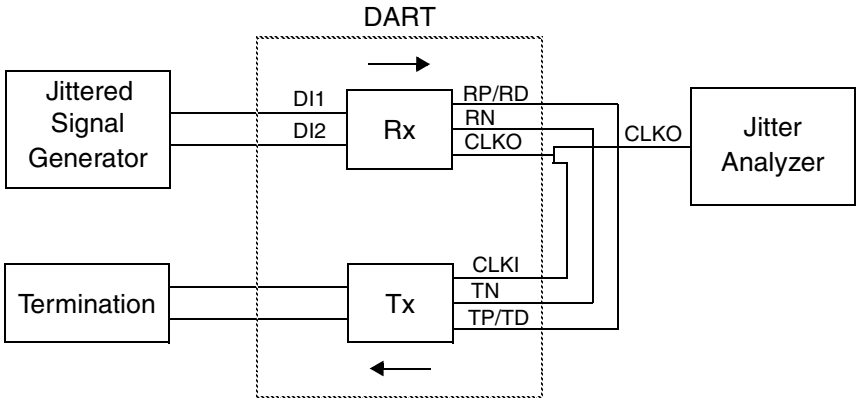


Figure 27. Jitter Transfer Test Arrangement

Jitter Generation

Jitter generation is the process whereby jitter appears at the output port of an individual unit of digital equipment in the absence of applied input jitter.

For E3, ITU-T Rec. G.703, SS 666339, ETSI TBR24, and ETS 300 689 specify the maximum jitter generation to be 1.5 UI peak-to-peak at the output of the terminal receiver for Category I equipment, 0.5 UI in a repeater application.

For DS3, Bellcore Technical Reference GR-499-CORE, Issue 1, 1995 specifies the maximum jitter generation to be 1.0 UI peak-to-peak at the output of the terminal receiver for Category I equipment.

The test arrangement illustrated in Figure 28 is used for performance of the jitter generation test. This test is made by using a jitterless transmit clock and then measuring the jitter at the output of the transmitter. A filter from 10 Hz to 400 kHz is used. Intrinsic test equipment jitter is subtracted from the measurement. The E3/DS3 jitter generation within the DART device is 0.05 UI peak-to-peak maximum for all frequencies specified in the three standards referenced above.

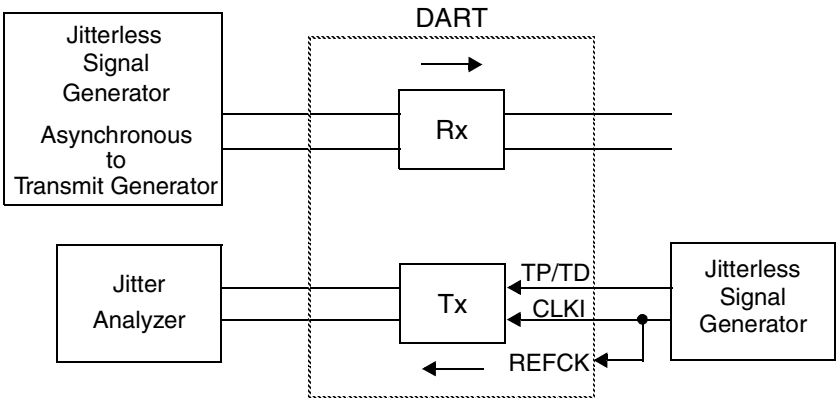


Figure 28. Jitter Generation Test Arrangement

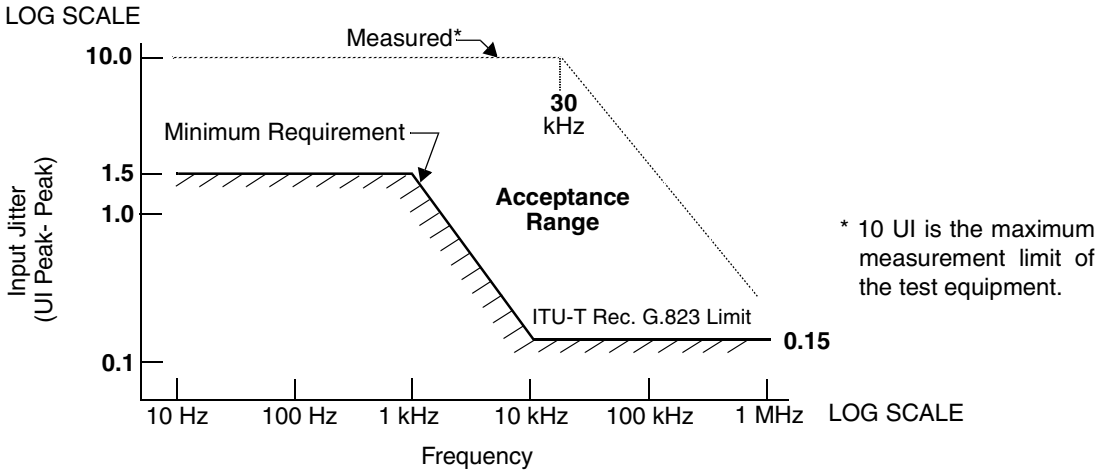
JITTER TOLERANCE

Input jitter tolerance is the maximum amplitude of sinusoidal jitter at a given jitter frequency, which when modulating the signal at an equipment port, results in no more than two errored seconds cumulative, where these errored seconds are integrated over successive 30-second measurement intervals and the jitter amplitude is increased in each succeeding measurement interval.

Requirements on input jitter tolerance are specified in terms of compliance with a jitter mask, which represents a combination of points. Each point corresponds to a minimum amplitude of sinusoidal jitter at a given jitter frequency which, when modulating the signal at an equipment input port, results in two or fewer errored seconds in a 30-second measurement interval.

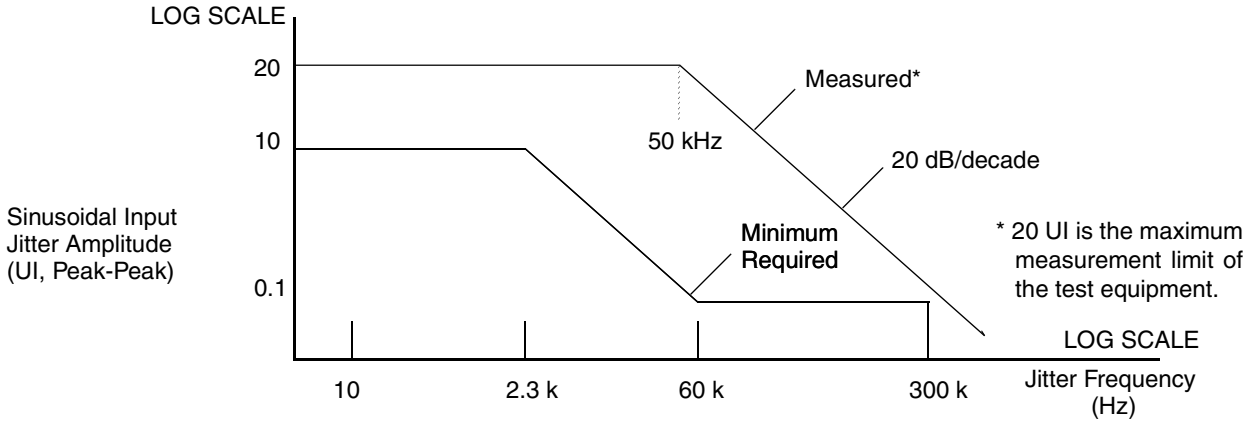
E3: ITU-T Recommendation G.823 specifies that network equipment must be able to accommodate and tolerate levels of jitter up to certain specified limits. The DART device accommodates and tolerates more input jitter than the level of input jitter specified by this recommendation. The tolerance curve and the measured curve are shown in Figure 29.

DS3: Bellcore Technical Reference GR-499-CORE, Issue 1, December 1995 specifies the minimum requirement jitter tolerance curve for Category II equipment (most stringent requirement). Jitter tolerance within the DART device meets and exceeds the performance requirements. Figure 30 presents the DS3 Bellcore minimum jitter tolerance requirement curve and the measured performance.



Notes: Unit Interval (UI) = 1/(System Clock Frequency) = 29.10 ns
Test conditions: V_{DD} = 5 V, T_A = 25 °C, HDB3 coding, 2^{15}-1 PRBS data pattern

Figure 29. Input Jitter Tolerance for E3



Notes: Unit Interval (UI) = 1/(System Clock Frequency) = 22.35 ns
Test conditions: V_{DD} = 5V, T_A = 25 °C, B3ZS coding, 2^{15}-1 PRBS data pattern

Figure 30. Input Jitter Tolerance for DS3

PHYSICAL DESIGN

High-frequency design techniques must be employed for layout of the printed circuit board on which the DART device is mounted. A summary of the special design requirements is provided below. More details are available in TranSwitch Application Note AN-406, Guidelines for ART/ARTE Printed Circuit Board Layout, Document Number TXC-02020-AN1.

The following guidelines and suggestions should be adhered to for a successful board design. At the E3 and DS3 frequencies it is important to use high-frequency layout techniques. The set of techniques discussed below is the bare minimum that should be used.

A solid ground plane with notches should be used. 'Solid' in this instance means that the impedance from any point in the plane to the board ground connection should be low. This means having as much metal left in the plane as possible. This is very important in regards to the location of the analog DART device, since its SNR can be severely degraded by I*Z drops in these planes. Notching is used to direct (i.e., steer) noise-induced current away from the DART device's ground return path. Under no circumstances should a DART device's ground region be connected to the "ground" through a trace. The trace is an impedance at high frequencies and not a short. Ground currents through the trace impedance will cause voltage noise. Do not run AC signals across the notches in the ground plane, as this will produce an impedance discontinuity and signal integrity will be affected.

Try to place the DART device in a manner that results in no high current devices (such as oscillators or drivers) being placed in line with the DART device and the card ground connection.

Do not use a solid power plane. Break the power plane into regions. Placing the power and ground planes in adjacent layers will produce an additional noise reduction due to capacitive coupling. For example, a six-layer board could be signal-signal-power(ground)-ground(power)-signal-signal. The following is the list of power regions:

1. Analog Receiver power, AVDDRX (tie AVDDPLL to AVDDRX)
2. Analog Transmitter power, AVDDTX (tie AVDDJ to AVDDTX)
3. Analog PLL power, AVDDTPLL
4. DART Digital power, DVDD
5. DART Dejitter PLL power, AVDDJ
6. Board power, VDD

If ferrite beads are used in the analog power lines, as is recommended, there will be a narrowing of the power plane at the ferrite bead. If the beads are not used, use as wide a path as possible back to the common connecting point. It should be noted that not using the beads may cause a large SNR reduction in the transceiver. The effect is highly board dependent and not easily predictable.

Figure 31 shows the recommended ground and power connections for the DART device. The passive components should be connected to the indicated ground (a solid plane with possible notching). Connecting the components to the wrong point will inject a noise signal into that part of the transceiver. Do not use a long trace to connect components to ground. Always use as short a trace as possible. The decoupling capacitors should be placed as close as feasible to their associated device pins and on the same side of the board as the DART device. Put a decoupling capacitor at every power pin. Placing the capacitors on the other side of the board may have a measurable impact on device performance. Again, it should be pointed out that a board trace is an impedance, not a short. The other passive components should also be placed as close as possible to their associated pins.

The DART terminal side CMOS output drivers have a drive capability of 4 mA. If driving long traces (the longer the trace, the greater the parasitic capacitance) or multiple loads these outputs may need to be buffered.

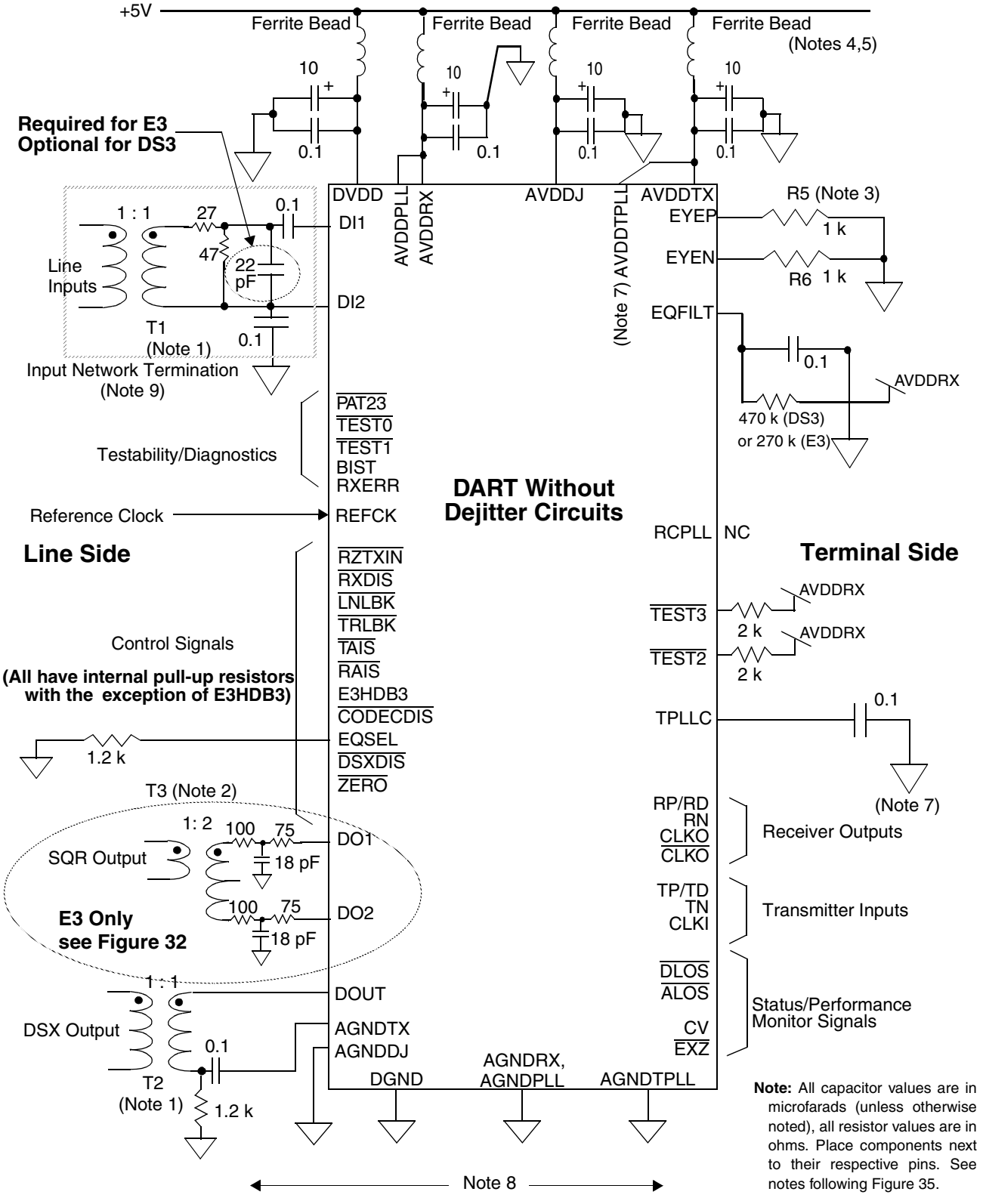
The notes at the bottom of Figure 31 give external component values and types, a listing of the various powers and grounds and other general information.

General Comments

A board trace at high frequencies is not a zero impedance metal interconnection. It is a distributed LC network. The values of the L and C (per unit length) parasitic components are determined by trace geometry (width and height) and the surrounding material (which determines the dielectric constant). A trace with a given geometry will have a different impedance if it is on an outside board layer from the same trace placed instead in an internal layer. Large branches (stubs) off a main trace will change the impedance at the branch point due to the effect of impedances in parallel, so branch lengths should be kept to a minimum (less than a quarter wavelength). This is very important for clock lines where load/source impedance mismatches can cause severe ringing, which leads to timing problems. Use buffers to reduce the difficulty of distributing a signal with multiple loads.

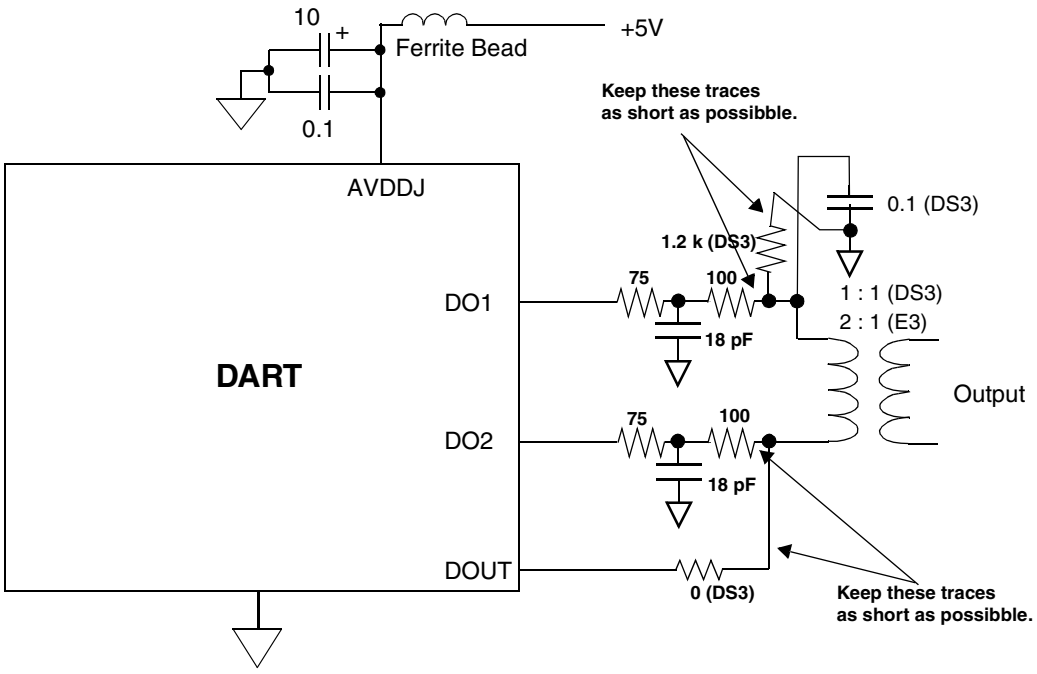
If relays are used to switch the transceivers in and out, use the 75 ohm shielded variety to minimize crosstalk, especially from the power used to energize the relay. Match the impedance of the board traces of the transmitter outputs and receiver inputs to the transmission line impedance (75 ohms if a 1:1 transformer is used) to minimize reflections. Physically separate the analog signal lines from the digital lines. Route the differential receiver lines side by side to make coupled noise common-mode. Use guard traces on the receive lines. These guard traces should be tied to ground. Avoid ninety-degree corners in the board lands, keeping lands as straight and short as possible. Use terminating (i.e., 51 ohm series-damping) resistors in the digital signal lines where appropriate (i.e., if the line is longer than a quarter wavelength of the highest signal frequency of importance, reflections will start causing problems).

The above comments are guidelines only. High frequency board layout is difficult and must be done with care. A bad board layout will reduce the SNR of the transceiver and cause timing problems with the board logic, perhaps to the point of requiring a complete board redesign.



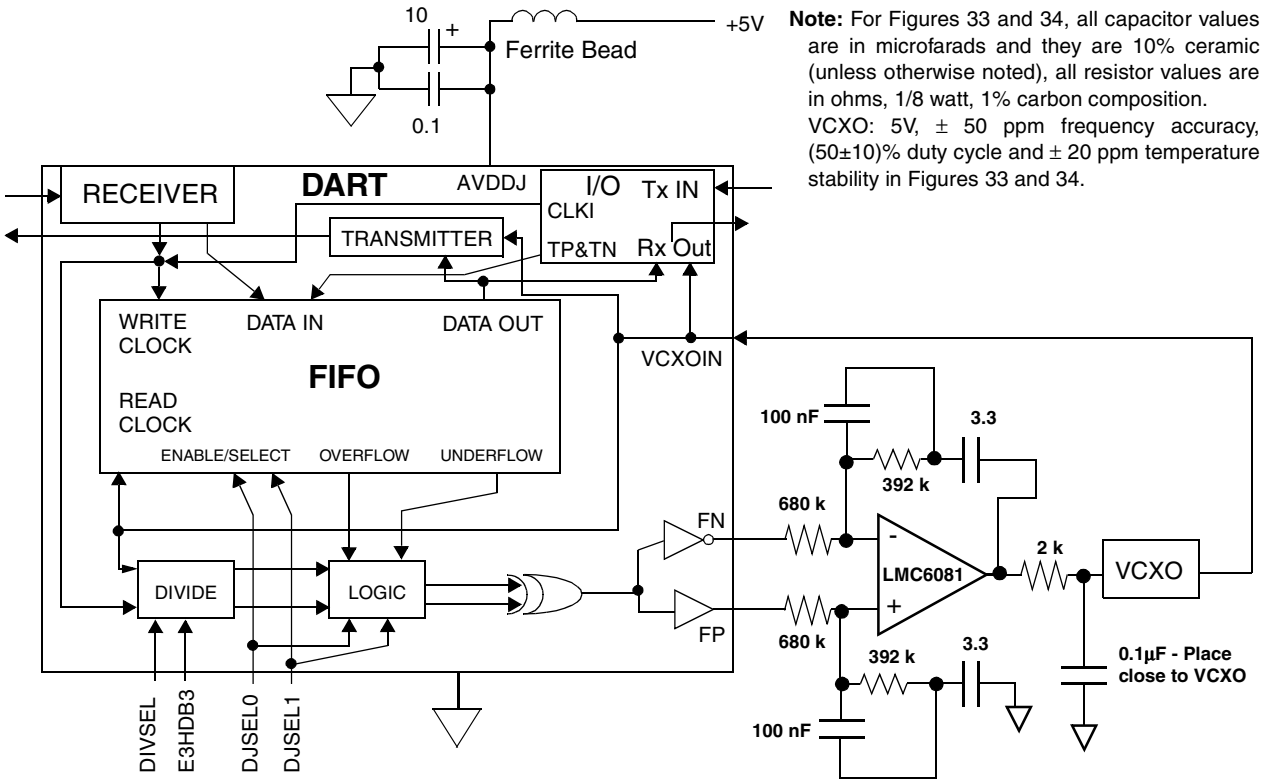
Note: All capacitor values are in microfarads (unless otherwise noted), all resistor values are in ohms. Place components next to their respective pins. See notes following Figure 35.

Figure 31. External Components, Pin Connections and Power/Grounds



Note: All capacitor values are in microfarads and they are 10% ceramic (unless otherwise indicated), all resistor values are in ohms, 1/8 watt, 1% carbon composition. Populate only those output components necessary for the application's signal rate. Components with a DS3 label should be used (installed) for DS3 only. All components not labeled DS3 should be used (installed) for E3 only. The components shown for the +5V supply are used for E3 and DS3.

Figure 32. DART Layout Guidelines for Combined E3/DS3 Board



Note: For Figures 33 and 34, all capacitor values are in microfarads and they are 10% ceramic (unless otherwise noted), all resistor values are in ohms, 1/8 watt, 1% carbon composition.
VCXO: 5V, ± 50 ppm frequency accuracy, (50±10)% duty cycle and ± 20 ppm temperature stability in Figures 33 and 34.

Figure 33. DART VCXO Interface When Using the Dejitter Buffer

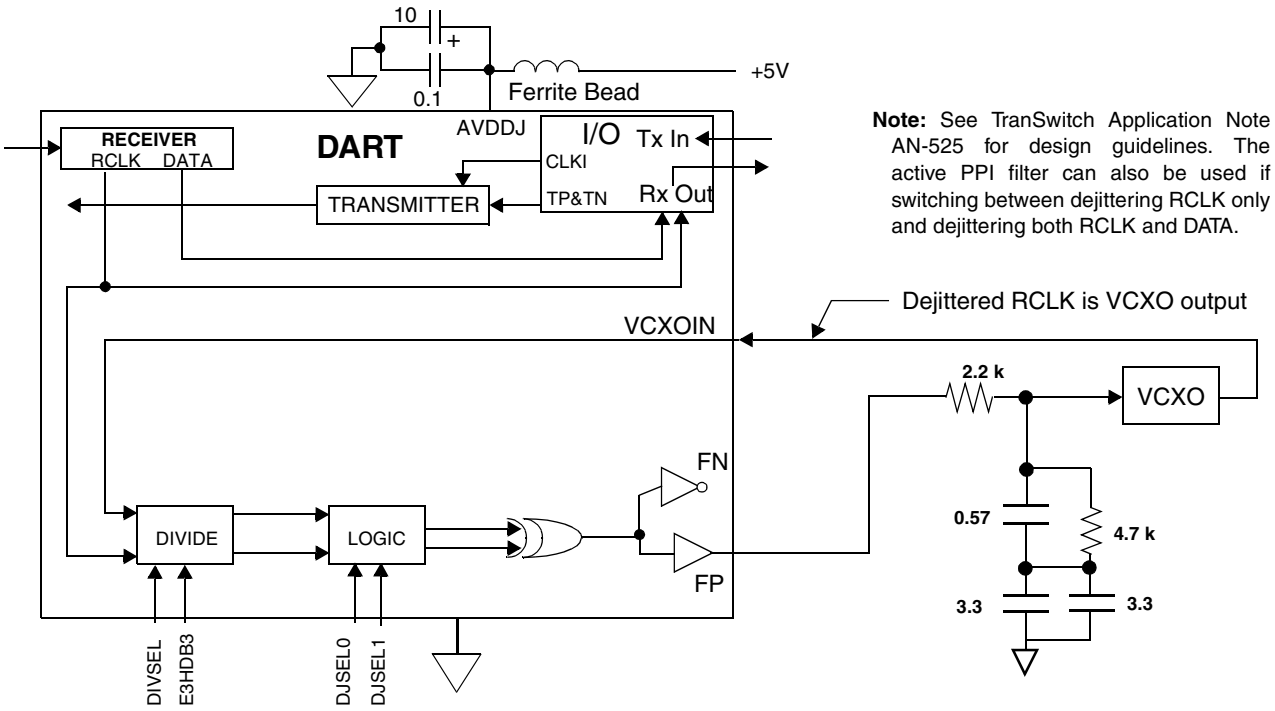


Figure 34. DART VCXO Interface for Dejittering RCLK Only

Table 7. Dejitter PLL Recommended Components

Part	Part Number(s)	Manufacturer/ Suppliers
3.3 µF capacitor, ceramic, 10V, X5R, +/- 10%	ECJ-3YB1A335K PCC1869CT-ND	Panasonic DigiKey
VCXO, 5V DIL	DFV 14-MHR 44.736 M V14112 DFV 14-KHR 34.368 M V14111	Fordhal Fordhal
VCXO, 5V SMD	DFV S1-KHR 44.736 M VS1047 DFV S1-KHR 34.368 M VS1047	Fordhal Fordhal
Low Input Offset Voltage, 5V supply, Op-Amp	LMC6081 or equivalent	National Semiconductor

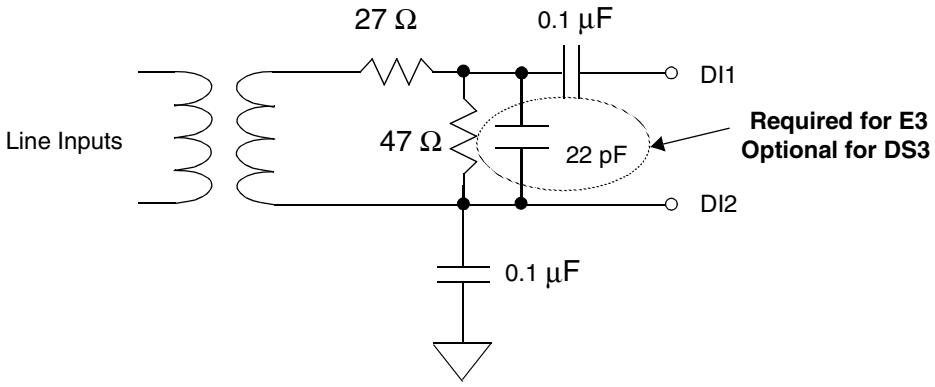


Figure 35. Suggested Single-Ended Termination Circuit for Non-Monitor Functions

Notes:

1. T1 and T2 are either Coilcraft WB1010 or Pulse PE65967 transformers, or equivalent.
2. T3 (for E3 only) is either a Coilcraft WB1020 or a Pulse PE65968 transformer, or equivalent. T3 is only required if the DART square wave transmit output is used (DO1, DO2). It is recommended that the board layout is designed to accommodate both the single-ended and differential layouts (see Figure 32).
3. R5 and R6 are only required for DART eye pattern monitoring purposes, not for device operation.
4. Fair-Rite #2743002111 or equivalent should be used for each ferrite bead.
5. Locate ferrite bead/capacitor decoupling as close as possible to device. Locate the 10 µF polarized capacitor as close as possible to the ferrite bead and place an individual 0.1 µF capacitor as close as possible to each voltage pin on the device.
6. The power supply decoupling as shown is the optimum case. The various DART power supplies can be combined with a slight reduction of SNR for each combination. The SNR loss for each combination is layout dependent and not easily quantified. Under no circumstances should the DART power supplies be tied to the card digital power supply.
7. Power connections for transmit PLL: Avoid traces for power connections if possible. Use a decoupling capacitor. Connect AVDDTPLL, AGNDTPLL (use of a single, solid ground plane with notching is recommended) and TPLLC as follows:

Operating Mode	AVDDTPLL Connection
Receive and Transmit	AVDDTX
Receive Only	AVDDRX
Transmit Only	AVDDTX

8. Use of a single, solid ground plane is recommended. Notching to steer large switching currents away from the ground paths (DART grounds to the card power connector) can be used. Do not route traces with AC signals over notches.
9. Figure 35 is the circuit suggested for future board designs in a non-monitor, non-redundant function. The attenuation circuit will prevent the AGC from operating near the limits of its linear range.

PACKAGE INFORMATION

The DART device is packaged in an 80-pin low profile plastic quad flat package suitable for surface mounting, as illustrated in Figure 36.

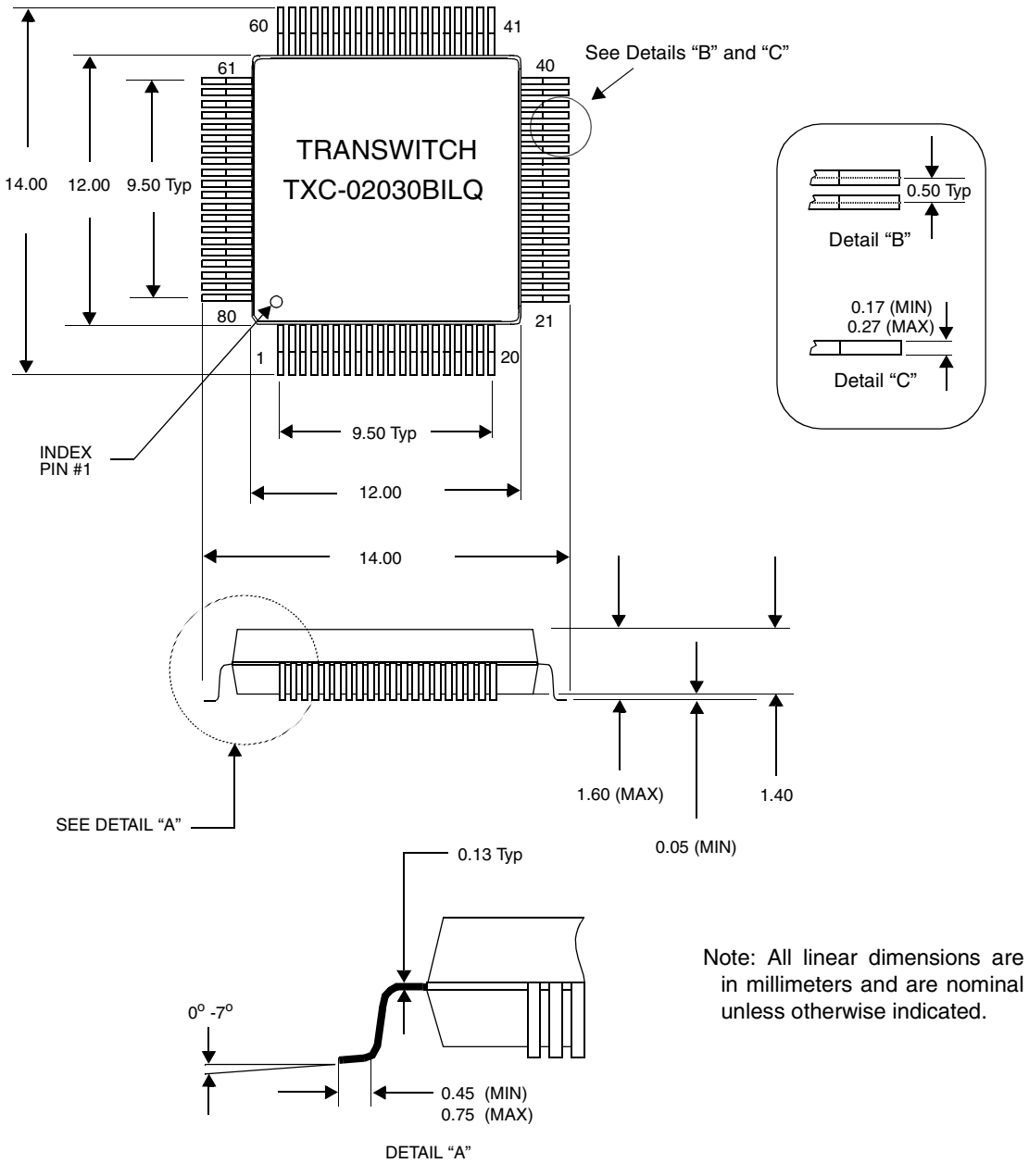


Figure 36. DART TXC-02030 80-Pin Low Profile Plastic Quad Flat Package

ORDERING INFORMATION

Part Number: TXC-02030BILQ 80-pin Low Profile Plastic Quad Flat Package

RELATED PRODUCTS

TXC-02020 (02021), ART (ARTE) VLSI Device (Advanced DS3/STS-1 Receiver/Transmitter). Performs the receive and transmit line interface functions required for transmission of DS3 (44.736 Mbit/s) or STS-1 (51.840 Mbit/s) signals across a coaxial interface. The ARTE is an extended-feature version of the ART, in a larger package.

TXC-02050, MRT Multi-Rate Line Interface VLSI Device. The MRT provides the functions for terminating ITU-specified 8448 kbit/s (E2) and 34368 kbit/s (E3) line rate signals, or 6312 kbit/s (JT2) line signals specified in the Japanese NTT Technical Reference for High Speed Digital Leased Circuits. An optional HDB3 codec is provided for the two ITU line rates.

TXC-03103, QT1F-*Plus* VLSI Device (Quad T1 Framer-*Plus*). A 4-channel framer for voice and data applications. This device handles all logical interfacing functionality to a T1 line. It has extended features relative to the QDS1F device. Requires +5.0 V power supply.

TXC-03108, T1Fx8 VLSI Device (8-Channel T1 Framer). An 8-channel framer for voice and data communications applications. This device handles all logical interfacing functionality to a T1 line and operates from a power supply of 3.3 volts.

TXC-03109, E1Fx8 VLSI Device (8-Channel E1 Framer). An 8-channel framer for voice and data communications applications. This device handles all logical interfacing functionality to an E1 line and operates from a power supply of 3.3 volts.

TXC-03114, QE1F-*Plus* VLSI Device (Quad E1 Framer-*Plus*). The QE1F-*Plus* is a 4-channel E1 (2048 kbit/s) framer designed for voice and data communications applications. A dual unipolar or NRZ line interface is supported with full alarm detection and generation per ITU-T G.703 and operates from a power supply of 3.3 or 5 volts.

TXC-03305, M13X VLSI Device (DS3/DS1 Mux/Demux with Enhanced Features). This single-chip device provides the functions needed to multiplex and demultiplex 28 independent DS1 signals to and from a DS3 signal with either an M13 or C-bit frame format. It includes some enhanced features relative to the M13E TXC-03303 device.

TXC-03361, E123MUX VLSI Device (E1/E2/E3 Mux/Demux). The E123MUX is a CMOS VLSI device that provides the E13 functions needed to multiplex and demultiplex 16 independent E1 signals to and from an E3 signal that conforms to the ITU-T G.751 Recommendation. The E123MUX can also be configured to operate as an E12 or E23 multiplexer and demultiplexer.

TXC-03401B, DS3F VLSI Device (DS3 Framer). Maps broadband payloads into the DS3 frame format. Operates in either the C-bit parity or M13 operating modes.

TXC-03452B, L3M VLSI Device (Level 3 Mapper). Maps a 44.736 Mbit/s DS3 or 34.368 Mbit/s E3 asynchronous line signal into an STM-1/STS-3/STS-1 formatted synchronous signal. Separate add/drop bus timing is available for loop multiplexers. The L3M provides the overhead processing for the mapped signal.

TXC-20153, DS3/STS-1 Line Interface Module (DS3LIM-SN). Complete and compact analog-to-digital interface that converts B3ZS-encoded DS3 or STS-1 line signals to and from NRZ data and clock signals. Packaged as 2.6 inch x 1.0 inch 50-pin DIP.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

2570 West El Camino Real
Suite 304
Mountain View, CA 94040

Tel: 650-949-6700
Fax: 650-949-6705
Web: www.atmforum.org

ATM Forum Europe Office

Av. De Tervueren 402
1150 Brussels
Belgium

Tel: 2 761 66 77
Fax: 2 761 66 79
Web:
www.euroinfo@atmforum.ocm

ATM Forum Asia-Pacific Office

Hamamatsucho Suzuki Building 3F
1-2-11, Hamamatsucho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3438 3694
Fax: 3 3438 3698
Web: www.apinfo@atmforum.com

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
7730 Carondelet Avenue, Suite 407
Clayton, MO 63105-3329

Tel: 800-854-7179 (within U.S.A.)
Tel: 314-726-0444 (outside U.S.A.)
Fax: 314-726-6418
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia Antipolis Cedex
France

Tel: 4 92 94 42 22
Fax: 4 92 94 43 33
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007

Tel: 800-669-6857 (within U.S.A.)
Tel: 903-769-3717 (outside U.S.A.)
Fax: 508-650-1375
Web: www.mvip.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5111
Fax: 22 733 7256
Web: www.itu.int

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: 215-697-2179
Fax: 215-697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
2575 NE Kathryn Street #17
Hillsboro, OR 97124

Tel: 800-433-5177 (within U.S.A.)
Tel: 503-693-6232 (outside U.S.A.)
Fax: 503-693-8344
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (within U.S.A.)
Tel: 908-699-5800 (outside U.S.A.)
Fax: 908-336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated DART Data Sheet that have significant differences relative to the previous and now superseded DART Data Sheet:

Updated DART Data Sheet: *PRELIMINARY* Ed. 2A, April 2000

Previous DART Data Sheet: *PRELIMINARY* Ed. 2, March 2000

The page numbers indicated below of this updated data sheet (**in bold font**) include changes relative to the superseded data sheet. The other page numbers indicated below of this updated data sheet are the changes relative to the Edition 1, June 1999 data sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	**Changed edition number and date.**
All	Changed *PRODUCT PREVIEW* document status markings to *PRELIMINARY* (and associated explanatory text on pages 1 and 59).
All	Removed all occurrences of “STS-1” and associated text that described the DART STS-1 functionality from the content of the document, except in descriptions of related products.
1	Added last sentence to description.
1, 4, 52, 53	Added “plastic” to description of package type
2-4	Updated Table of Contents, List of Tables and List of Figures.
5, 7	Removed $\overline{\text{PQUAL}}$ from diagrams for Figures 1 and 2.
8	Changed $\overline{\text{STS1}}$ to $\overline{\text{TEST2}}$ in diagram for Figure 3.
9	Changed second paragraph of Adaptive Equalizer/AGC section. Changed “The CV is 9...” to “The CV is approximately 9...” in the paragraph for B3ZS/HDB3 Decoder section.
10	Changed third paragraph of LOS Detector section. Changed number 3 of Tx I/O Control section.
11	Added last sentence to first paragraph for DS3 Shaped Output section.
13	Changed first paragraph on page. Changed first paragraph for $2^{15}/2^{23}$ - 1 PRBS Analyzer section. Changed last two sentences of paragraph for Input Reference Clock section. Changed paragraph for Dejitter FIFO/Dejitter PLL Operation section.
14	Changed first and third paragraphs. Removed Line Loopback from diagram for Figure 4.
16, 17	Added Receive block and Symbol DOUT to diagrams for Figures 8 and 9.
17, 18	Added Symbol DOUT to diagrams for Figures 10 and 11.
19, 20	Added Figures 12 and 13, and associated text. Renumbered all succeeding Figures.
21	Changed Symbol names for pins 3 and 59 in diagram for Figure 14.
22	Changed Name/Function for Symbol AVDDJ.

Page Number of Updated Data Sheet	Summary of the Change
23	Added last sentence to Name/Function for Symbols $\overline{EXZ}$, CV, $\overline{DLOS}$ and $\overline{ALOS}$.
24	Added "See Figure 31" to Name/Function for Symbols RCPLL and $\overline{TEST3}$. Changed Symbol name for Pin No. 3 from $\overline{PQUAL}$ to $\overline{TEST3}$ and changed Name/Function.
25	Changed Name/Function for Symbol $\overline{ZERO}$. Changed Symbol name for Pin No. 59 from $\overline{STS1}$ to $\overline{TEST2}$ and changed Name/Function.
26	Changed Name/Function for Symbol EQSEL.
27	Changed Name/Function for Symbol VCXOIN.
28	Clarified ESD Classification in first table and added Note 3.
32	Changed Min and Max values in both tables for Symbol t_{OD}.
33	Changed Min in first table for Symbol t_{SU}. Changed Min and Max in second table for Symbol t_{OD}.
34	Changed Min and Max in first table for Symbol t_{OD}. Added Figure 23. Renumbered all succeeding figures.
34	**Changed Min and Max in second table for Symbol t_{OD}.**
38	Extensively changed Transmitter Line Side Output Specifications table.
43	Changed second paragraph.
45	Changed list of power regions (middle of page).
46	Added two sentences about guard traces to middle of second paragraph.
47	Changed diagram (several changes) for Figure 31.
48	Changed diagram (added 1.2 k resistor) for Figure 32.
49	Removed last sentence of Note.
49, 50	Changed component values and removed AGNDDJ labels from diagrams for Figures 33 and 34.
50	Added Table 7.
51	Changed diagram (22 pF) for Figure 35. Changed Note 9.
53	Updated Related Products.
54-55	Updated Standards Documentation Sources.
56-57	**Updated List of Data Sheet Changes.**

- NOTES -

- NOTES -

TranSwitch Corporation • 3 Enterprise Drive • Shelton, CT 06484 USA • Tel: 203-929-8810 • Fax: 203-926-9453 • www.transwitch.com

DOCUMENTATION UPDATE REGISTRATION FORM

If you would like to receive updated documentation for selected devices as it becomes available, please provide the information requested below (print clearly or type) then tear out this page, fold and mail it to the Marketing Communications Department at TranSwitch. Marketing Communications will ensure that the relevant Product Information Sheets, Data Sheets, Application Notes, Technical Bulletins and other publications are sent to you. You may also choose to provide the same information by fax **(203.926.9453)**, or by e-mail **(info@txc.com)**, or by telephone **(203.929.8810)**. Most of these documents will also be made immediately available for direct download as Adobe PDF files from the TranSwitch World Wide Web Site (**www.transwitch.com**).

Name: _____

Company: _____ Title: _____

Dept./Mailstop: _____

Street: _____

City/State/Zip: _____

If located outside U.S.A., please add - Country: _____ Postal Code: _____

Telephone: _____ Ext.: _____ Fax: _____

E-mail: _____

Please provide the following details for the managers in charge of the following departments at your company location.

Department	Title	Name
Company/Division	_____	_____
Engineering	_____	_____
Marketing	_____	_____

Please describe briefly your intended application(s) and indicate whether you would like to have a TranSwitch applications engineer contact you to provide further assistance:

_____

_____

_____

_____

If you are also interested in receiving updated documentation for other TranSwitch device types, please list them below rather than submitting separate registration forms:

_____ _____ _____ _____ _____ _____ _____

_____ _____ _____ _____ _____ _____ _____

Please fold, tape and mail this page (see other side) or fax it to Marketing Communications at 203.926.9453.

TRANSWITCH®

Engines for Global Connectivity

(Fold back on this line second, then tape closed, stamp and mail.)

TRANSWITCH

3 Enterprise Drive
Shelton, CT 06484-4694
U.S.A.

First
Class
Postage
Required

TranSwitch Corporation

Attention: Marketing Communications Dept.
3 Enterprise Drive
Shelton, CT 06484-4694
U.S.A.

(Fold back on this line first.)

Please complete the registration form on this back cover sheet, and fax or mail it, if you wish to receive updated documentation on this TranSwitch product as it becomes available.