MIL-STD-1553 DUAL REDUNDANT REMOTE TERMINAL HYBRID

DESCRIPTION

The BUS-65142 Series is a complete dual redundant MIL-STD-1553 Remote Terminal Unit (RTU) packaged in a small 1.9" x 2.1" hybrid. The device is based upon two DDC custom ICs, which includes two monolithic bi-polar low power transceivers and one CMOS protocol containing data buffers and timing control logic. It supports all 13 mode codes for dual redundant operation, any combinaion of which can be illegalized.

Parallel data transfers are accomplished with a DMA type handshaking, compatible with most CPU types. Data transfers to/from memory are simplified by the latched command word and word count outputs.

Error detection and recovery are enhanced by BUS-65142 Series special features. A 14-bit built-in-test word register stores RTU information, and sends it to the Bus Controller in response to the Mode Command Transmit Bit Word. The BUS-65142 Series performs continuous on-line wraparound self-test, and provides four error flags to the host CPU. Inputs are provided for host CPU control of 6 bits of the RTU Status Word.

Its small hermetic package, -55°C to +125°C operating temperature range, and complete RTU operation make the BUS-65142 ideal for most MIL-STD-1553 applications requiring hardware or microprocessor subsystems.

FEATURES

- ***Complete Intergrated Remote Terminal Including:***
  - ***–Dual Low-Power Transceivers***
  - ***–Complete RT Protocol***
- ***Direct Interface to Systems With No Processor***
- ***Radiation Tolerant Version Available***
- ***Space Qualified Version Available***
- ***High Reliability Screening Available***

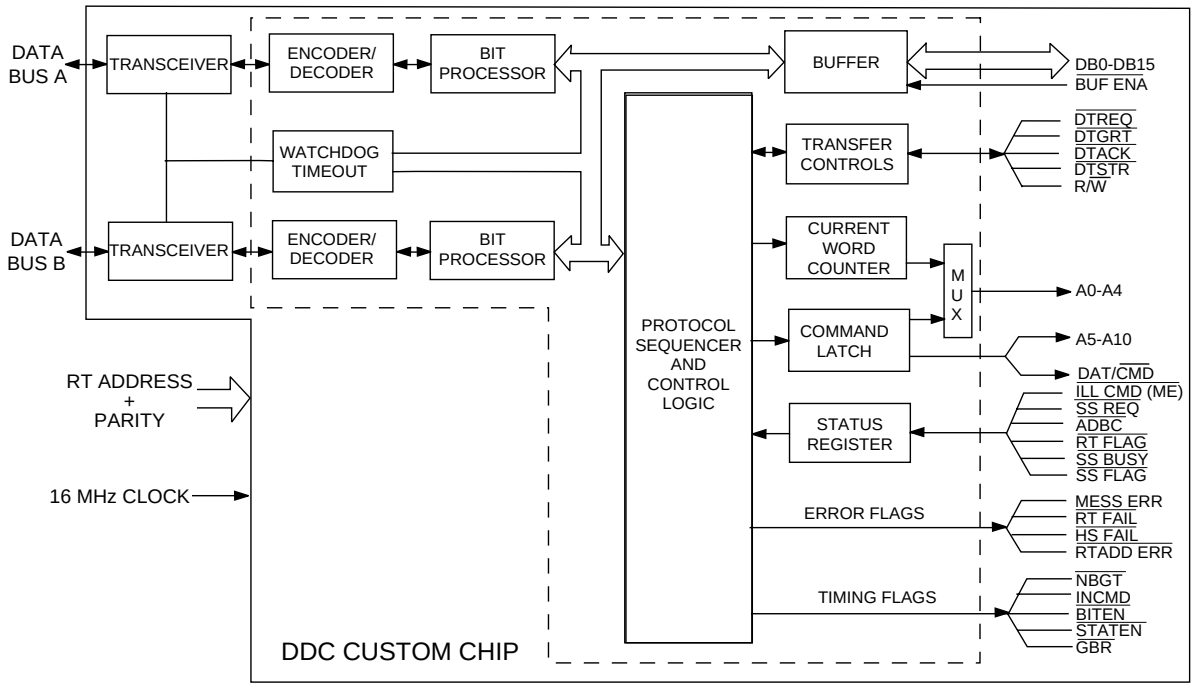


FIGURE 1. BUS-65142 SERIES BLOCK DIAGRAM

TABLE 1. BU-65142 and BUS-65142/44 SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
RECEIVER				
Differential Input Impedance (DC to 1 MHz)	4.0			kohm
Differential Input Voltage			40	Vp-p
Input Threshold Level (Direct Coupled)	0.70		1.20	Vp-p
CMRR (DC to 2 MHz)	40			dB
CMV (DC to 2 MHz)	±10			V
TRANSMITTER				
Differential Output Voltage				
■ Direct Coupled Across 35 Ω, Measured on Bus	6	7	9	Vp-p
■ Transformer Coupled Across 70 Ω, Measured on Stub:	18	21	27	Vp-p
Output Noise, Differential (Direct Coupled)			10	mVp-p, diff
Output Offset Voltage, (Transformer Coupled Across 70 ohms)	-250		+250	mVp-p, diff
Rise/Fall Time	100	150	300	nsec
LOGIC				
V_{IH}	2.4			V
V_{IL}			0.7	V
IIH (V_{IH}=2.7V)				
■ BRO ENA, ADDRE-ADDRA(RTAD4-RTAD0), ADDRP (connect to 30kΩ pull-up)	0.04		0.2	mA
■ (V_{IH}=2.7V) DB15 - DB0 (connect to a 45kΩ pull-up)	0.04		0.2	mA
■ (VIH≥2.4V) All Other Inputs			±20	µA
I_{IL} (V_{IL}=0.4V)				
■ BRO ENA, ADDRE-ADDRA(RTAD4-RTAD0), ADDRP (connect to 30kΩ pull-up)			0.4	mA
■ (V_{IL}=0.4V) DB15 - DB0 (connect to a 45kΩ pull-up)			0.4	mA
■ (V_{IL}=≥0.7V) All Other Inputs---			±20	µA
V_{OH}				
■(I_{OH}=-0.4mA) A9-A5(SA4-SA0), RTADERR, HSFAIL, DAT/CMD, RTFAIL, BITEN, NBGT, GBR, ME, STATEN	2.4			V
V_{OH}				
■ (I_{OH}=-0.4mA) All Other Inputs---	2.4			V
V_{OH}				
■ (I_{OH}=-0.4mA) DB15 - DB0 (connect to a 45kΩ pull-up)	2.4			V
V_{OL}				
■(I_{OH}=-2mA) A9-A5(SA4-SA0), RTADERR, HSFAIL, DAT/CMD, RTFAIL, BITEN, NBGT, GBR, ME, STATEN			0.4	V
V_{OH}				
■(I_{OL}=2 mA) All Other Inputs---			0.4	V

TABLE 1. BU-65142 and BUS-65142/44 SPECIFICATIONS (continued)

PARAMETER	MIN	TYP	MAX	UNITS
LOGIC (continued)				
VOH				
■ (I_{OH}=-2mA) DB15 - DB0 (connect to a 45kΩ pull-up)			0.4	V
C_1 (f = 1 MHz)			50	pF
C_0 (f = 1 MHz)		10		pF
C_{I0} ((f = 1 MHz)			50	pF
■ DB15 - DB0 (connect to a 45kΩ pull-up)				
POWER SUPPLY REQUIREMENTS				
+5V (BU-65142X1/2, BUS-65142/43/44/45)	4.5		5.5	V
Current Drain		50	115	mA
-15V (BU-65142X1, BUS-65142/44)	-15.75		-14.25	V
Current Drain				
• Idle		30	60	mA
• 25% Transmitter Duty Cycle		68	108	mA
• 50% Transmitter Duty Cycle		105	160	mA
• 100% Transmitter Duty Cycle		180	255	mA
-12V (BU-65142X2, BUS-65143/45)	-12.6		-11.4	V
Current Drain				
• Idle		30	60	mA
• 25% Transmitter Duty Cycle		80	120	mA
• 50% Transmitter Duty Cycle		130	185	mA
• 100% Transmitter Duty Cycle		230	305	mA
POWER DISSIPATION (See Note)				
Total Hybrid				
■ BU-65142X1/BUS-65142/44				
• Idle		0.700	1.475	W
• 25% Transmitter Duty Cycle		0.912	1.856	W
• 50% Transmitter Duty Cycle		1.125	2.238	W
• 100% Transmitter Duty Cycle		1.550	3.000	W
■ BU-65142X2/BUS-65143/45				
• Idle		0.610	1.295	W
• 25% Transmitter Duty Cycle		0.860	1.680	W
• 50% Transmitter Duty Cycle		1.110	2.065	W
• 100% Transmitter Duty Cycle		1.160	2.895	W
Hottest Die				
■ BU-65142X1/BUS-65142/44				
• Idle		0.335	0.680	W
• 25% Transmitter Duty Cycle		0.550	1.010	W
• 50% Transmitter Duty Cycle		0.760	1.350	W
• 100% Transmitter Duty Cycle		1.185	2.030	W
■ BU-65142X2/BUS-65143/45				
• Idle		0.290	0.590	W
• 25% Transmitter Duty Cycle		0.540	0.870	W
• 50% Transmitter Duty Cycle		0.790	1.260	W
• 100% Transmitter Duty Cycle		1.290	1.960	W

TABLE 1. BU-65142 and BUS-65142/44 SPECIFICATIONS (continued)				
THERMAL				
• Thermal Resistance, Junction-to-Case, Hottest Die (θJC)			20	°C/W
• Operating Junction Temperature	-55		150	°C
• Storage Temperature	-65		150	°C
• Lead Temperature (soldering, 10 sec.)			+300	°C
PHYSICAL CHARACTERISTICS				
Size				
78-pin Kovar (BUS-65142/43)	1.87 x 2.10 x 0.25 (47.5 x 53.3 x 6.4)			in (mm)
82-pin Kovar Flat Pack (BUS-65142/43)	1.61 x 2.20 x 0.181 (40.8 x 55.8 x 4.6)			in (mm)
78-pin Ceramic QIP (BU-65142D)	1.80 x 2.10 x 0.21 (45.7 x 53.3 x 5.3)			in (mm)
78-pin Ceramic Flat Pack (BU-65142F)	1.80 x 2.10 x 0.21 (45.7 x 53.3 x 5.3)			in (mm)
Weight	1.7 (4.1)			oz (g)

Note:

Power dissipation specifications assume a transformer coupled configuration, with external disipation (while transmitting) of 0.14 watts for the active isolation transformer, 0.8 watts for the active coupling transformer, 0.45 watts for each of the two bus isolation resistors, and 0.15 watts for each of the two bus termination resistors.

TABLE 2. BU-65142 SERIES RADIATION SPECIFICATIONS			
PART NUMBER	**TOTAL DOSE**	**SINGLE EVENT UPSET**	**SINGLE EVENT LATCHUP**
BU-65142 X1/X2	300K Rad	5.3×10^{-6} errors/device-day, (LET Threshold of 59 MeV/mg/cm^2)	Immune

INTRODUCTION

The BUS-65142 is a complete dual redundant Remote Terminal Unit (RTU) packaged in a small 1.9 x 2.1 hybrid. It is fully compliant with MIL-STD=1553B and supports all message formats. As shown in FIGURE 1, it includes 2 transceivers and a custom chip containing 2 encoders, 2 bit processors, an RTU protocol sequencer and control logic, output latches, and buffers. With the addition of 2 data bus transformers, the BUS-65142 is ready for connection to a MIL-STD-1553 data bus.

Data is transferred to and from the subsystem host CPU over a 16-bit parallel highway, which is isolated by a set of bi-directional buffers. All transfers are made with a DMA type handshake sequence of request, grant and acknowledge. Read/write and data strobes are provided to simplify interfacing to external RAM. Also simplifying the RAM interface is the availability of latched command word and auto-incrementing word counter. These signals may be used as an address to map the data directly to and from RAM.

The BUS-65142 allows the subsystem host CPU to control 6 of the bits in the RTU status word. Of particular interest is the Illegal Command input which may be used to set the message error bit and illegalize any command word. The BUS-65142 provides four error flags to the subsystem host CPU for evaluating its condition. In addition a continuous on-line self-test is performed by the BUS-65142 on every transmission. The last Transmitted Word of every message is wrapped around the decoder and compared with the Actual Word. Any discrepancy is flagged as an error.

TIMING

Interfacing the subsystem host CPU to the BUS-65142 is simple and compatible with most microprocessors. FIGURE 3 and 4 illustrate typical MIL-STD-1553 messages for Transmit data and Receive data. FIGURES 5 and 6 illustrate RT to RT transfers. In each case $\overline{\text{NBGT}}$ identifies the start of the message, and INCMD identifies that a command is being processed. The handshake sequence $\overline{\text{DTREQ}}$, $\overline{\text{DTGRT}}$, and $\overline{\text{DTACK}}$ is used to transfeer each word over the parallel data highway. $\overline{\text{DTSRB}}$ and RD/$\overline{\text{WR}}$ are used to control transfers to RAM memory. $\overline{\text{GBR}}$ identifies a “good block received”, when a received message has passed all validation checks and has the correct word count. $\overline{\text{BUFENA}}$ (Buffer Enable) must be applied to enable the internal tri-state buffers.

ERROR FLAGS

Four error flags are ouput to the subsystem to provide information on the condition of the BUS-65142.

The $\overline{\text{ME}}$ (Message Error) line goes LOW if any of the following error conditions exist:
format error
word count error
invalid word
sync error
RT to RT address error
T/R bit error.

The $\overline{\text{RTFAIL}}$ (Remote Terminal Failure) line goes LOW whenever the results of a continuous wraparound self-test shows a discrepancy, or a transmitter watchdog timeout has occurred.

The $\overline{\text{HSFAIL}}$ (Handshake Failure) line goes LOW whenever the system dows not issue a $\overline{\text{DTGRT}}$ in response to a $\overline{\text{DTREQ}}$ before timing-out.

The $\overline{\text{RTADR ERR}}$ (RT Address Error) line goes LOW whenever the sum of the 5 address lines and parity lines show a parity error (the terminal will not respond to commands while this error condition exists).

STATUS REGISTER

Six inputs to the BUS-65142 allow the subsystem host CPU to control bits in the RTU status word. The Illegal Command input may be used to set the Message Error bit in the Status Word and suppress the transmission of data to the bus controller. This line allows illegalization of any combination of commands. The latched Command Word may be connected to the address pins of an optional external PROM, which would drive the Illegal Command line LOW when it identifies a command programmed as illegal.

STATUS REGISTER BIT ASSIGNMENTS

The $\overline{\text{SRO}}$ (Subsystem Request) line is used to set the Status Word service request bit.

The $\overline{\text{ADBC}}$ (Accept Dynamic Bus Control) line is used to set the Status Word bus control bit.

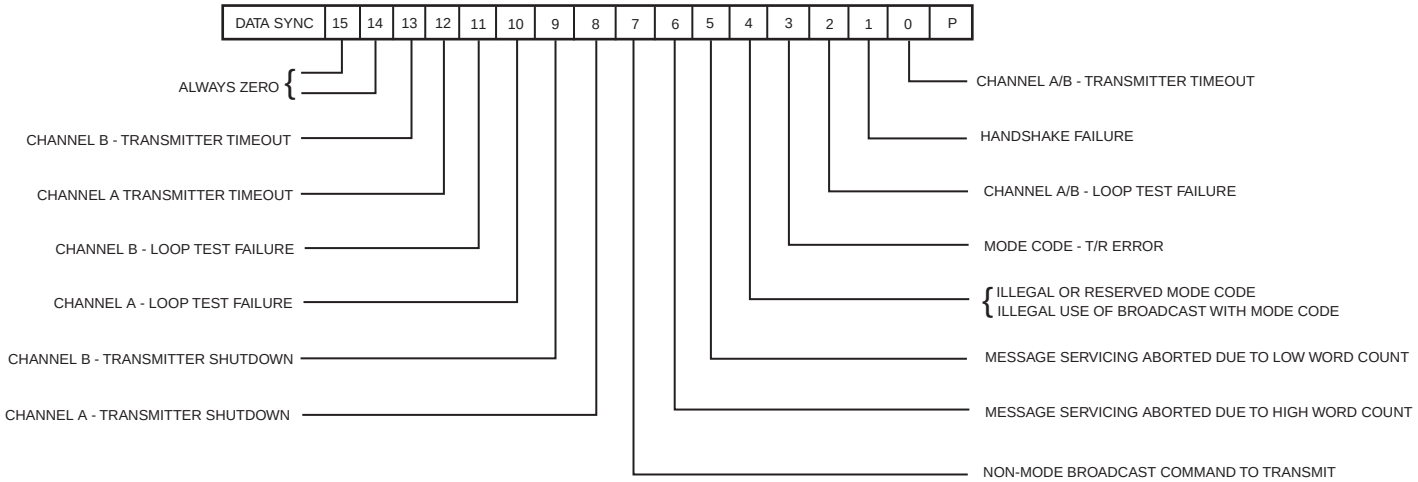
The $\overline{\text{RTFLAG}}$ (RT Flag Line) is used to set the Status Word terminal flag bit.

The $\overline{\text{BUSY}}$ (Busy) line is used to set the Status Word busy bit, and inhibit subsystem requests for data.

The $\overline{\text{SSFLAG}}$ (SubSystem Flag) line is used to set the Status Word subsytem (fault) flag.

BUILT-IN-TEST

The BUS-65142 contains a 14-bit Built-In-Test (BIT) word register which stores information about the condition of the RTU. When a mode code is received to transmit the BIT word, the contents of the BIT register is transmitted over the 1553 bus. FIGURE 2 shows the fault assigned to each bit in the BIT word. Conditions monitored are; transmitter timeouts, loop test failures, transmitter shutdown, subsystem handshake failure, and the results of individual message validations.



NOTES

1. BITS 3-7 ARE CLEARED IN THE BEGINNING OF EACH NEW MESSAGE AND UPDATED AT THE END OF THE MESSAGE. THEY ONLY REFLECT THE PRESENT COMMAND WORD.
2. BITS 0-2 AND 10-13 ARE LATCHED AND ONLY CLEARED BY A MODE RESET COMMAND OR A MASTER RESET ($\overline{\text{RESET}}$).
3. BITS 8 AND 9 ARE SET ONLY BY THE MODE COMMAND FOR "TRANSMITTER SHUTDOWN" AND ARE CLEARED BY THE $\underline{\text{MODE}}$ COMMAND FOR "OVERRIDE TRANSMITTER SHUTDOWN" OR "RESET REMOTE TERMINAL". BITS 8 AND 9 ARE ALSO CLEARED BY $\overline{\text{RESET}}$.

FIGURE 2. BUILT-IN-TEST (BIT) WORD REGISTER

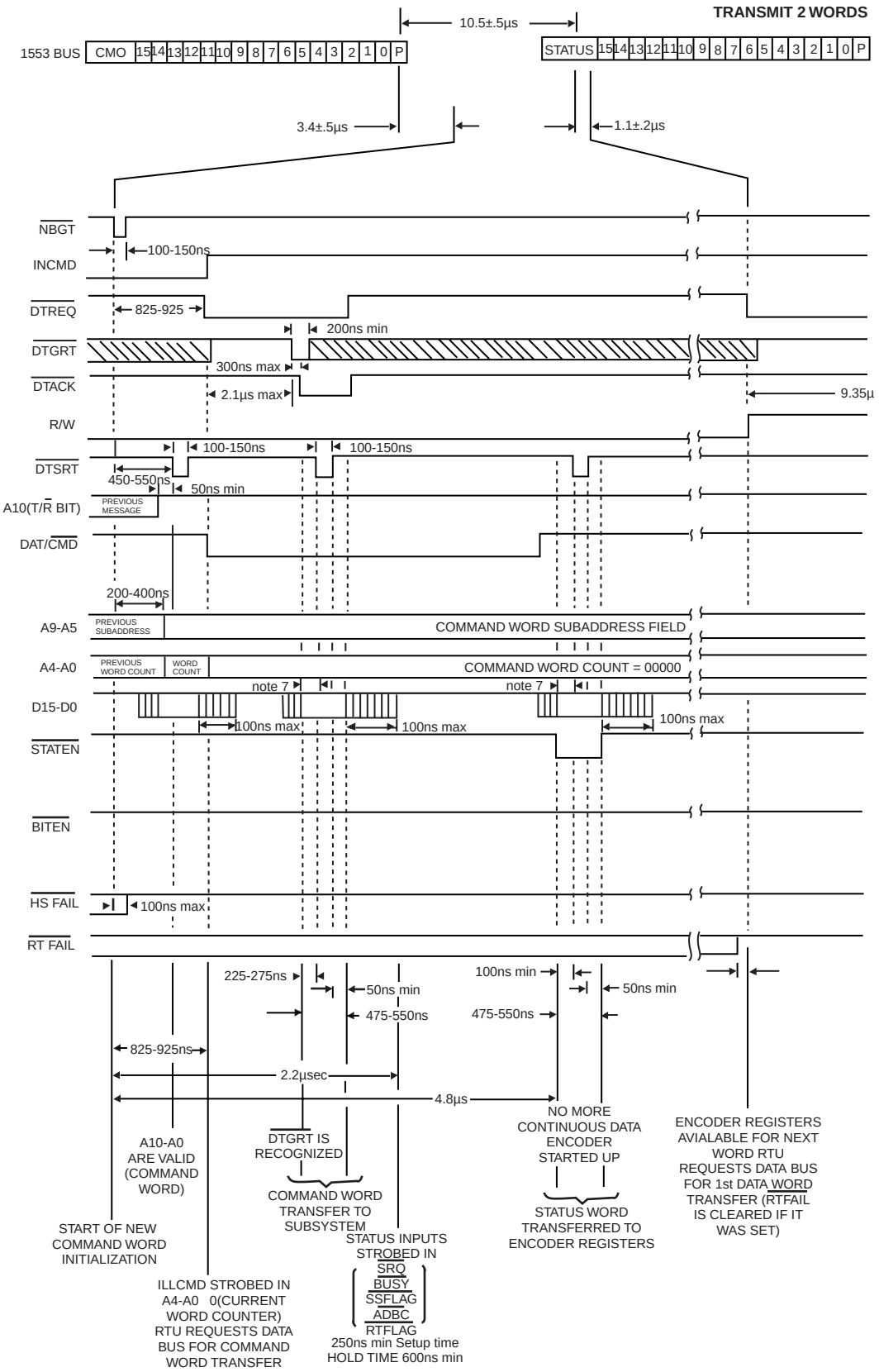
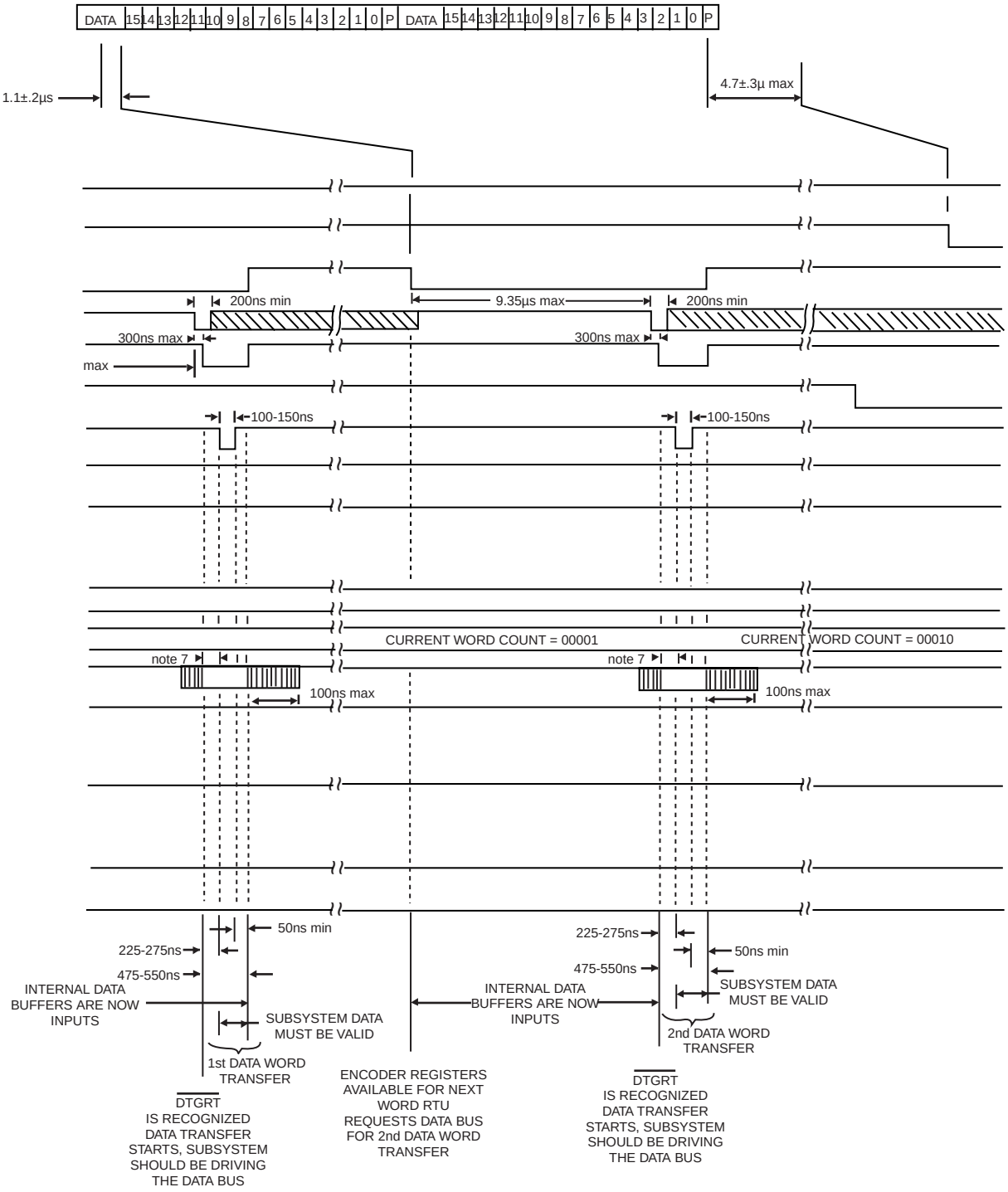


FIGURE 3. TRANSMIT TIMING DIAGRAM



NOTES

1. LEGEND
   - DON'T CARE
   - DATA BUS UNDEFINED
2. EACH WORD IS DRIVEN FOR ≅ 18-19µS ON D15-D05.
   IF BUF ENA IS ACTIVE THE LAST WORD IS AVAILABLE FOR 3.5-4µS SINCE THE STATUS WORD MUST BE SUPPORTED.
3. DATA BUS IS SHOWN WITH BUF ENA CONNECTED TO DTACK (SEE PIN FUNCTION TABLE, PIN 67)
4. THE POSITION OF DTACK WILL VARY DEPENDING ON WHEN DTGRT IS ISSUED; THE TIME WILL BE 100nS MIN to 150ns MAX FROM DTGRT.
5. HSFAIL IS ASSERTED UPON EXCESS DTGRT RESPONSE TIME.
   INCMD WILL SUBSEQUENTLY GO LOW, AND NO FURTHER DATA TRANSFERS WILL OCCUR.
6. RTFAIL IS CLEARED WHEN THE STATUS WORD IS TRANSMITTED. ONCE SET, FLAG WILL REMAIN SET FOR THE ENTIRE MESSAGE.
   THE INCMD FALLING EDGE CAN BE USED TO LATCH RTFAIL STATUS.
7. 100nS MIN REPRESENTS SETUP TIME FOR VALID DATA BEFORE DTSTR GOES LOW FOR A WRITE CYCLE.
   A READ CYCLE REQUIRES VALID DATA 160 nS MAX AFTER DTACK GOES LOW

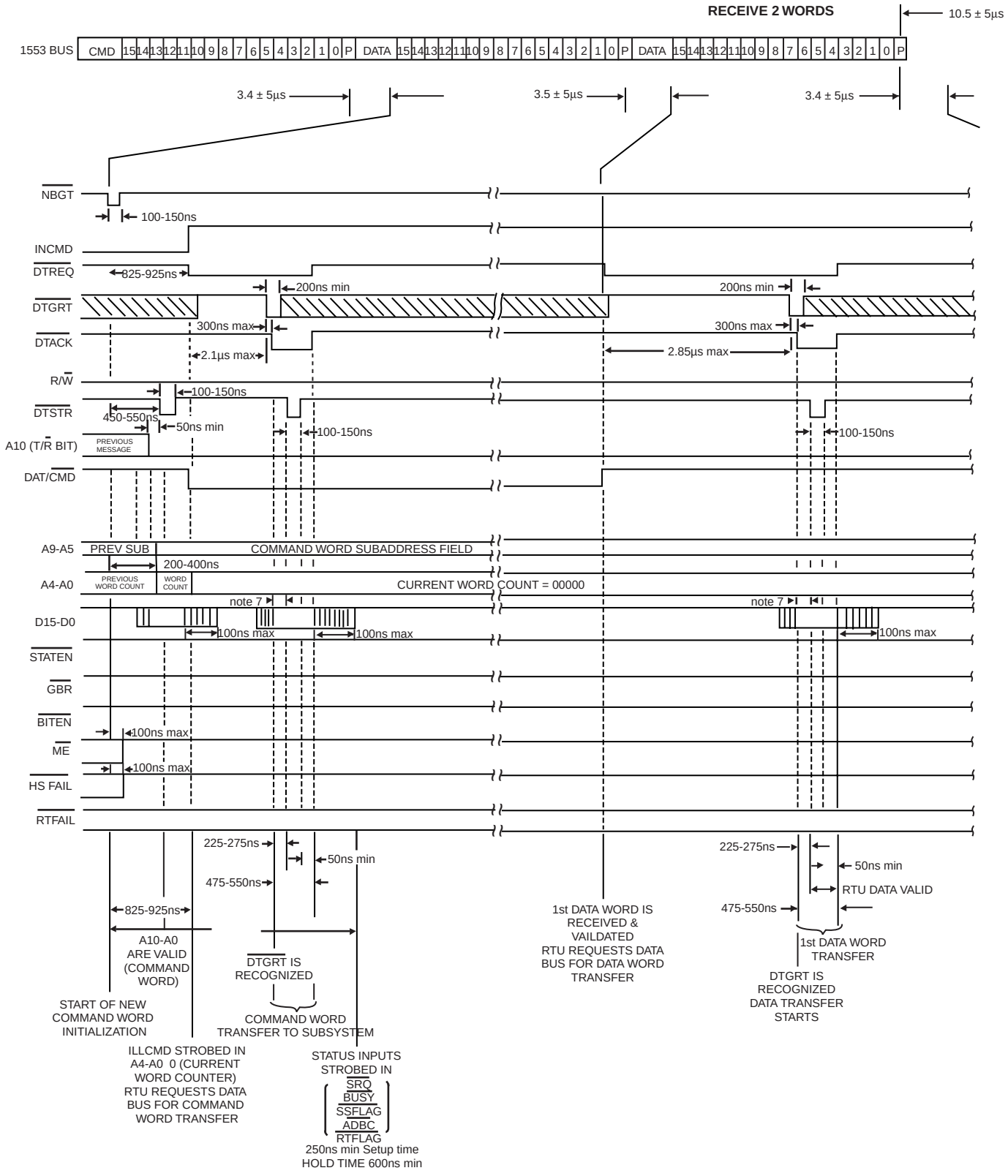
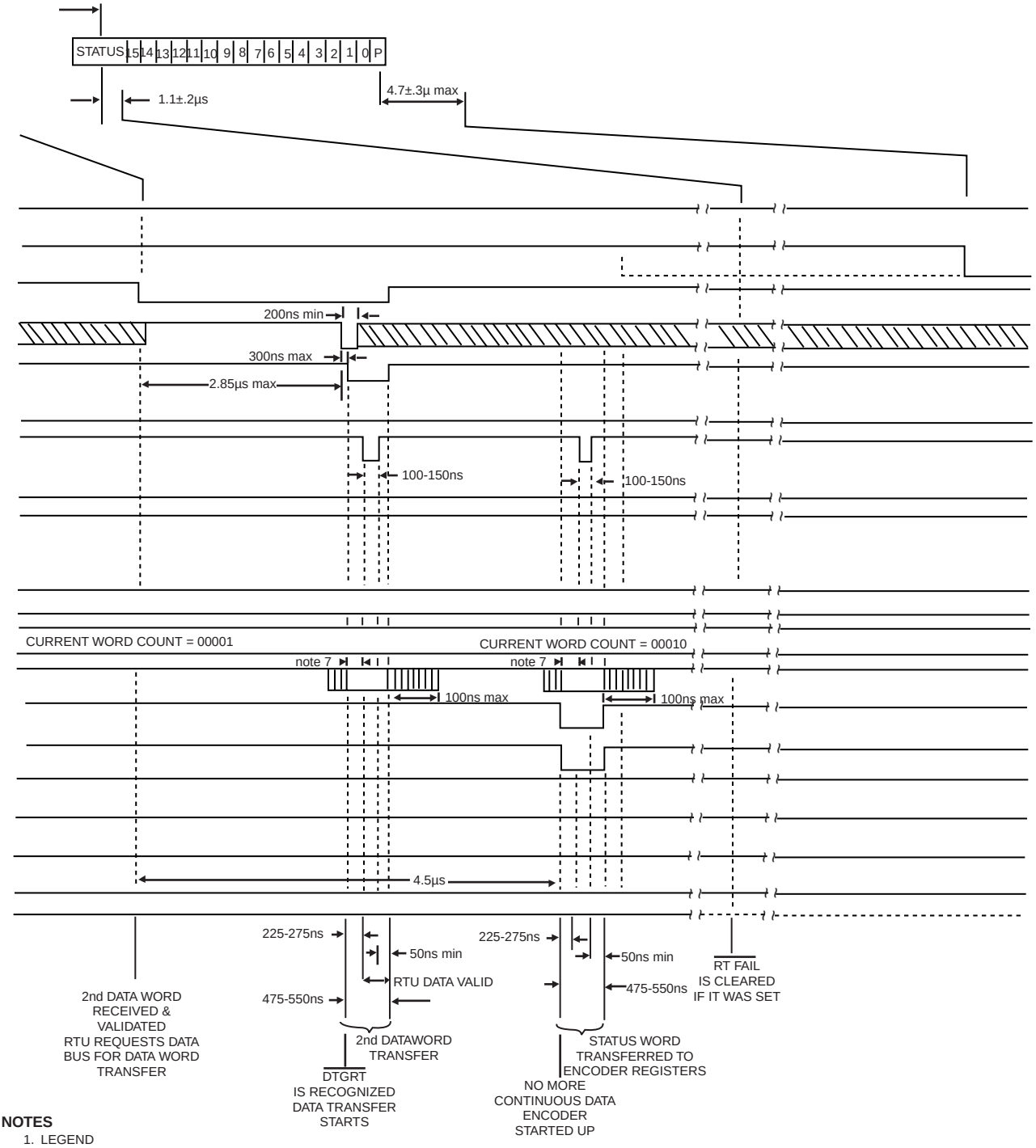


FIGURE 4. RECEIVE TIMING DIAGRAM



NOTES

1. LEGEND
   - DON'T CARE
   - DATA BUS UNDEFINED
   - REPRESENTS THE SEQUENCE OF EVENTS IF THE COMMAND WAS BROADCAST. NOTE: NO STATUS WOULD BE TRANSMITTED ON1553 BUS.
2. EACH WORD IS DRIVEN FOR ≅ 18-19µS ON D15-D0. IF BUF ENA IS ACTIVE THE LAST WORD IS AVAILABLE FOR 3.5-4µS SINCE THE STATUS WORD MUST BE SUPPORTED.
3. DATA BUS IS SHOWN WITH BUF ENA CONNECTED TO DTACK (SEE PIN FUNCTION TABLE, PIN 67)
4. THE POSITION OF DTACK WILL VARY DEPENDING ON WHEN DTGRT IS ISSUED; THE TIME WILL BE 100NS MIN TO 150ns MAX FROM DTREQ
5. HSFAIL IS ASSERTED UPON EXCESS DTGRT RESPONSE TIME. GBR WILL NOT BE SET.
6. RTFAIL IS CLEARED WHEN THE STATUS WORD IS TRANSMITTED. ONCE SET, FLAG WILL REMAIN SET FOR THE ENTIRE MESSAGE. THE INCMD FALLING EDGE CAN BE USED TO LATCH RTFAIL STATUS.
7. 100nS MIN REPRESENTS SETUP TIME FOR VALID DATA BEFORE DTSTR GOES LOW.

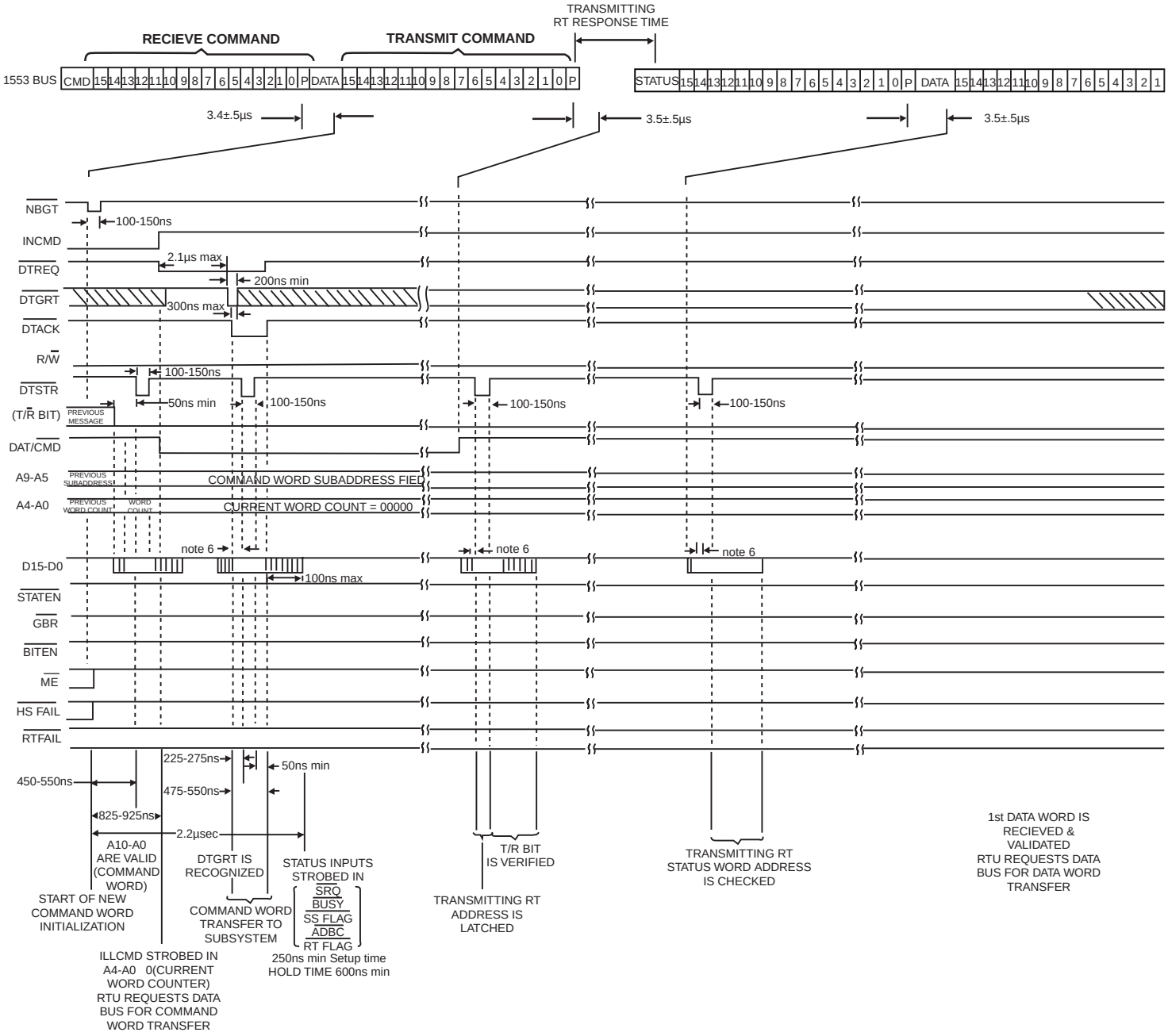
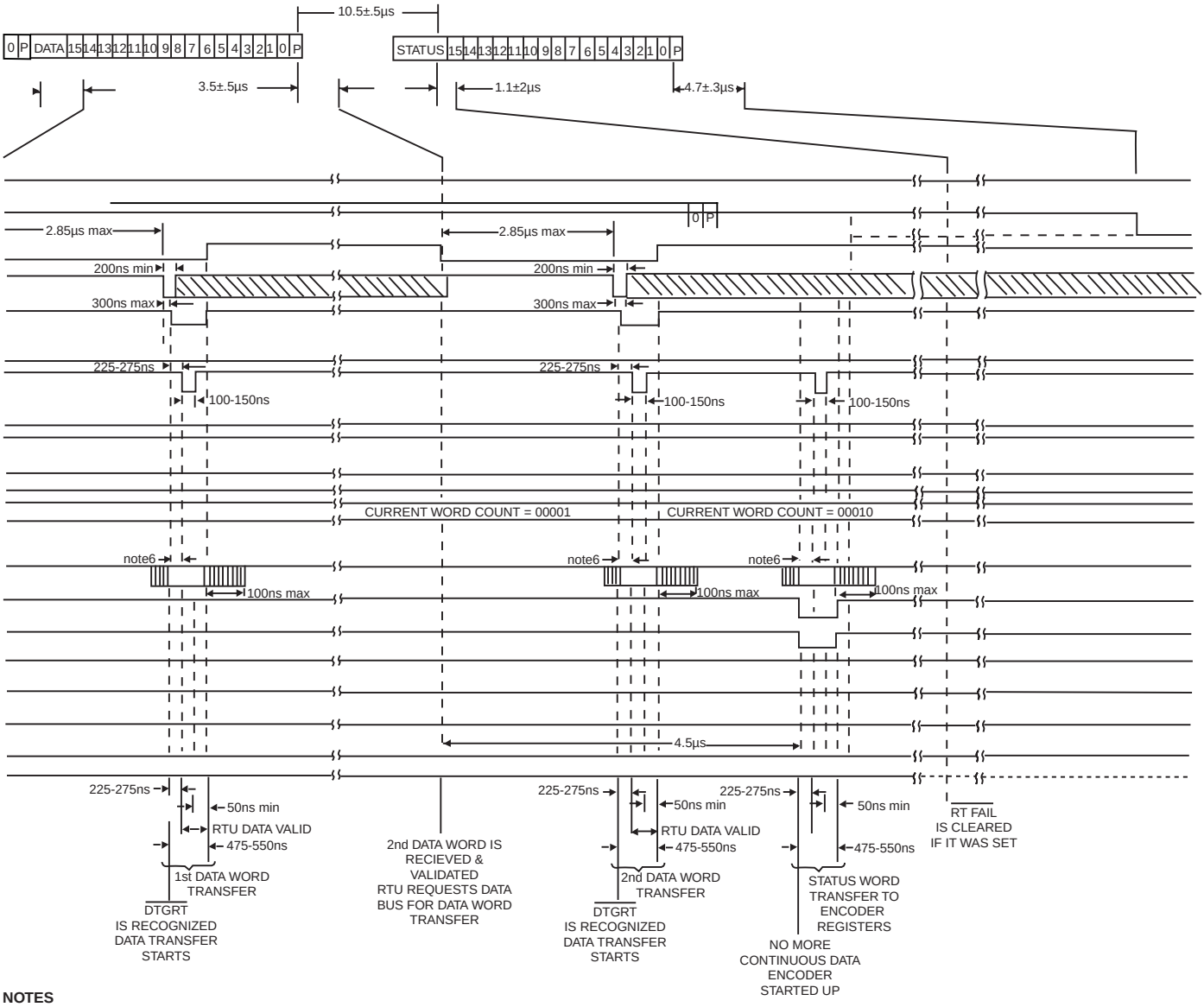


FIGURE 5. RT TO RT (RECEIVE) TIMING DIAGRAM



NOTES

1. LEGEND
   - DON'T CARE
   - DATA BUS UNDEFINED
   - REPRESENTS THE SEQUENCE OF EVENTS IF THE COMMAND WAS BROADCAST.
     NOTE: NO STATUS WOULD BE TRANSMITTED ON1553 BUS.
2. EACH WORD IS DRIVEN FOR ≅ 18-19µS ON D15-D0.
   IF BUF ENA IS ACTIVE THE LAST WORD IS AVAILABLE FOR 3.5-4µS SINCE THE STATUS WORD MUST BE SUPPORTED.
3. DATA BUS IS SHOWN WITH BUF ENA CONNECTED TO DTACK (SEE PIN FUNCTION TABLE, PIN 67)
4. THE TIMING DIAGRAM REPRESENTS A DTGRT RESPONSE TIME OF 0.92µS FOR COMMAND TRANSFER AND 2.1µS FOR DATA.
   THE MAXIMUM RESPONSE TIME FROM DTREQ TO DTGRT TO GUARANTEE A SUCCESSFUL TRANSFER IS 1.5µS FOR THE COMMAND TRANSFER AND 2.33µS FOR DATA TRANSFER TO THE SUBSYSTEM. THE POSITION OF DTACK WILL VARY DEPENDING ON WHEN DGRT IS ISSUED
5. RTFAIL IS CLEARED WHEN THE STATUS WORD IS TRANSMITTED. ONCE SET, FLAG WILL REMAIN SET FOR THE ENTIRE MESSAGE.
   THE INCMD FALLING EDGE CAN BE USED TO LATCH RTFAIL STATUS.
6. 100nS MIN REPRESENTS SETUP TIME FOR VALID DATA BEFORE DTSTR GOES LOW.

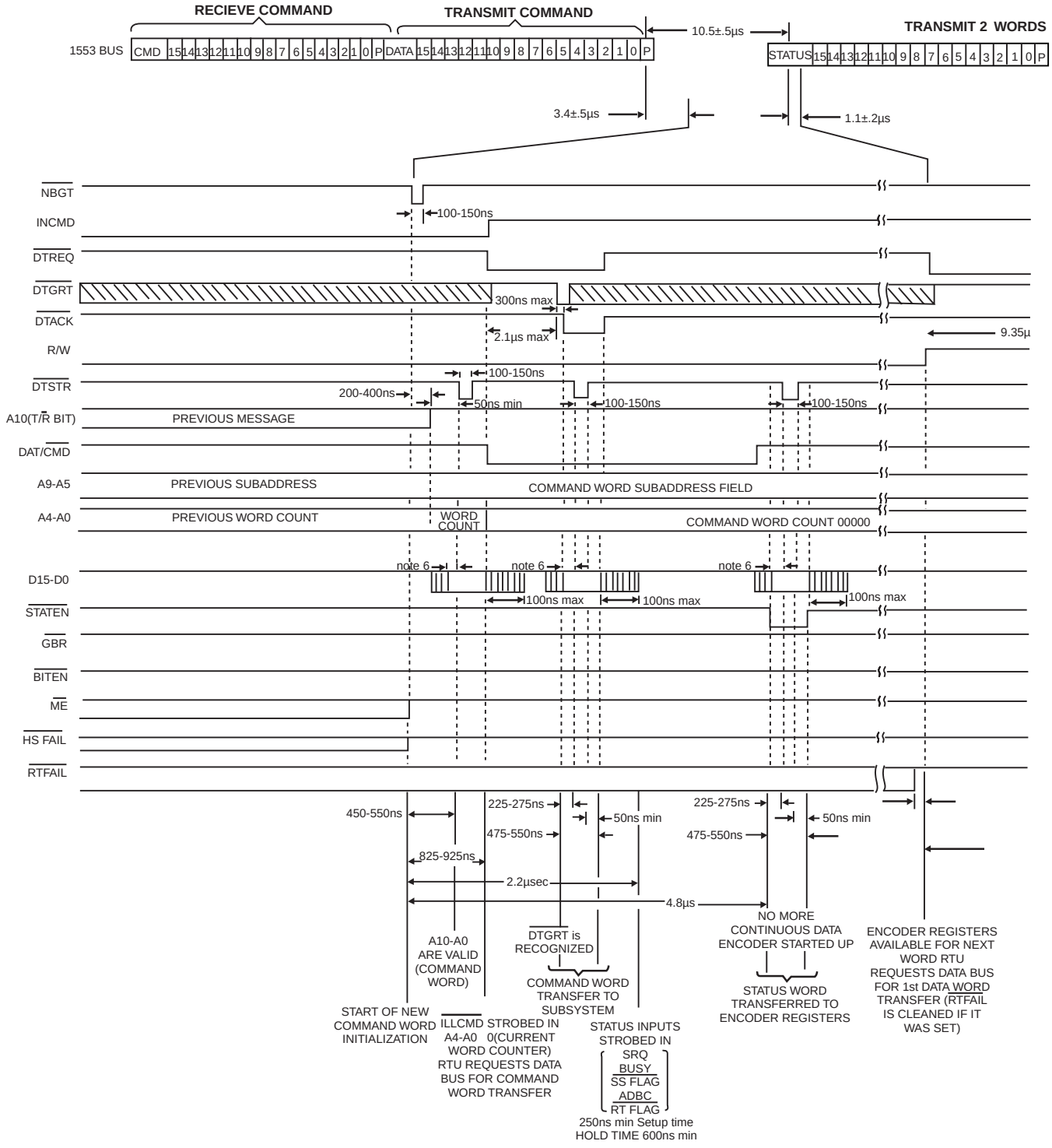
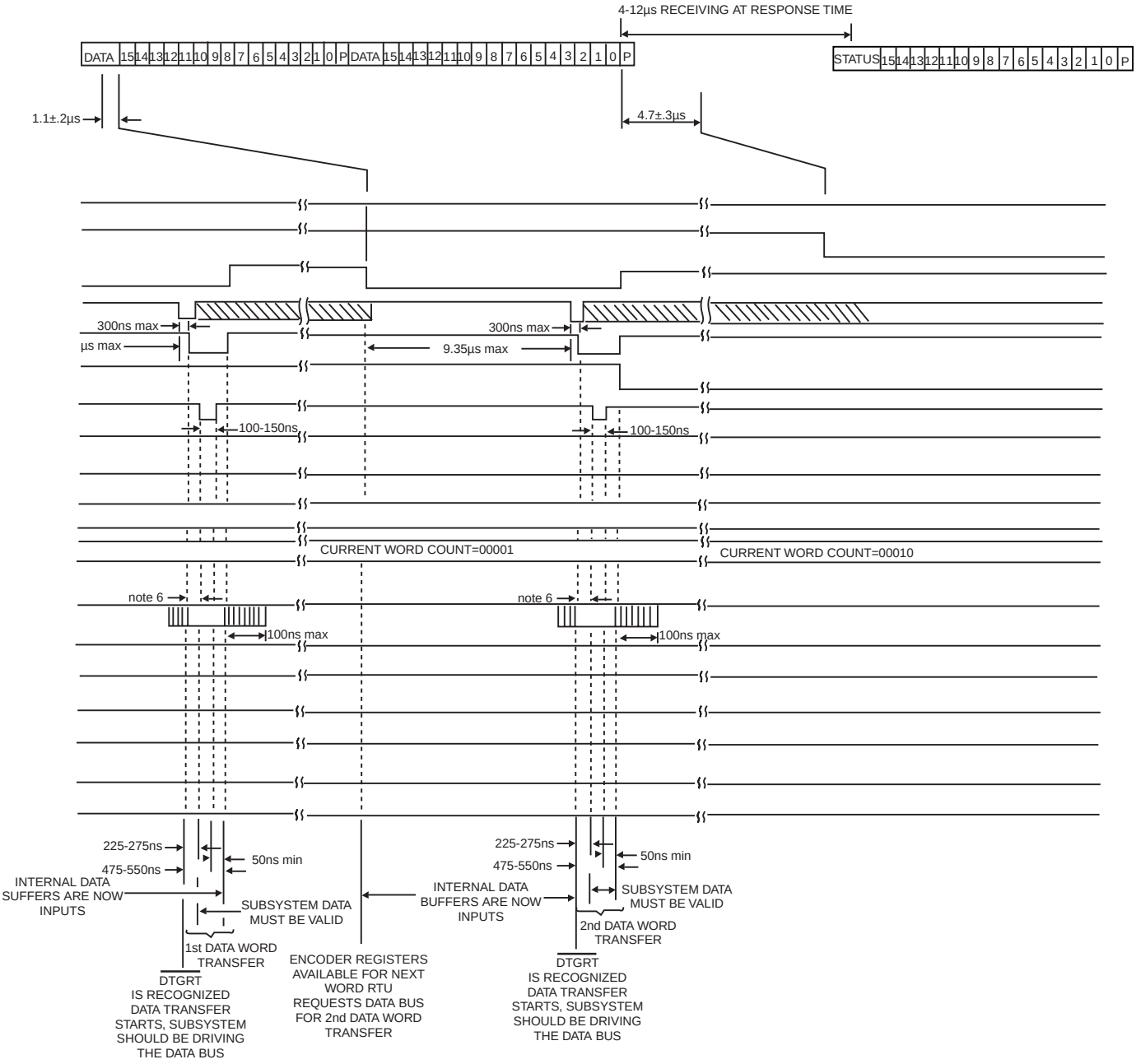


FIGURE 6. RT TO RT (TRANSMIT) TIMING DIAGRAM



NOTES

1. LEGEND
   - DON'T CARE
   - DATA BUS UNDEFINED
   - REPRESENTS THE SEQUENCE OF EVENTS IF THE COMMAND WAS BROADCAST.
     NOTE: NO STATUS WOULD BE TRANSMITTED ON1553 BUS.
2. EACH WORD IS DRIVEN FOR ≅ 18-19µS ON D15-D0.
   IF BUF ENA IS ACTIVE THE LAST WORD IS AVAILABLE FOR 3.5-4µS SINCE THE STATUS WORD MUST BE SUPPORTED.
3. DATA BUS IS SHOWN WITH BUF ENA CONNECTED TO DTACK (SEE PIN FUNCTION TABLE, PIN 67)
4. THE MAXIMUM RESPONSE TIME FROM DTREQ TO DTGRT TO GUARANTEE A SUCCESSFUL TRANSFER IS 2.1µS FROM THE COMMAND WORD AND 9.35µS FROM THE DATA TRANSFER FROM THE SUBSYSTEM. THE POSITION OF DTACK WILL VARY DEPENDING ON WHEN DGRT IS ISSUED. THE TIME WILL BE 100Ns MIN TO 150nS FROM DTREQ.
5. RTFAIL IS CLEARED WHEN THE STATUS WORD IS TRANSMITTED. ONCE SET, FLAG WILL REMAIN SET FOR THE ENTIRE MESSAGE. THE INCMD FALLING EDGE CAN BE USED TO LATCH RTFAIL STATUS.
6. 100nS MIN REPRESENTS SETUP TIME FOR VALID DATA BEFORE DTSTR GOES LOW FOR A WRITE CYCLE. A READ CYCLE REQUIRES VALID DATA 150nS MAX AFTER DTACK GOES LOW.

MODE CODES

The BUS-65142 implements all mode codes applicable to dual-redundant systems. Mode codes can also be illegalized using the appropriate I/O signals. Mode command illegalization and handling are detailed below in TABLE 2.

TABLE 2. MODE CODES IMPLEMENTED

DYNAMIC BUS CONTROL (00000)
MESSAGE SEQUENCE = DBC * STATUS
The RT responds with status. If the subsystem wants control of the bus, it must set DBACC in the Configuration Register.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits Set: message error (SW), High Word Count (BIT Word).
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Bits set: message error (S/W), T/R Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No status response. Bits Set: message error, broadcast received (S/W), Illegal Mode Code, T/R Error (BIT Word).
5. **Broadcast Address.** No status response. Bits Set: message error, broadcast received (S/W), Illegal Mode Code (BIT Word).

SYNCHRONIZE WITHOUT DATA WORD (00001)
MESSAGE SEQUENCE = SYNC * STATUS
The RT responds with status. If sent as a broadcast, the broadcast receive bit will be set and status response suppressed.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No statue response. Bits Set: message error (SW), High Word Count (BIT Word)
3. **T/$\overline{R}$ bit Set to Zero.** No statue response. Bits set: message error (S/W), T/R Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No statue response. Bits Set: message error, broadcast received (S/W), Illegal Mode Code, T/R Error (BIT Word).

STATUS WORD (00010)
MESSAGE SEQUENCE = TRANSMIT WORD * STATUS
The status and BIT word registers are not altered by this command and contain the status from the previous command.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No statue response. Bits Set: message error (SW), High Word Count (BIT Word)
3. **T/$\overline{R}$ bit Set to Zero.** No statue response. Bits set: message error (S/W), T/R Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No statue response. Bits Set: message error, broadcast received (S/W), Illegal Mode Code, T/R Error (BIT Word).
5. **Broadcast Address.** No statue response. Bits Set: message error, broadcast received (S/W), T/R Error (BIT Word).

INITIATE SELF-TEST (00011)
MESSAGE SEQUENCE = SELF TEST * STATUS
The RT responds with a status word. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. Short-loop test is initiated on the status word transmitted. If the test fails, an RT fail flag is set.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No statue response. Bits Set: message error (SW), High Word Count (BIT Word)
3. **T/$\overline{R}$ bit Set to Zero.** No statue response. Bits set: message error (S/W), T/R Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No statue response. Bits Set: message error, broadcast received (S/W), T/R Error (BIT Word).
5. **Faulty Test.** Bits set: terminal flag (S/W), A/$\overline{B}$ Loop Test Fail, Current 1553 Bus (A or B) Loop Test Fail (BIT Word)

TRANSMITTER SHUTDOWN (00100)
MESSAGE SEQUENCE =SHUTDOWN * STATUS
This command is only used with dual redundant bus systems. The RT responds with status. At the end of the status transmission, the RT inhibits any further transmission from the dual redundant channel. Once shutdown, the transmitter can only be reactivated by OVERRIDE TRANSMITTER SHUTDOWN or RESET RT commands.
ERROR CONDITIONS
1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No statue response. Bits Set: message error (SW), High Word Count (BIT Word)
3. **T/$\overline{R}$ bit Set to Zero.** No statue response. Bits set: message error (S/W), T/R Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No statue response. Bits Set: message error, broadcast received (S/W), Illegal Mode Code, T/R Error (BIT Word).

***** = Status Response Time

TABLE 2. MODE CODES IMPLEMENTED (continued)

OVERRIDE TRANSMITTER SHUTDOWN (00101)

MESSAGE SEQUENCE = OVERRIDE SHUTDOWN * STATUS

This command is only used with dual redundant bus systems. The RTU responds with status. At the end of the status transmission, the RTU re-enables the transmitter of the redundant bus. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No statue response. Bits Set: message error (SW), High Word Count (BIT Word)
3. **T/$\overline{R}$ bit Set to Zero.** No statue response. Bits set: message error, broadcast received (S/W), T/R Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No statue response. Bits Set: message error, broadcast received (S/W), Illegal Mode Code, T/R Error (BIT Word).

INHIBIT TERMINAL FLAG BIT (00110)

MESSAGE SEQUENCE = INHIBIT TERMINAL FLAG * STATUS

The RTU responds with status and inhibits further internal or external setting of the terminal flag bit in the status register. Once the terminal flag has been inhibited, it can only be reactivated by an Override Inhibit Terminal Flag or Reset RT command. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No statue response. Bits Set: message error (SW), High Word Count (BIT Word)
3. **T/$\overline{R}$ bit Set to Zero.** No statue response. Bits set: message error (S/W), T/R Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No statue response. Bits Set: message error, broadcast received (S/W), T/R Error (BIT Word).

OVERRIDE INHIBIT TERMINAL FLAG BIT (00111)

MESSAGE SEQUENCE = OVERRIDE INHIBIT TERMINAL FLAG * STATUS

The RTU responds with status and reactivates the terminal flag bit in the status register. If the command was broadcast, the broadcast received bit is set and and status transmission is suppressed.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No statue response. Bits Set: message error (SW), High Word Count (BIT Word)
3. **T/$\overline{R}$ bit Set to Zero.** No statue response. Bits set: message error (S/W), T/R Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No statue response. Bits Set: message error, broadcast received (S/W), T/R Error (BIT Word).

RESET REMOTE TERMINAL (01000)

MESSAGE SEQUENCE = RESET REMOTE TERMINAL * STATUS

The RTU responds with status and internally reseets. Transmitter shutdown, mode commands, BIT Word, and inhibit terminal flag commands will be reseet. If the command was broadcast, the broadcast received bit is set and the status word is suppressed.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No statue response. Bits Set: message error (SW), High Word Count (BIT Word).
3. **T/$\overline{R}$ bit Set to Zero.** No statue response. Bits Set: message error (S/W), T/R Error (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No statue response.. Bits set: message error, broadcast received (S/W), T/R Error (BIT Word).

RESERVED MODE COMMAND (01001-01111)

MESSAGE SEQUENCE = RESERVED MODE COMMAND * STATUS

The RTU responds with clear status and no data. If the command is illegalized through an optional PROM, the message error bit is set and only the ststus word is transmitted.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No statue response. Bits Set: message error (SW), High Word Count (BIT Word).
3. **T/$\overline{R}$ bit Set to Zero.** No statue response. Bits set: message error (S/W), Illegal Mode Code (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No statue response. Bits Set: message error, broadcast received (S/W), Illegal Mode Code (BIT Word).

***** = Status Response Time

TABLE 2. MODE CODES IMPLEMENTED (continued)

TRANSMIT VECTOR WORD (10000)

MESSAGE SEQUENCE = TRANSMIT VECTOR WORD * STATUS VECTOR WORD

The RTU transmits a status word followed by a vector word.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits Set: message error (SW), High Word Count (BIT Word)
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Bits set: message error (S/W),Low Word Count (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No status response. Bits Set: message error, broadcast received (S/W), Illegal Mode Code, T/R Error, Low Word Count (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (S/W), Illegal Mode Code, (BIT Word).

SYNCHRONIZE WITH DATA WORD (10001)

MESSAGE SEQUENCE = SYNCHRONIZE WITH DATA WORD * STATUS

The data word received fo;;owing the command word is transferred to RAM. The status word is then transmitted. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed..

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No status response. Bits Set: message error (SW), Low Word Count (BIT Word)
3. **Command Followed by too many Data Words.** No status response. Bits Set: message error (SW), High Word Count (BIT Word)
4. **Command T/$\overline{R}$ bit Set to One.** No status response. Bits set: message error (S/W), T/R Error, High Word Count (BIT Word).
5. **Command T/$\overline{R}$ bit Set to Zero and Broadcast Address.** No status response. Bits set: message error, broadcast received (S/W), High Word Count, T/R Erro (BIT Word).

TRANSMIT LAST COMMAND (10010)

MESSAGE SEQUENCE = TRANSMIT LAST COMMAND * STATUS

The status and BIT word registers are not altered by this command. The SW contains the status from the previous command. The data word transmitted contains the prevous valid command (providing it was not another TRANSMIT LAST COMMAND).

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits Set: message error (SW)
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Bits set: message error (S/W), T/R Error, Low Word Count (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No status response. Bits Set: message error (S/W), Illegal Mode Code, T/R Error (BIT Word).
5. **Broadcast Address.** No status response. Bits Set: message error, broadcast received (S/W), Illegal Mode Code (BIT Word).

TRANSMIT BIT WORD (10011)

MESSAGE SEQUENCE = TRANSMIT BIT WORD * STATUS

The RTU responds with status followed by the BIT word. The BIT word is not altered by this command; however, the next SW will reflect errors in this trnsmission.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits Set: message error (SW).
3. **T/$\overline{R}$ bit Set to Zero.** No status response. Bits Set: message error (S/W), T/R Error, Low Word Count (BIT Word).
4. **Zero T/$\overline{R}$ bit and Broadcast Address.** No status response.. Bits set: message error (S/W), Illegal Mode Code, T/R Error, Low Word Count (BIT Word).
5. **Broadcast Address.**No status response.. Bits set: message error, broadcast received (S/W), Illegal Mode Code (BIT Word)

***** = Status Response Time

TABLE 2. MODE CODES IMPLEMENTED (continued)

SELECTED TRANSMITER SHUTDOWN (10100)

MESSAGE SEQUENCE = SELECTED TRANSMITER SHUTDOWN * STATUS VECTOR WORD

The data word received is transmitted to the subsystem and status is transmitted. No other action is taken by the RTU. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. Intended for use with RT's with more than one dual redundant channel.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No status response. Bits Set: message error (SW), High Word Count, Illegal Mode Code (BIT Word)
3. **Command Followed by too many Data Word.** No status response. Bits Set: message error (SW), Low Word Count, Illegal Mode Code (BIT Word)
4. **Command T/$\overline{R}$ bit Set to One.** No status response. Bits set: message error (S/W), Illegal Mode Code, High Word Count (BIT Word).
5. **Command T/$\overline{R}$ bit Set to One and Broadcast Address.** No status response. Bits Set: message error, broadcast received (S/W), Illegal Mode Code, High Word Count (BIT Word).

OVVERRIDE SELECTED TRANSMITTER SHUTDOWN (10101)

MESSAGE SEQUENCE = OVVERRIDE SELECTED TRANSMITTER SHUTDOWN * STATUS

The data word received after the command is transferred to the subsystem. No other action is taken by the RTU. If the command was broadcast, the broadcast received bit is set and status transmission suppressed.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No status response. Bits Set: message error (SW), Low Word Count, Illegal Mode Code (BIT Word)
3. **Command Followed by too many Data Words.** No status response. Bits Set: message error (SW), High Word Count, Illegal Mode Code (BIT Word)
4. **Command T/$\overline{R}$ bit Set to One.** No status response. Bits set: message error (S/W), Illegal Mode Code, High Word Count (BIT Word).
5. **Command T/$\overline{R}$ bit Set to One and Broadcast Address.** No status response. Bits set: message error, broadcast received (S/W), Illegal Mode Code, High Word Count, T/R Erro (BIT Word).

RESERVED MODE CODES (10110-11111)

MESSAGE SEQUENCE = RESERVED MODE CODE (T/R = 1) * STATUS
RESERVED MODE CODE (T/R = 0) * STATUS

If Valid (T/R = 0)

The RTU responds with status. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed. If the command is illegalized through an optional PROM, the message error bit is set and only the status word is transmitted.

If Valid (T/R = 1)

Respond with status and one data word.

ERROR CONDITIONS (T/R = 1)

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits Set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).

ERROR CONDITIONS (T/R = 0)

1. **Invalid Command.** No response, command ignored.
2. **Command not followed by Contiguous Data Word.** No status response. Bits set: message error (S/W), Low Word Count, Illegal Mode Code (BIT Word).
3. **Command followed by to many Data Words.** No status response. Bits Set: message error (S/W), High Word Count, Illegal Mode Code (BIT Word).

UNDEFINED MODE CODES

(T/R = 0, MODE CODES 00000 TO 01111)

No Response, set message error bit.

***** = Status Response Time

PIN FUNCTION TABLE				
PACKAGE & PIN			FUNCTION	DESCRIPTION
78-Pin QIP	82-Pin Flat-Pack	78-Pin Flat-Pack		
1	2	1	A9 (SA4)	Latched output of the most significant bit (MSB) in the subaddress field of the command word.
2	4	3	A7 (SA2)	Latched output of the third most significant bit in the subaddress field of the command word.
3	6	5	A5 (SA0)	Latched output of the least significant bit (LSB) in the subaddress field of the command word.
4	8	7	DB1	Bi-directional parallel data bus Bit 1
5	10	9	DB3	Bi-directional parallel data bus Bit 3
6	12	11	DB5	Bi-directional parallel data bus Bit 5
7	14	13	DB7	Bi-directional parallel data bus Bit 7
8	16	15	DB9	Bi-directional parallel data bus Bit 9
9	18	17	DB11	Bi-directional parallel data bus Bit 11
10	20	19	DB13	Bi-directional parallel data bus Bit 13
11	22	21	DB15	Bi-directional parallel data bus Bit 15 (MSB)
12	24	23	BRO ENA	Broadcast enable - when HIGH, this input allows recognition of an RT address of all ones in the command word as a broadcast message. When LOW, it prevents response to RT address 31 unless it has the assigned terminal address.
13	26	25	ADDRE (RTAD4)	Input of the MSB of the assigned terminal address.
14	28	27	ADDRC (RTAD2)	Input of the 3rd MSB of the assigned terminal address.
15	30	29	ADDRA (RTAD0)	Input of the LSB of the assigned terminal address.
16	32	31	$\overline{\text{RTADERR}}$	Output signal used to inform subsystem of an address parity error. If LOW, indicates parity error and the RT will not respond to any command address to a single terminal. It will respond to broadcast commands if BRO ENA is HIGH.
17	34	33	$\overline{\text{TXDATA B}}$	LOW output to the primary side of the coupling transformer that connects B channel of the 1553 bus.
18	36	35	NC	
19	38	37	GND B	Power Supply return connection for the B channel transceiver.
20	40	39	RXDATA B	Input from the HIGH side of the primary side of the coupling transformer that connects to the B channel of the 1553 Bus.
21	81	78	A3 (WC3/ CWC3)	Multiplexed address line output. When INCMD is LOW or A5 thru A9 are all zeroes or all ones (Mode Command), it represents the latched output of the 2nd MSB in the word count field of the command word. When INCMD is HIGH and A5 thru A9 are not all zeroes or all ones, it represents the 2nd MSB of the current word counter.
22	79	76	A1 (WC1/ CWC1)	Multiplexed address line output. When INCMD is LOW or A5 thru A9 are all zeroes or all ones (Mode Command), it represents the latched output of the 2nd LSB in the word count field of the command word. When INCMD is HIGH and A5 thru A9 are not all zeroes or all ones, it represents the 2nd LSB of the current word counter.

PIN FUNCTION TABLE (continued)				
PACKAGE & PIN			FUNCTION	DESCRIPTION
78-Pin QIP	82-Pin Flat-Pack	78-Pin Flat-Pack		
23	77	74	$\overline{\text{DTGRT}}$	Data transfer grant -- active LOW input signal from the subsystem that informs the RT, when $\overline{\text{DTREQ}}$ is asserted, to start the transfer. Once transfer is started, $\overline{\text{DTGRT}}$ can be removed.
24	75	72	INCMD	In-Command -- HIGH level output signal used to inform the subsystem that the RT is presently servicing a command.
25	73	70	$\overline{\text{HSFAIL}}$	Handshake Fail-- output signal that goes LOW and stays LOW whenever the subsystem fails to supply $\overline{\text{DTGRT}}$ in time to do a successful transfer. Cleared by the next $\overline{\text{NBGT}}$.
26	71	68	$\overline{\text{DTSTR}}$	A LOW level output pulse (166ns) present in the middle of every data word transfer over the parallel data bus. Used to latch or strobe the data into memory, FIFOs, registers, etc. Recommended using the rising edge to clock data in.
27	69	66	(DAT/$\overline{\text{CMD}}$)	Address line output that is LOW whenever the command word is being transferred to the subsystem over the parallel data bus, and is HIGH whenever data words are being transfered.
28	67	64	$\overline{\text{RTFAIL}}$	Remote Terminal Failure-- latched active LOW output signal to the subsystem to flag detection of a remote terminal continuous self-test failure. Also set if the Watchdog Timeout circuit is activated. Cleared by the start of the next message transmission (status word) and set if problem is again detected.
29	65	62	$\overline{\text{DTREQ}}$	Data Transfer Request --active LOW output signal to the subsystem indicating that the RT has data for or needs data from the subsystem and requests a data transfer over the parallel data bus. Will stay LOW until transfer is completed or transfer timeout has ocurred.
30	63	60	$\overline{\text{ADBC}}$	Accept Dynamic Bus Control-- active LOW input signal from the subsystem used to set the Dynamic Bus Control Acceptance bit in the status register if the command word was a valid, legal mode command for dynamic bus control.
31	61	58	TEST 2	Factory test point output-DO NOT USE (see note 1)*
32	59	56	A10 (T/$\overline{\text{R}}$)	Latched output of the T/R bit in the command word.
33	57	54	$\overline{\text{ILLCMD}}$	Illegal Command--active LOW input signal from the subsystem, strobed in on the rising edge of INCMD. Used to define the command word as illegal and to set the message error bit in the status register.
34	55	52	$\overline{\text{SS REQ}}$	Subsystem Service Request-- Input from the subsystem used to control the Service Request Bit in the status register. If LOW when the status word is updated, the Service Request Bit will be set; if HIGH, it will be cleared.
35	53	50	$\overline{\text{BITEN}}$	Built-in-Test Word Enable--LOW level output pulse (.5µs), present when the built-in-test word is enabled on the parallel data bus.
36	51	48	$\overline{\text{RXDATA A}}$	Input from the LOW side of the primary side of the coupling transformer that connects to the A channel of the 1553 Bus.

PIN FUNCTION TABLE (continued)				
PACKAGE & PIN			FUNCTION	DESCRIPTION
78-Pin QIP	82-Pin Flat-Pack	78-Pin Flat-Pack		
—	49	46	+5VA	+5V input power supply connection for the A channel transceiver.
38	47	44	-VA	-15V/-12V input power supply connection for the A Channel transceiver (Note 5).
39	45	42	TXDATA A	HIGH output to the primary side of the coupling transformer that connects to the A channel of the 1553 Bus.
40	43	40	$\overline{\text{NBGT}}$	New Bus Grant -- LOW level output pulse (166ns) used to indicate the start of a new protocol sequence in response to the command word just received.
41	3	2	A8 (SA3)	Latched output of the 2nd MSB in the subaddress field of the command word.
42	5	4	A6 (SA1)	Latched output of the 2nd LSB in the subaddress field of the command word.
43	7	6	DB0	Bi-directional parallel data bus Bit 0 (LSB)
44	9	8	DB2	Bi-directional parallel data bus Bit 2
45	11	10	DB4	Bi-directional parallel data bus Bit 4
46	13	12	DB6	Bi-directional parallel data bus Bit 6
47	15	14	DB8	Bi-directional parallel data bus Bit 8
48	17	16	DB10	Bi-directional parallel data bus Bit 10
49	19	18	DB12	Bi-directional parallel data bus Bit 12
50	21	20	DB14	Bi-directional parallel data bus Bit 14
51	23	22	+5V	+5V input power supply connection for RTU digital logic section.
52	25	24	GND	Power supply return for RTU digital logic section.
53	27	26	ADDRD	Input of the 2nd MSB of the assigned terminal address.
54	29	28	ADDRB	Input of the 2nd LSB of the assigned terminal address.
55	31	30	ADDRP	Input of Address Parity Bit. The combination of assigned terminal address and ADDRP must be odd parity for the RT to work.
56	33	32	TXDATA B	HIGH, output to the primary side of the coupling transformer that connects to the B channel transceiver.
—	35	34	-VB	-15V/-12V input power supply connection for the B channel transceiver (Note 5).
58	37	36	+5VB	+5 V input power supply connection for the B channel transceiver.
59	39	38	$\overline{\text{RXDATA B}}$	Input from the LOW side of the primary side of the coupling transformer that connects to the B channel of the 1553 Bus.
60	80	77	A2 (WC2/ CSW2)	Multiplexed address line output. When INCMD is LOW or A5 thru A9 are all zeroes or all ones (Mode Command), it represents the latched output of the 3rd MSB in the word count field of the command word. When INCMD is HIGH and A5 thru A9 are not all zeroes or all ones, it represents the 3rd MSB of the current word counter.
61	78	75	A0 (WCO/ CSWO)	Multiplexed address line output. When INCMD is LOW or A5 thru A9 are all zeroes or all ones (Mode Command), it represents the latched output of the LSB in the word count field of the command word. When INCMD is HIGH and A5 thru A9 are not all zeroes or all ones, it represents the LSB of the current word counter.

PIN FUNCTION TABLE (continued)				
PACKAGE & PIN			FUNCTION	DESCRIPTION
78-Pin QIP	82-Pin Flat-Pack	78-Pin Flat-Pack		
62	76	73	$\overline{\text{DTACK}}$	Data Transfer Acknowledge-- active LOW output signal during data transfers to or from the subsystem indicating the RTU has received the $\overline{\text{DTGRT}}$ in response to $\overline{\text{DTREQ}}$ and is presently doing the transfer. Can be connected directly to (BUF ENA) for control of tri-state data buffers; and to tri-state address buffer control lines, if they are used.
63	74	71	A4 (WC4/ CWC4)	Multiplexed address line output. When INCMD is LOW or A5 thru A9 are all zeroes or all ones (Mode Command), it represents the latched output of the MSB in the word count field of the command word. When INCMD is HIGH and A5 thru A9 are not all zeroes or all ones, it represents the MSB of the current word counter.
64	72	69	RD/$\overline{\text{WR}}$	Read/$\overline{\text{Write}}$-- output signal that controls the direction of the internal data bus buffers. Normally, the signal is LOW and the buffers drive the data bus. When data is needed from the subsystem, it goes HIGH to turn the buffers around and the RT now appears as an input. The signal is HIGH only when $\overline{\text{DTREQ}}$ is active (LOW).
65	70	67	$\overline{\text{GBR}}$	Good Block Received--LOW level output pulse (.5µs) used to flag the subsystem that a valid, legal, non-mode receive command with the correct number of data words has been received without a message error and successfully transferred to the subsystem.
66	68	65	16MHz IN	16MHz Clock Input--input for the master clock used to run RTU circuits.
67	66	63	$\overline{\text{BUF ENA}}$	Buffer Enable-- input used to enable or tri-state the internal data bus buffers when they are driving the bus. When LOW, the data bus buffers are enabled. Could be connected to $\overline{\text{DTACK}}$, if RT is sharing the same data bus as the subsystem. (see note 2)*.
68	64	61	$\overline{\text{RESET}}$	Input resets entire RT when LOW.
69	62	59	$\overline{\text{RTFLAG}}$	Remote Terminal Flag--Input signal used to control the terminal flag bit in the status register. If LOW when the status word is updated, the terminal flag bit would be set; if HIGH, it would be cleared. Normally connected to $\overline{\text{RTFAIL}}$.
70	60	57	$\overline{\text{TEST 1}}$	Watchdog Timeout test point--DO NOT USE. (See note 3)* (input).
71	58	55	$\overline{\text{SSBUSY}}$	Subsystem Busy-- input from the subsystem used to control the busy bit in the status register. If LOW when the status word is updated, the busy bit will be set, if HIGH it will be cleared. If the busy bit is set in the status register, no data will be requested from the subsystem in response to a transmit command. On receive commands, data will be transferred to the subsystem.
72	56	53	$\overline{\text{SSFLAG}}$	Subsystem Flag-- input from the subsystem used to control the subsystem flag bit in the status register. If LOW when the status word is updated, the subsystem flag will be set; if HIGH it will be cleared.

PIN FUNCTION TABLE (continued)				
PACKAGE & PIN			FUNCTION	DESCRIPTION
78-Pin QIP	82-Pin Flat-Pack	78-Pin Flat-Pack		
73	54	51	$\overline{ME}$	Message Error--output signal that goes LOW and stays LOW whenever there is a format or word error with the received message over the 1553 Data Bus. Cleared by the next $\overline{NGBT}$.
74	52	49	RXDATA A	Input from the HIGH side of the primary side of the coupling transformer that connects to the A channel of the 1553 Bus.
75	50	47	GND A	Power supply return connection for the A channel transceiver.
76	48	45	N/C	Not connected.
77	46	43	$\overline{TXDATA}$ A	Low output to the primary side of the coupling transformer that connects to the A channel of the 1553 Bus.
78	44	41	$\overline{STATEN}$	Status Word Enable-- LOW level active output signal present when the status word is enabled on the parallel data bus.
–	1,41, 42,82	–	N/C	These pins are not used on this package.

PIN FUNCTION TABLE NOTES:

1. TEST 2

This pin provides the output of the BUS-65142 BIT Comparison output. It indicates the loop test results for every word transmitted by the BUS-65142. A test can be performed by actioning the RTU to transmit while the test fixture opens the receiver lines to force an error condition. A logic 1 (high) indicates the loop test passed. Normally this pin is left open.

2. $\overline{BUFENA}$

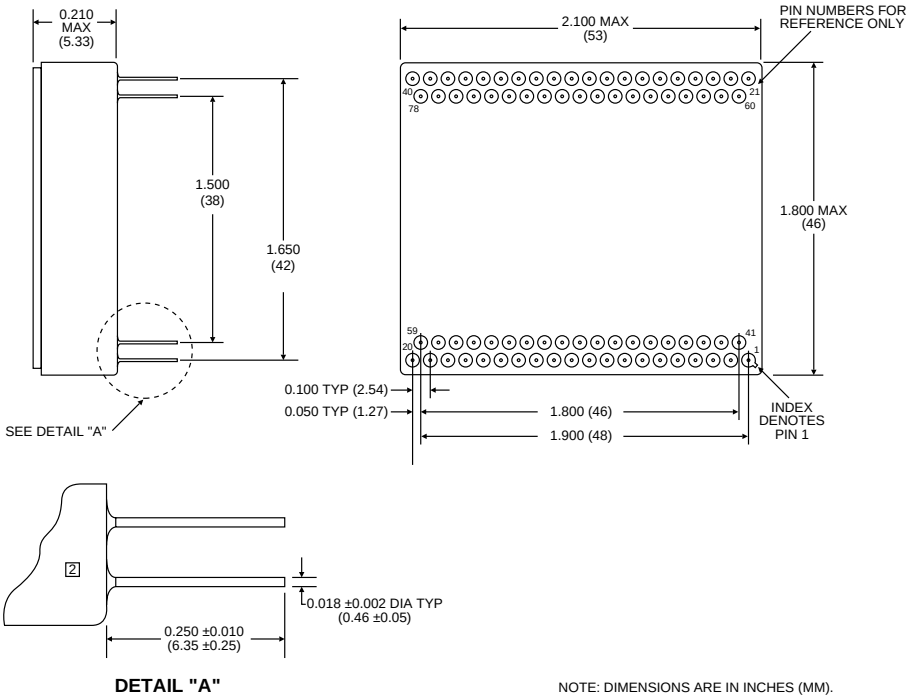
This pin is typically tied to $\overline{DTACK}$, causing the BUS-65142 to drive the shared data bus only while $\overline{DTACK}$ is active. If desired $\overline{BUFENA}$ can be grounded. The data will remain latched on the data bus pins for 18µs from $\overline{DTSRB}$ and 3.5µs for the last word of a message as the device's status word or BIT word is transferred to the BC ($\overline{STATEN}$ or $\overline{BITEN}$ low). Once the STATUS or BIT Word transfer is complete, the data bus will automatically again contain the last data word. The BUS-65142 will automatically switch the direction of the internal buffers during a transmit operation.

3. $\overline{TEST}$ 1

This test allows the user to force the active channel to transmit indefinetly, in order to test the built in Watchdog Timer feature of the BUS-65142. When this pin is grounded and the active channel is stimulated with a valid transmit command, the BUS-65142 will respond with a status word and contiguous data (last data word loaded or STATUS WORD if none is loaded) until the built-in time out occurs. Normally this pin is left open or an optional pull-up can be used.

4. PINS 1, 41, 42, 82 for BUS-65144/45 82-pin Flat Pack, FIGURE 8 are not connected (N/C).

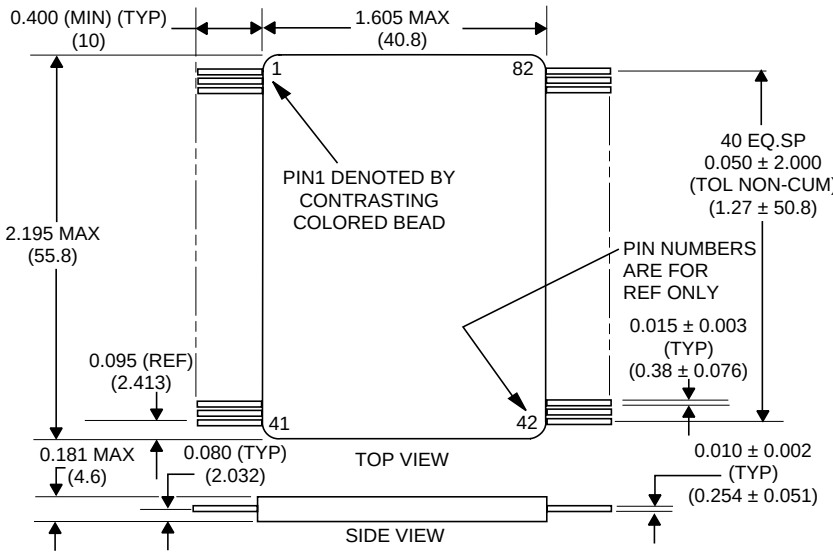
5. $-V_A$ and $-V_B$ are not connected (N/C) for BU-65142X3.



DETAIL "A"

NOTE: DIMENSIONS ARE IN INCHES (MM).

FIGURE 7. BUS-65142/43 MECHANICAL OUTLINE (STANDARD PRODUCT) (78-PIN KOVAR QIP)



Note: Dimensions are in inches (millimeters).

**FIGURE 8. BUS-65144/45 MECHANICAL OUTLINE (STANDARD PRODUCT)
(82-PIN KOVAR FLAT PACK)**

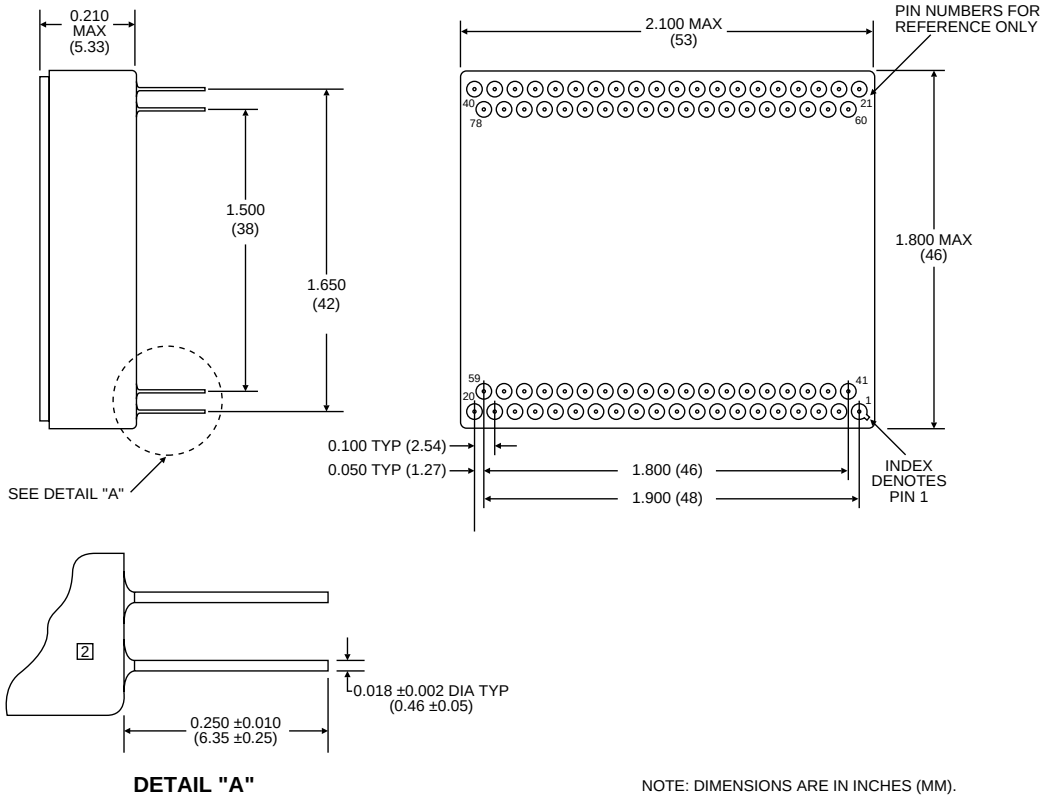


**FIGURE 9. BU-65142D MECHANICAL OUTLINE (HI-REL RADIATION TOLERANT VERSION
(78-PIN CERAMIC QIP)**

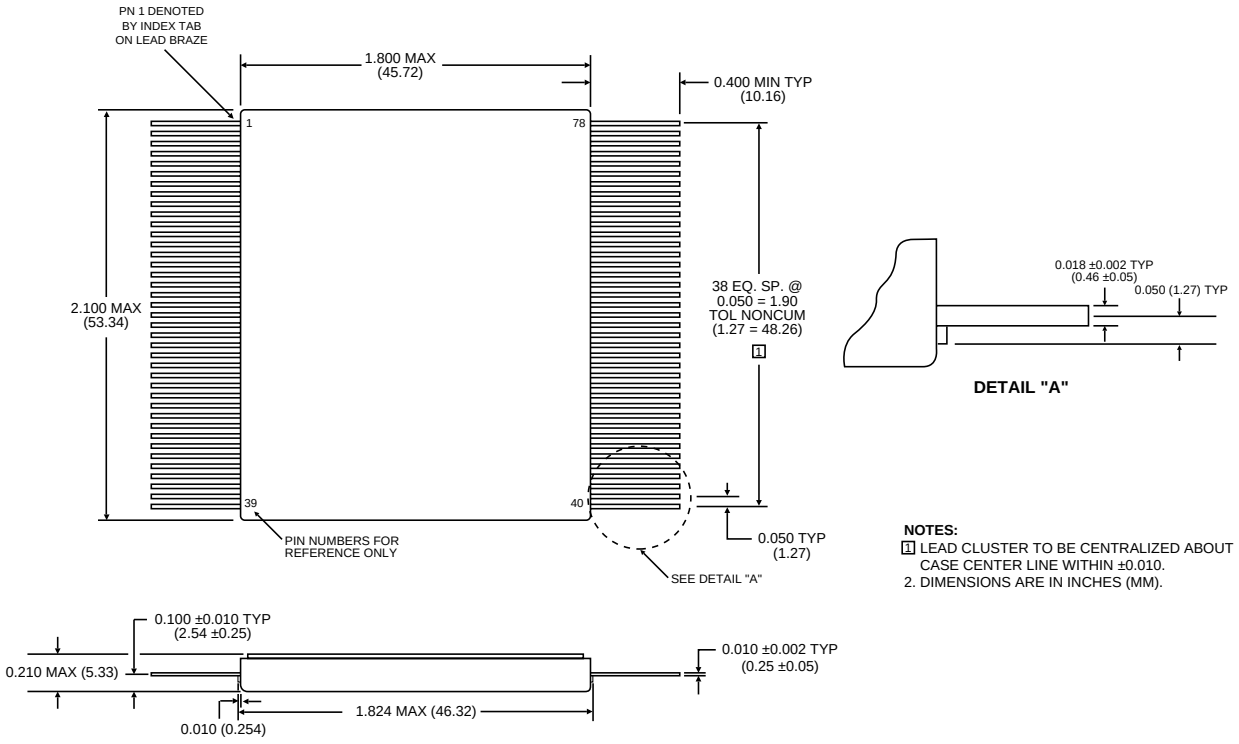


FIGURE 10. BU-65142F MECHANICAL OUTLINE (HI-REL / RADIATION TOLERANT VERSION) (78-PIN CERAMIC FLAT PACK)

ORDERING INFORMATION

BU-65142D1- 110X

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- K = One Lot Date Code
- W = One Lot Date Code and PreCap Source
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, PreCap Source and 100% Pull Test
- Blank = None of the Above

Test Criteria:
- 0 = None

Process Requirements:
- 0 = Standard DDC Processing, no Burn-In (See page xiii.)
- 1 = MIL-PRF-38534 Compliant
- 2 = B*
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In

Temperature Grade/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

Transceiver Option:
- 1 =+15 Volts and - 15 Volts
- 2 =+5 Volts and - 12 Volts

Package Options:
- D = 78-pin QIP Package (See Figure 9)
- F = 78-pin Flatpack (See Figure 10)

Product Type:
- BU-65142 = Radiation Tolerant Remote Terminal

ORDERING INFORMATION

BUS-6514X- XX0X

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- K = One Lot Date Code
- W = One Lot Date Code and PreCap Source
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, PreCap Source and 100% Pull Test
- Blank = None of the Above

Test Criteria:
- 0 = None

Process Requirements:
- 0 = Standard DDC Processing, no Burn-In (See page xiii.)
- 1 = MIL-PRF-38534 Compliant
- 2 = B*
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In

Temperature Grade/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

Power Supply and Packaging
- 2 = -15 V 78-pin QIP (See Figure 7)
- 3 = -12 V 78-pin QIP (See Figure 7)
- 4 = -15 V 82-pin Flat Pack (See Figure 8)
- 5 = -12 V 82-pin Flat Pack (See Figure 8)

* Standard DDC Processing with burn-in and full temperature test: see table below.

Mating Transformer: BUS-25679 is for the BUS-65142, and BU-65142X1.
BUS-29854 is for the BUS-65143, and BU-65142X2.

STANDARD DDC PROCESSING		
TEST	**MIL-STD-883**	
	METHOD(S)	**CONDITION(S)**
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	A
BURN-IN	1015, Table 1	—

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