IF 1-Chip Processor (Video IF and Mono FM Sound IF)

Description

The U4462B is a a video/sound IF concept for TV-IF signal processing. The circuit processes all video IF signals with negative modulation and FM sound IF signals (mono FM intercarrier sound). With 5 V supply voltage, the U4462B is suitable for TV, VCR and multimedia applications.

Features

- 5 V supply voltage; low power consumption
- Minimum number of external components
- Active carrier generation by FPLL principle (frequency-phase-locked-loop) for true synchronous demodulation
- Very linear video demodulation, excellent pulse response and good intermodulation figures
- VCO circuit is operating on picture carrier frequency
- Alignment-free AFC without external reference circuit
- VIF-AGC with peak sync detection
- Tuner AGC with adjustable take-over point
- Completely alignment-free PLL demodulator for FM-intercarrier sound IF signals (mono)

Ordering Information

Extended Type Number	Package	Remarks
U4462B–BSD	SDIP28	
U4462B–BFLG3	SO28	Delivery in taped form

Block Diagram

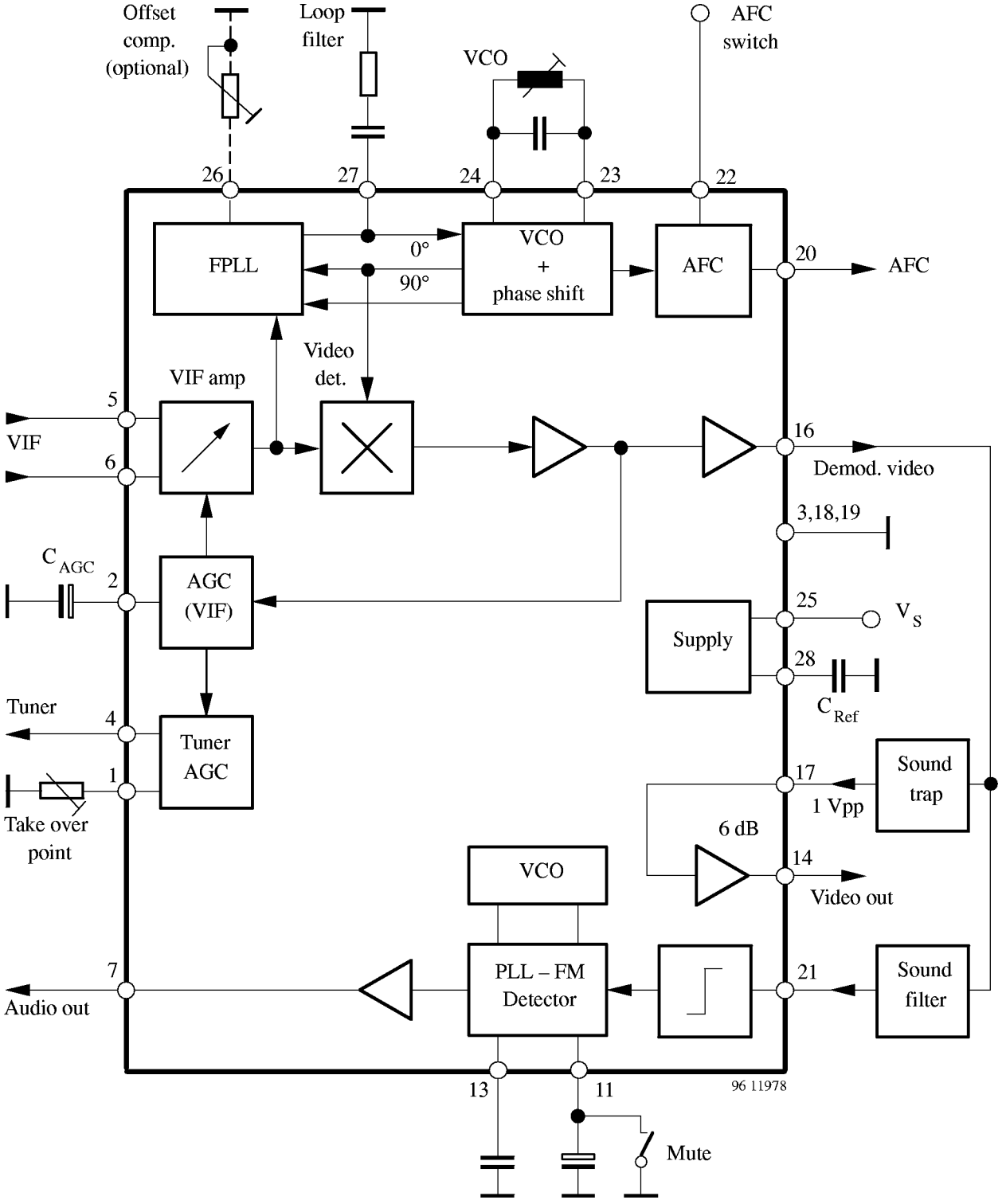


Figure 1. Block diagram

Circuit Description

Vision IF Amplifier

The video IF signal (VIF) is fed through a SAW filter to the differential input (Pin 5-6) of the VIF amplifier. This amplifier consists of three ac-coupled amplifier stages. Each differential amplifier is gain controlled by the automatic gain control (VIF-AGC). The output signal of the VIF amplifier is applied to the FPLL carrier generation and the video demodulator.

Tuner-and VIF-AGC

At Pin 2, the VIF-AGC charges/discharges the AGC capacitor to generate a control voltage for setting the gain of VIF amplifier and tuner in order to keep the demodulated video output signal (Pin 16) at a constant level. Therefore, the sync level of the demodulated video signal is the criterion for a fast charge/discharge of the AGC capacitor. The AGC control voltage at Pin 2 is transferred to an internal control signal and is fed to the tuner AGC to generate the tuner AGC current on Pin 4 (open collector output). The take-over point of the tuner AGC can be adjusted at Pin 1 by a potentiometer or an external dc voltage (from interface circuit or microprocessor).

FPLL, VCO and AFC

The FPLL circuit (frequency-phase-locked loop) consists of a frequency- and a phase detector to generate control voltage for the VCO tuning. In locked mode, the VCO is controlled by the phase detector and in unlocked mode the frequency detector is superimposed. The VCO operates with an external resonance circuit (L and C parallel) and is controlled by internal varicaps. The VCO control voltage at Pin 27 (loop filter) is also converted to a current and represents the AFC output signal at Pin 20.

A practicable VCO alignment of the external coil is the adjustment to zero AFC output current at Pin 20. At center frequency the AFC output current is equal to zero. The optional potentiometer at Pin 26 allows an offset compensation of the VCO phase for improved sound quality (fine adjustment). Without a potentiometer (open circuit at Pin 26), this offset compensation is not active.

The oscillator signal passes a phase shifter and supplies the in-phase signal (0°) and the quadrature signal (90°) of the generated picture carrier.

AFC Switch

The AFC output signal at Pin 20 can be controlled by a switching voltage at Pin 22. It is possible to switch off the AFC.

Video Demodulation and Amplifier

The video IF signal, which is applied from the gain-controlled IF amplifier, is multiplied with the in-phase component of the VCO signal. The video demodulator is designed for low distortion and large bandwidth. The demodulator output signal passes an integrated low-pass filter for attenuation of the residual vision carrier and is fed to the video amplifier. The video amplifier is realized by an operational amplifier with internal feedback and 8 MHz bandwidth. An additional noise clipping is provided. The video signal is fed to VIF-AGC and to the video output buffer. This amplifier offers easy adaptation of the sound trap and sound filter. For nominal video IF modulation, the video output signal at Pin 16 is 1.5 V (peak-to-peak value).

Sound IF Limiter Amplifier

The intercarrier signal coming from the sound filter is fed to a 7-stage limiter amplifier. This guarantees high input sensitivity and excellent AM suppression.

PLL-FM Demodulator

The alignment–free "Phase-Locked-Loop" (PLL) FM demodulator covers a wide frequency range of 4.5 MHz up to 6.5 MHz with excellent noise performance. The linear voltage-to-frequency characteristic results in low harmonic distortion. The free-running frequency of the internal VCO circuit is about 5.5 MHz.

Audio Amplifier, De-emphasis and Mute Switch

The demodulated FM signal is bufferred to Pin 7 via de-emphasis filter. The de-emphasis low-pass filter consists of an internal 5-kΩ series resistor and an external capacitor at Pin 13. FM muting is possible by switching Pin 11 to ground.

Pin Description

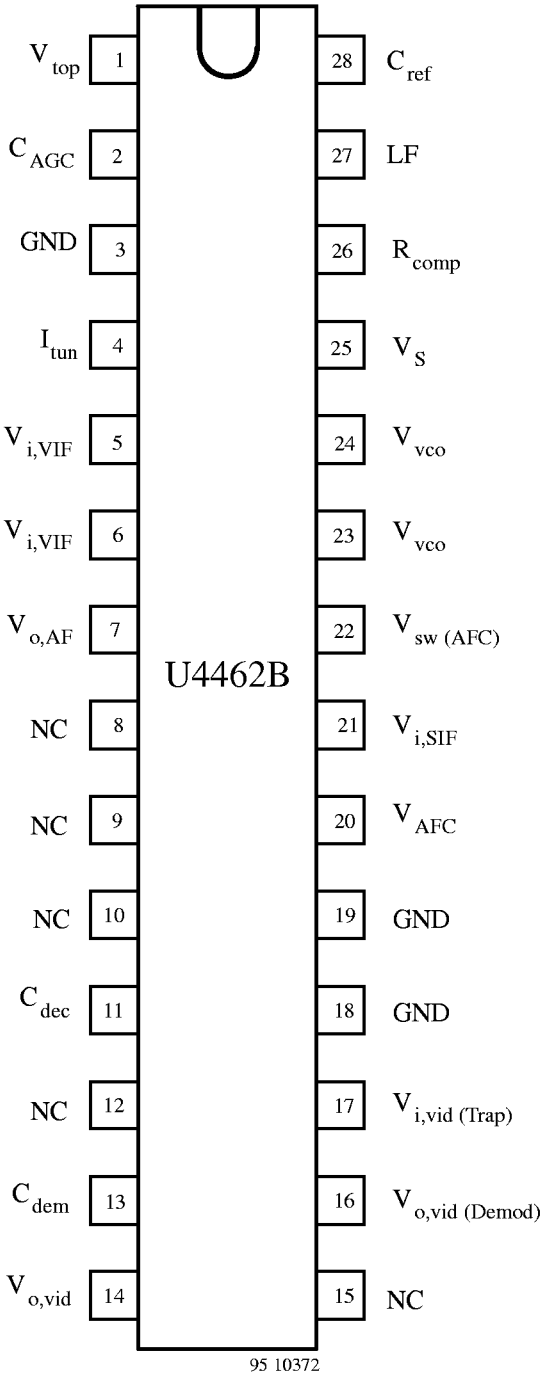


Figure 2. Pinning

Pin	Symbol	Function
1	V_{top}	Tuner AGC – take over point
2	C_{AGC}	VIF-AGC (time constant)
3	GND	Ground
4	I_{tun}	Tuner AGC output current
5, 6	$V_{i,VIF}$	VIF input (symmetrical)
7	$v_{o,AF}$	Audio output
8	NC	Not connected
9	NC	Not connected
10	NC	Not connected
11	C_{dec}	Decoupling capacitor and mute switch
12	ND	Not connected
13	C_{dem}	De-emphasis capacitor
14	$v_{o,vid}$	Video output (6 dB amplifier)
15	NC	Not connected
16	$V_{o,vid}$	Video demodulator output
17	$V_{i,vid}$	Video input (6 dB amplifier)
18	GND	Ground
19	GND	Ground
20	V_{AFC}	AFC output
21	$v_{i,SIF}$	FM sound IF input
22	V_{sw}	AFC control switch
23, 24	V_{vco}	VCO circuit (FPLL)
25	V_s	Supply voltage
26	R_{comp}	Offset compensation
27	LF	Loop filter
28	C_{ref}	Internal reference voltage

Absolute Maximum Ratings

Reference point Pin 3 (19), unless otherwise specified

Parameters		Symbol	Value	Unit
Supply voltage SDIP28 package SO28 package	Pin 25	V_s	9.0 6.0	V V
Supply current	Pin 25	I_s	80	mA
Power dissipation	V_S = 9 V V_S = 6 V	P	720 480	mW mW
Output currents	Pins 10, 14, 15 and 16	I_{out}	5	mA
External voltages	Pins 1, 2, 5, 6, 7, 11, 13, 14, 16, 17, 21, 26, 28 23, 24, 27 4 20, 22	V_{ext}	+ 4.5 + 3.5 + 13.5 V_S	V V V V
Junction temperature		T_j	+125	°C
Storage temperature		T_{stg}	–25 to +125	°C
Electrostatic handling *) all Pins		V_{ESD}	± 200	V

*) equivalent to the discharge of a 200-pF capacitor via a 0-Ω resistor

Operating Range

Parameters		Symbol	Value	Unit
Supply voltage range SDIP28 package SO28 package	Pin 25	V_S	4.5 to 9.0 4.5 to 6.0	V V
Ambient temperature		T_{amb}	0 to +70	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient (when soldered to PCB) SDIP28 package SO28 package	R_{thJA}	55 75	K/W K/W

Electrical Characteristics

V_s = +5 V, T_{amb} = +25°C; reference point Pin 3 (19), unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
DC supply	Pin 25					
Supply voltage SDIP28 package SO28 package		V_S	 4.5 4.5	 5.0 5.0	 9.0 6.0	 V V
Supply current		I_S	65	73	80	mA
VIF input	Pin 5–6					
Input sensitivity, RMS value	For FPLL locked	$v_{i,VIF}$		80	120	μV_{RMS}
Input resistance	See note 1, page 10	R_{in}		1.2		kΩ
Input capacitance	See note 1, page 10	C_{in}		2		pF
IF AGC	Pin 2					
IF gain control range		G_v	60	65		dB
AGC capacitor		C_{AGC}		2.2		µF
Tuner AGC	Pins 1 and 4	(see note 2, page 10)				
Available tuner-AGC current		I_{tun}	1	2	4	mA
Permissible output voltage		V_{tun}	0.3		13.5	V
IF slip – tuner AGC	Current I_{tun}: 10% to 90%	ΔG_{IF}		8	10	dB
IF input signal for minimum take-over point	R_{top} = 10 kΩ (V_{top}= 4.5 V)	v_{in}			4	mV
IF input signal for maximum take-over point	R_{top} = 0 (V_{top} = 0.8 V)	v_{in}	40			mV
Variation of the take-over point by temperature	ΔT_{amb} = 55°C VIF-AGC: G_v = 46 dB	Δv_{in}		2	3	dB
FPLL and VCO	Pins 23, 24, 26 and 27	(see note 3, page 10)				
Max. oscillator frequency	For carrier generation	f_{vco}	60			MHz
Vision carrier capture range	f_{vco} = 38.9 MHz C_{vco} = 6.8 pF	Δf_{cap}	± 1.5	± 2		MHz
Oscillator drift (free-running) as a function of temperature	See note 4, page 10 ΔT_{amb} = 55°C, C_{vco} = 6.8 pF, f_{vco} = 38.9 MHz	$\Delta f/\Delta T$			–0.3	%
Video demodulator output	Pin 16					
Output current -source -sink	DC and AC DC and AC	$\pm I_{out}$	4 2		5 3	mA mA
Output resistance	See note 1, page 10	R_{out}			100	Ω
Video output signal	Peak-to-peak value	$v_{o,vid}$	1,26	1,4	1,54	V_{pp}
Sync level		V_{sync}		1.8		V
Zero carrier level (ultra-white level)	AGC voltage V_2= 3 V	V_{DC}		3.3		V
Supply-voltage influence on the ultra-white level		ΔV/V		1		%/V
Video bandwidth (–3 dB)	$R_L \geq$ 1 kΩ, $C_L \leq$ 50 pF	B	6	8		MHz

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Video frequency response over the AGC range		ΔB			2.0	dB
Differential gain error		DG		2	5	%
Differential phase error		DP		2	5	deg
Intermodulation 1.07 MHz related to color carrier	Test signal unmodulated, with picture carrier: 0 dB color carrier: – 6 dB sound carrier: – 24 dB	α_{IM}	52			dB
Video signal to noise ratio	Weighted, CCIR–567	$S/_N$	56	60		dB
Residual vision carrier fundamental wave 38.9 MHz and second harmonic 77.8 MHz		v_{res}		2	10	mV
Ripple rejection, Pin 25/ 16	See note 1, page 10	RR	35			dB
AFC output	Pin 20					
Control slope		$\Delta I/_{\Delta f}$		0.7		µA/kHz
Frequency drift by temperature	Related to the picture carrier frequency			0.25	0.6	%
Output voltage: upper limit lower limit		V_{AFC}	V_s–0.6		 0.6	 V V
Output current		I_{AFC}		± 0.2		mA
AFC switch	Pin 22					
Control voltage: AFC “off” AFC “on”	See note 5, page 10	V_{sw}	 0 2.0		 0.8 V_s	 V V
Switching current		I_{sw}		± 100		µA
Video input (6 dB amplifier):	Pin 17					
Input resistance	See note 1, page 10	R_{in}		3		kΩ
Input capacitance	See note 1, page 10	C_{in}		2.0		pF
Internal dc bias voltage (clamping voltage)		V_{DC}		1.7		V
Video input signal (CVBS)	Peak-to-peak value	$v_{i,vid}$		1		V_{pp}
Video output (6 dB amplifier):	Pin 14					
DC output voltage (Sync)		V_{DC}		1.25		V
Voltage gain, Pin 17, 14		G_v		6		dB
Video output signal (CVBS)	Peak-to-peak value $v_{in} = 1V_{pp}$ Pin 17	$v_{o,vid}$		2		V_{pp}
FM sound IF input:	Pin 21					
Input limiting voltage, RMS value	AF output signal at Pin 7: –3 dB	$v_{i,SIF}$			150	mV_{RMS}
DC input voltage		V_{DC}		1.7		V
Input resistance	See note 1, page 10	R_{in}		600	750	Ω
Input capacitance	See note 1, page 10	C_{in}		1.5		pF

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
FM – PLL						
Free-running frequency		f_{vco}		5.5		MHz
Oscillator drift (free running) as a function of temperature	$\Delta T = 55$ °C	Δf_{vco}		500		kHz
Oscillator shift (free running) as a function of supply voltage	$4.5\ V < V_s < 9.0\ V$	Δf_{vco}		200		kHz
Capture range of PLL		Δf_{cap}	±1.4	±1.9		MHz
Holding range of PLL		Δf_{hold}	±2.0	±3.0		MHz
Audio output	Pin 7					
DC output voltage		V_{DC}		2.3		V
AF output voltage		$v_{o,AF}$		500		mV_{RMS}
Output resistance		R_{out}		140		Ω
De-emphasis capacitor	Pin 13					
Value of de-emphasis capacitor		C_{dem}		10		nF
Decoupling capacitor and mute switch	Pin 11					
Value of decoupling capacitor		C_{dec}		2.2		µF
Control voltage for "mute off"	AF "on", see note 6	V_{sw}	2.0		V_s	V
Control voltage for "mute on"	AF "off"	V_{sw}	0		0.8	V

Notes:

1.) This parameter is given as an application information and not tested during production.

2.) An adjustment of the turn-over point (delayed tuner AGC) with external resistor R_{top} or external voltage V_{top} is possible.

3.) External resonance circuit of VCO: f = 38.9 MHz, C_{VCO} = 6.8 – 10 pF, coil L_{VCO} with unloaded Q factor $Q_O \geq 55$, minimum oscillator voltage $V_{Pin24} = 40\ mV_{RMS}$

4.) The oscillator drift is related to the picture carrier frequency, with an external temperature-compensated LC circuit.

5.) Without control voltage at Pin 22, the "AFC on" mode is automatically selected.

6.) Without external control voltage at Pin 11, the mute function is not active.

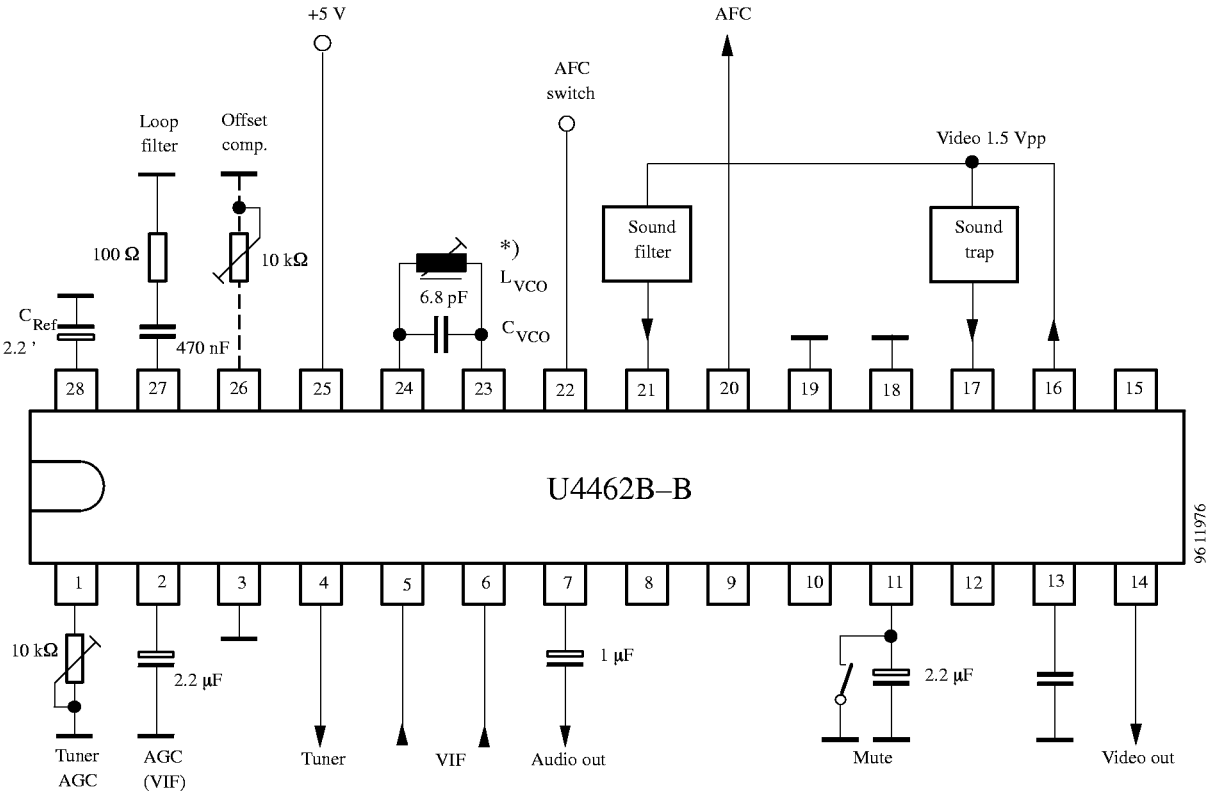


Figure 3. Test circuit

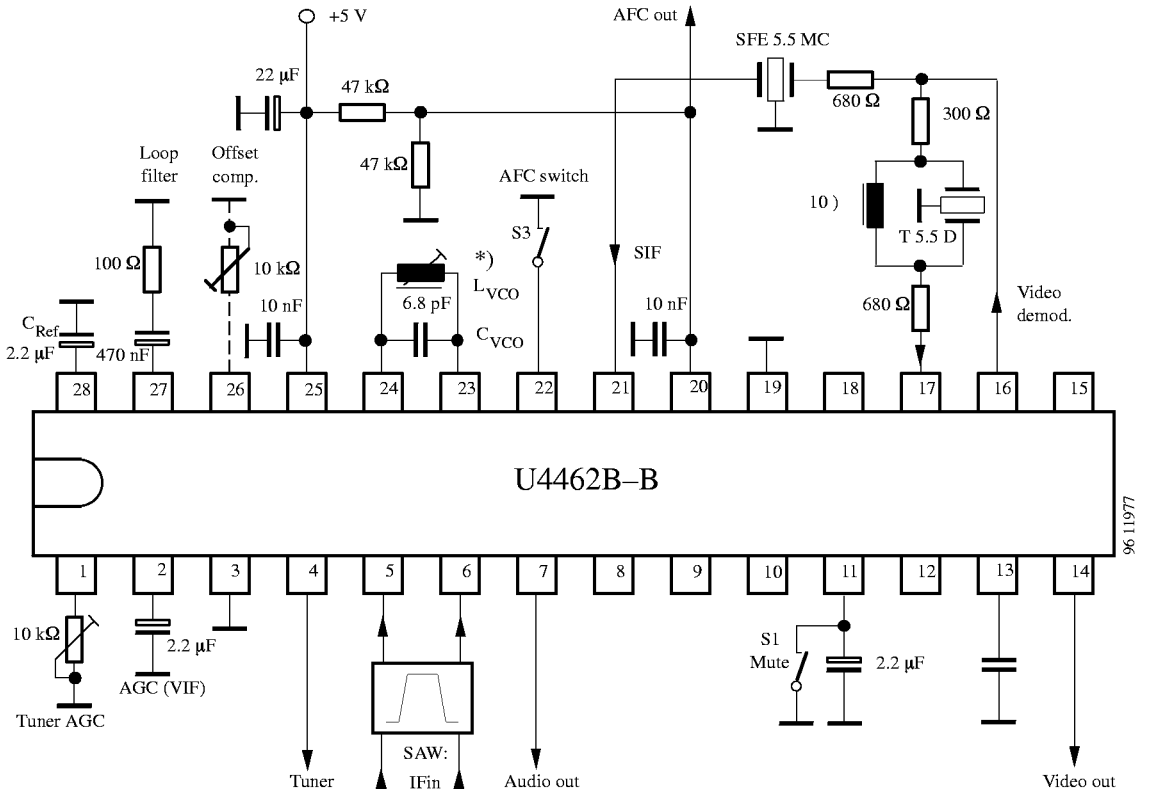


Figure 4. Basic application circuit

Internal Pin Configuration

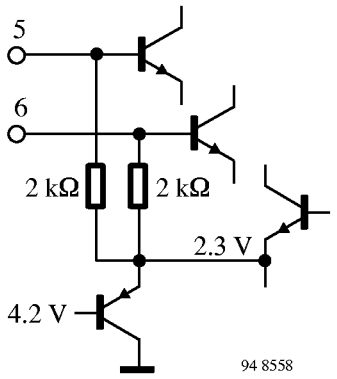


Figure 5. Video IF input (Pins 5 and 6)

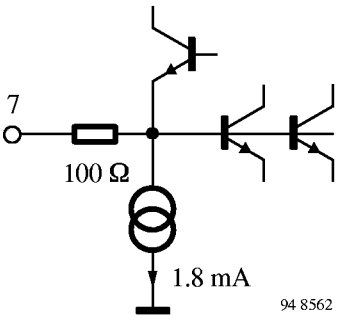


Figure 9. Audio output (Pin 7)

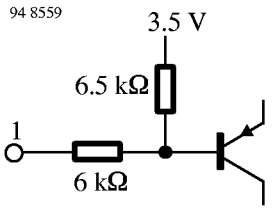


Figure 6. Take-over point – tuner AGC (Pin 1)

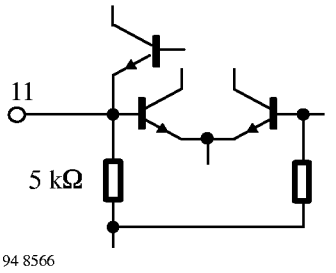


Figure 10. Decoupling capacitor (Pin 11) and mute switch

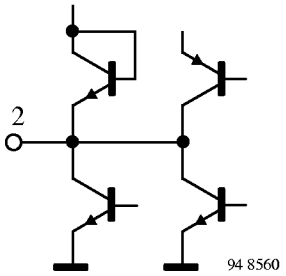


Figure 7. Time constant – VIF AGC (Pin 2)

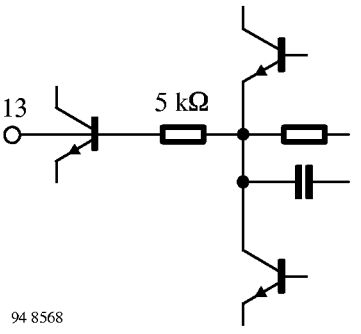


Figure 11. De-emphasis (Pin 13)

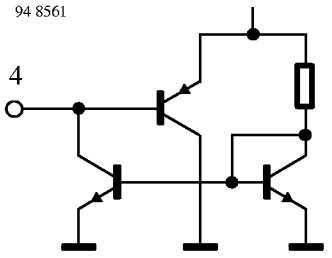


Figure 8. Tuner AGC current output (Pin 4)

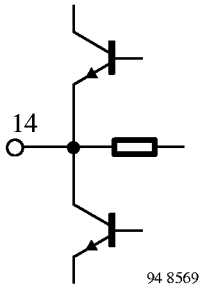


Figure 12. Video output (6 dB amplifier) (Pin 14)

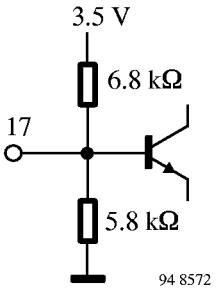


Figure 13. Video input (6 dB amplifier) (Pin 17)

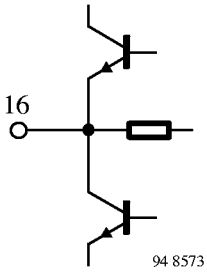


Figure 14. Video demodulator output (Pin 16)

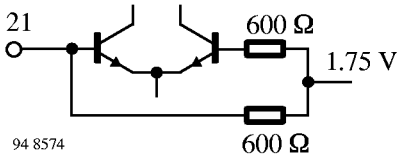


Figure 15. FM sound IF input (Pin 21)

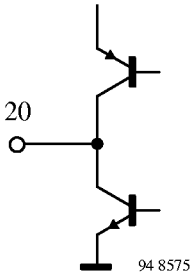


Figure 16. AFC output (Pin 20)

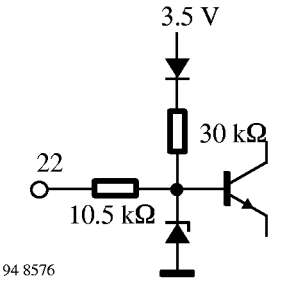


Figure 17. AFC control switch (Pin 22)

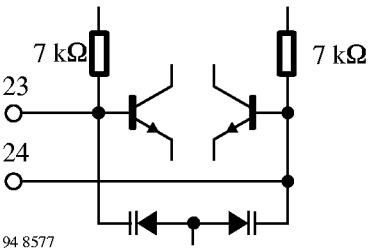


Figure 18. VCO circuit (Pin 23–24)

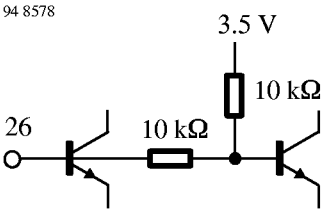


Figure 19. Offset compensation (Pin 26)

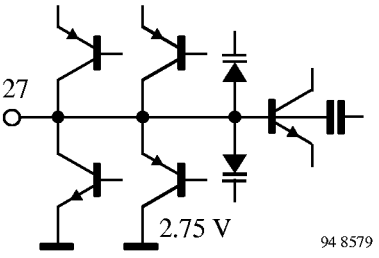


Figure 20. Loop filter (Pin 27)

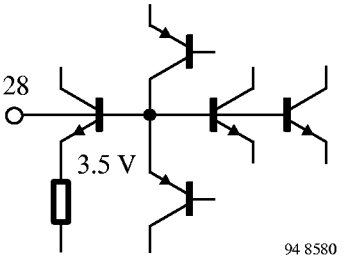
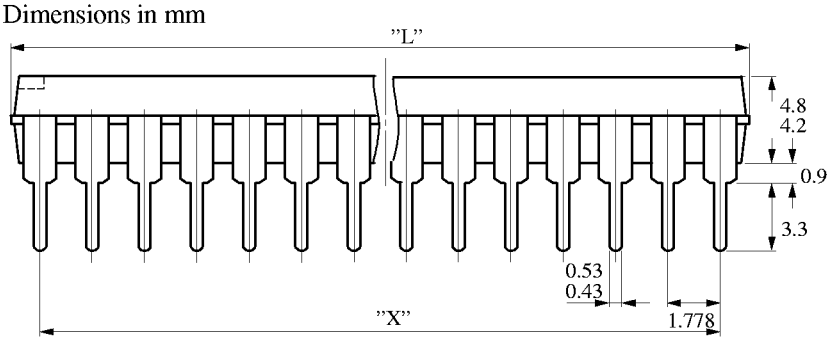


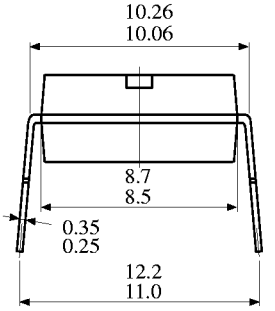
Figure 21. Internal reference voltage (Pin 28)

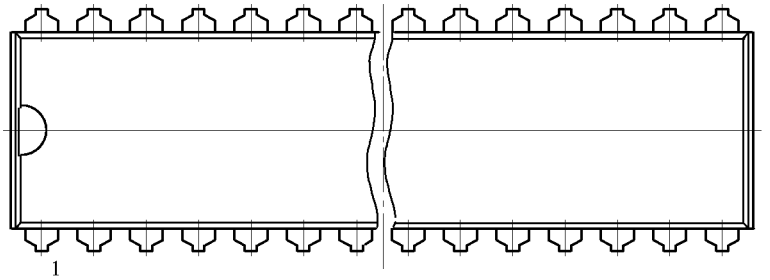
Package Information

Package SDIP28–30

Dimensions in mm







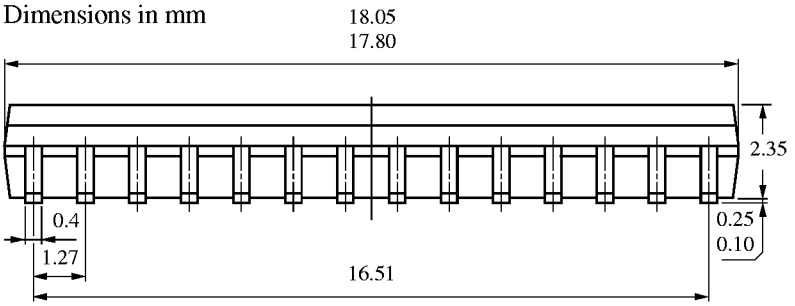
Package	"L" min	"L" max	"X"
SDIP28	27.1	27.5	23.114
SDIP30	27.1	27.5	24.892

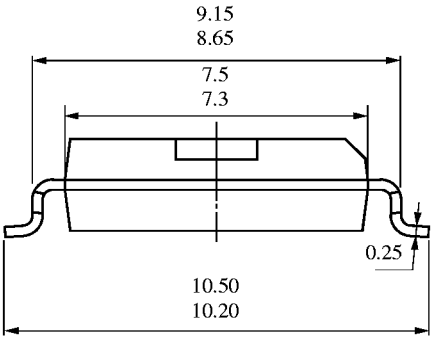
technical drawings
according to DIN
specifications

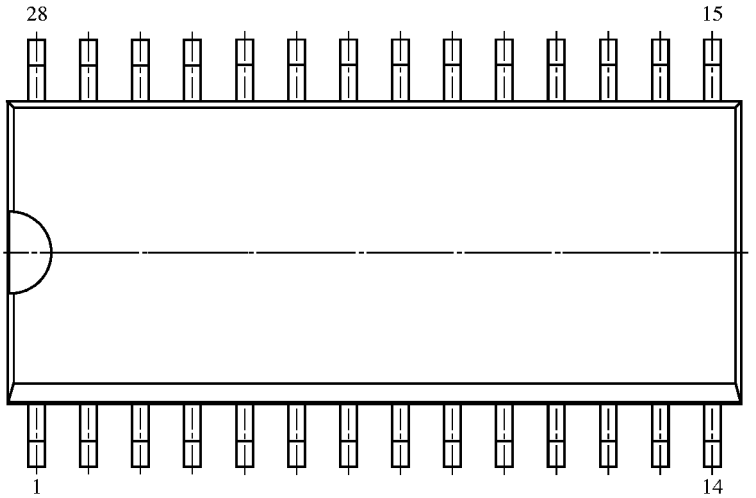
13028

Package SO28

Dimensions in mm







technical drawings
according to DIN
specifications

13033

Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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