Frequency Synthesizer for TV and VCR Tuner with UNIVERSAL BUS

Features

- 1.3 GHz divide-by-8 prescaler integrated (can be bridged)
- EASY LINK INTERFACE to MOSMIC and MIXER-IC
- UNIVERSAL BUS: I²C-bus **or** 3-wire-bus
  I²C-bus software compatible to U6204B
  3-wire-bus software compatible to U6359B
- I²C-Bus Mode: 3 bidirectional ports (open collector)
  5 level ADC or unidirectional port (open collector)
  3 addresses selectable at pin 10 and
  1 address fixed for multituner application
- 3-Wire Bus Mode: 3 unidirectional output ports (open collector)
  Lock output (open collector)
- Low power consumption (typ. 5 V/35 mA)
- Electrostatic protection according to MIL-STD 883
- SO-16 small package

Block Diagram

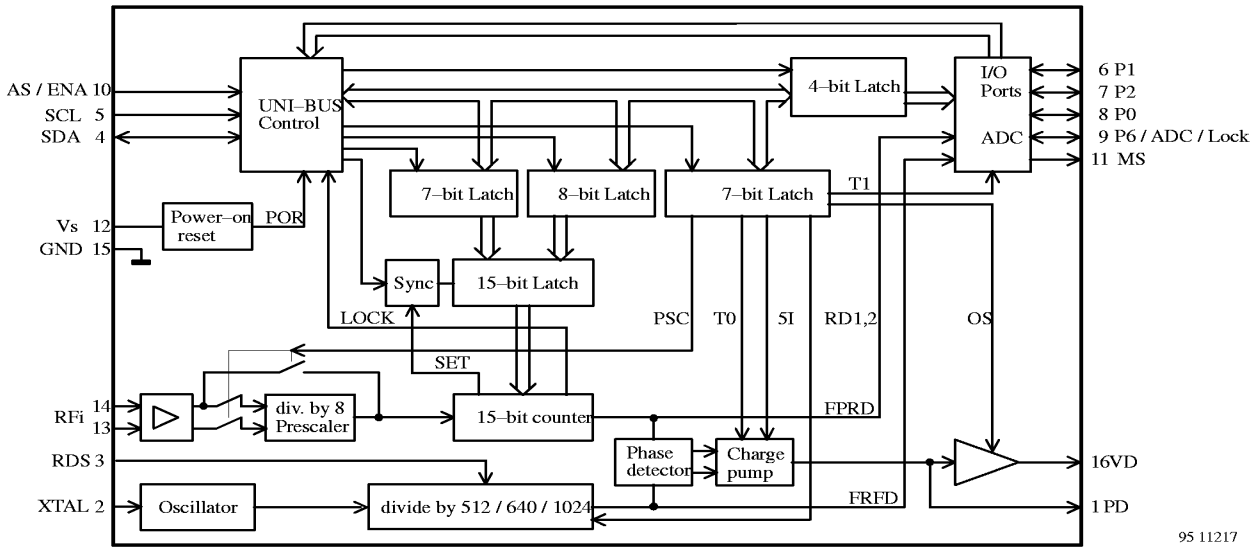
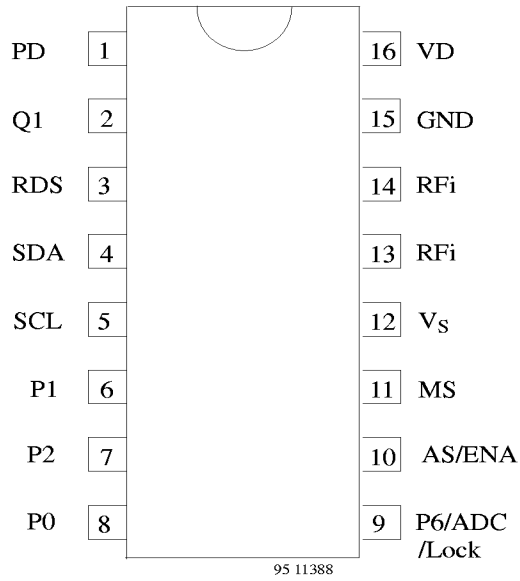


Figure 1.

U6224B-AFP

Pin Description



Pin	Symbol	Function
1	PD	Charge pump output
2	Q1	XTAL
3	RDS	Reference divider select input
4	SDA	Data input/output
5	SCL	Clock input
6	P1	Input/output port
7	P2	Input/output port
8	P0	Input/output port
9	P6/ADC/ Lock	Port output/ADC-input/Lock output
10	AS/ENA	Address select/Enable input
11	MS	Mixer switch output
12	Vs	Supply voltage
13	RFi	RF input
14	RFi	RF input
15	GND	Ground
16	VD	Active filter output

Description

The U6224B is a single chip PLL designed for TV and VCR receiver systems. It consists of a bridgeable divide-by-8 prescaler with an integrated preamplifier, a 15 bit programmable divider, a crystal oscillator and a reference divider with three selectable divider ratios (÷512/÷640/÷1024), a phase/frequency detector together with a charge-pump, which is driving the tuning amplifier. Only one external transistor is required for varactor line driving. The device can be controlled via I^2C-bus format or 3-wire-bus format. It detects automatically which bus format is received, therefore there is no need for a bus selection pin. In I^2C-bus mode the device has one fixed I^2C-bus address and three programmable addresses, programmed by applying a specific input voltage to the address select input, enabling the use of up to three synthesizers in a system. This pin serves in 3-wire-bus mode as the enable signal input. There are four open collector outputs for switching functions available. In 3-wire-bus mode there are three open collector outputs and one serves as Locksignal output. The logic of the output ports P0-2 is inverted in order to drive without change in software gate 1 of MOSMIC prestages directly. This feature removes the formerly external pnp switching transistors. All open collector outputs are capable of sinking at least 10 mA. The MS output is provided to control directly a mixer-oscillator IC in combination with the output port P0-2 state. In I^2C-bus mode there is an Analog-to-Digital Converter available for digital AFC control applications and the ports P0-2 can be used as inputs.

Functional Description

The U6224B is programmed via 2-wire I^2C-bus or 3-wire-bus depending on the received data format. The three bus inputs pin 4, 5, 10 are used as SDA, SCL and address select inputs in I^2C-bus mode or as data, clock and enable inputs in 3-wire-bus mode. The data includes the scaling factor SF and switching output information. In I^2C-bus mode there are some additional functions available (ADC, bidirectional ports, etc.).

Oscillator frequency calculation:
f_{VCO} = PSF * SPF * f_{refosc}/SRF

f_{VCO}: Locked frequency of voltage controlled oscillator

PSF: Scaling factor of prescaler (÷1 or ÷8 in I^2C-/÷8 in 3-wire-bus mode)

SPF: Scaling factor of programmable divider (15 bit in I^2C-/14 bit in 3-wire-bus mode)

SRF: Scaling factor of reference divider (÷512/÷640/÷1024)

f_{refosc}: Reference oscillator frequency: 3.2/4 MHz crystal or external reference frequency

The input amplifier together with a divide-by-8 prescaler gives an excellent sensitivity (see 'TYPICAL PRESCALER INPUT SENSITIVITY'). The input impedance is shown in the diagram 'TYPICAL INPUT IMPEDANCE'. When a new divider ratio according to the requested f_{VCO} is entered, the phase detector and charge

pump together with the tuning amplifier adjusts the control voltage of the VCO until the output signals of the programmable divider and the reference divider are in frequency and phase locked. The reference frequency may be provided by an external source capacitively coupled into pin 2, or by using an on-board crystal with an 18 pF capacitor in series. The crystal operates in the series resonance mode. The reference divider division ratio is selectable to ÷512/÷640/÷1024. Therefore with a 4 MHz crystal and the nominal division ratio of 512 of the reference divider the comparison frequency is 7.8125 kHz, which gives 62.5 kHz steps for the VCO, or with a 3.2 MHz crystal respectively 6.25 kHz comparison frequency and 50 kHz VCO step size. In I^2C-bus mode the division ratio may be set via two bits, in 3-wire-bus mode via a voltage at pin 3. In addition there are port outputs available for band switching and other purposes.

Application

A typical application is shown on page 14. All input/output interface circuits are shown on pages 12 and 13. Some special features which are related to test- and alignment procedures for tuner production are explained in the following bus mode description.

Absolute Maximum Ratings

All voltages are referred to GND (pin 15).

Parameters	Test Conditions / Pins		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Pin 12	Vs	–0.3		6	V
RF input voltage		Pin 13, 14	RFi	–0.3		Vs+0.3	V
Xtal input voltage		Pin 2	Q1	–0.3		Vs+0.3	V
Charge pump output voltage		Pin 1	PD	–0.3		Vs+0.3	V
Active filter output voltage		Pin 16	VD	–0.3		Vs+0.3	V
Bus input/output voltage		Pin 4, 5	VSDA, VSCL	–0.3		6	V
SDA output current	open collector	Pin 4	ISDA	–1		5	mA
Address select/ENA input		Pin 10	VAS/ ENA	–0.3		Vs+0.3	V
Port output current	open collector	Pin 6-9	P0-2, P6	–1		15	mA
Total port output current	open collector	Pin 6-9	P0-2, P6	–1		50	mA
Port input/output voltage	in off state	Pin 6-9	P0-2, P6	–0.3		15	V
Port output voltage	in on state	Pin 6-9	P0-2, P6	–0.3		6	V
Junction temperature			Tjmax	–40		125	°C
Storage temperature			Tstor	–40		125	°C

Operating Range

All voltages are referred to GND (pin 15).

Parameters	Test Conditions / Pins		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Pin 12	Vs	4.5	5	5.5	V
Ambient temperature			Tamb	0		70	°C
Input frequency	PSC = 1	Pin 13, 14	RFi	80		1300	MHz
Input frequency	PSC = 0	Pin 13, 14	RFi	1		220	MHz
Programmable divider	I^2C-bus mode		SF	256		32767	
Programmable divider	3-wire-bus mode		SF	256		16383	
Xtal oscillator		Pin 2	fXtal	3	4	4.48	MHz
Thermal resistance	SO-16 small		Rthja			110	K/W

Electrical Characteristics

Test conditions (unless otherwise specified): Vs = 5 V, Tamb = 25 °C

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply current (prescaler on)	P0-2 = 1; P6 = 0; PSC =1 Pin 12	Is		35		mA
Supply current (prescaler off)	P0-2 = 1; P6 = 0; PSC =0 Pin 12	Is		21		mA
Input sensitivity						
f_{RFi} = 80-1000 MHz	PSC =1 Pin 13	Vi [1]	10		315	mVrms
f_{RFi} = 1300 MHz	PSC =1 Pin 13	Vi [1]	40		315	mVrms
f_{RFi} = 10-220 MHz	PSC =0 Pin 13	Vi [1]	10		315	mVrms
Crystal oscillator						
Recommended crystal series resistance			10		200	Ω
Crystal oscillator drive level	Pin 2			50		mVrms
Crystal oscillator source impedance	Nominal spread ±15 % Pin 2			–650		Ω
External reference input frequency	AC coupled sinewave Pin 2		3		4.5	MHz
External reference input amplitude	AC coupled sinewave Pin 2		70		200	mVrms
Port outputs/lock output (open collector), Lock condition: low, P0-2, P6, Lock						
Leakage current	VH = 13.5 V Pins 6-9	IL			10	µA
Saturation voltage	IL = 10 mA Pins 6-9	VSL [2]			0.5	V
Port inputs (P0-2)						
Input voltage high	Pins 6-8	Vi'H'	2.7			V
Input voltage low	Pins 6-8	Vi'L'			0.8	V
Input current high	Vi'H' = 13.5 V Pins 6-8	Ii'H'			10	µA
Input current low	Vi'L' = 0 V Pins 6-8	Ii'L'	–10			µA
ADC input (ADC), see page 7 for ADC-levels						
Input current high	Vi'H' = 13.5 V Pin 9	Ii'H'			10	µA
Input current low	Vi'L' = 0 V Pin 9	Ii'L'	–10			µA
Charge pump output (PD)						
Charge pump current 'H'	5I = 1, VPD = 1.7 V Pin 1	IPDH		±180		µA
Charge pump current 'L'	5I = 0, VPD = 1.7 V Pin 1	IPDL		±50		µA
Charge pump leakage current	TO = 1, VPD = 1.7 V Pin 1	IPDTRI		±5		nA
Charge pump amplifier gain	Pin 1, 16			6400		

Notes: 1) RMS-voltage calculated from the measured available power on 50 Ω.
2) Tested with one port active. The collector voltage of an active port may not exceed 6 V.

Parameters	Test Conditions / Pins		Symbol	Min.	Typ.	Max.	Unit
Bus inputs (SDA, SCL)							
Input voltage high		Pin 4, 5	Vi'H'	3		5.5	V
Input voltage low		Pin 4, 5	Vi'L'			1.5	V
Input current high	Vi'H' = Vs	Pin 4, 5	Ii'H'			10	µA
Input current low	Vi'L' = 0 V	Pin 4, 5	Ii'L'	–20			µA
Output voltage SDA (open collector)	ISDA'L' = 3 mA	Pin 4	VSDA 'L'			0.4	V
Address selection/Enable input (AS/ENA)							
Input current high	Vi'H' = Vs	Pin 10	Ii'H'			10	µA
Input current low	Vi'L' = 0 V	Pin 10	Ii'L'	–10			µA
Mixer switch output (MS)							
Output voltage band A	I MS = –20 µA	Pin 11	V MSA	0	0.25	1	V
Output voltage band B	I MS = –20 µA	Pin 11	V MSB	1.6	0.4*Vs	2.4	V
Output voltage band C	I MS = –20 µA	Pin 11	V MSC	Vs–1	Vs–.75	Vs	V

I²C-Bus Description

Functional Description

When the U6224B is controlled via 2-wire I²C-bus format, then data and clock signals are fed into the SDA and SCL lines respectively. Depending on the LSB of the address byte the device can be either accept new data (write mode: LSB = 0) or send data (read mode: LSB = 1). The device has one fixed and three programmable I²C-bus addresses. The tables 'I²C-BUS WRITE DATA FORMAT' and 'I²C-BUS READ DATA FORMAT' describe the format of the data and show how to select the device address by applying a voltage at Pin 10.

Write Mode (Address byte LSB = 0)

When write mode is activated and the correct address is received, the SDA line is pulled low by the device during the acknowledge period, and then also during the acknowledge periods, when additional data bytes are programmed. After the address transmission (first byte), data bytes can be sent to the device. There are four data bytes requested to fully program the device. Once the correct address is received and acknowledged, the first bit of the following byte determines whether that byte is interpreted as byte 2 or 4; a logic 0 for divider information and a logic 1 for control and port output information. When byte 2 was received the device always expects byte 3 next. Likewise when byte 4 was received, byte 5 is expected. Additional data bytes can be entered without the need to re-address the device to the device until an I²C-bus stop condition is recognised. This allows a smooth frequency sweep for fine tuning AFC purposes. The table 'I²C-BUS PULSE DIAGRAM' shows some possible data transfer examples.

The programmable divider bytes PDB1 and PDB2 are controlling the division ratio of the 15 bit programmable divider. They are loaded in a 15 bit latch after the 8th clock pulse of the second divider byte PDB2, the control and the port register latches are loaded after the 8th clock pulse of the control byte CB1 resp. port byte CB2.

The control byte CB1 allows to control the following special functions:

- 5I-bit switches between low and high charge pump current
- T1-bit enables divider test mode when it is set to logic 1
- T0-bit allows to disable the charge pump when it is set to logic 1
- PSC-bit switches prescaler off when it is set to logic 0
- RD1 and RD2-bit allow to select the reference divider ratio
- OS-bit disables the charge pump drive amplifier output when it is set to logic 1.

Only in I²C-bus mode the charge pump current can be controlled. In 3-wire-bus mode there is always the high charge pump current active.

The OS-bit function disables the complete PLL function. This allows the tuner alignment by supplying the tuning voltage directly through the 30 V supply voltage of the tuner.

The control byte CB2 programs the port outputs P0-2 and P6; for the MOSMIC ports P0-2 a logic 1 for high impedance output (off) or a logic 0 for low impedance output and for the standard port P6 a logic 0 for high impedance output (off) or a logic 1 for low impedance output (on). At power-on the MOSMIC ports P0-2 are set to low impedance state and the standard port P6 to high impedance state.

Description	I²C-BUS WRITE DATA FORMAT								
	MSB								LSB
Address byte	1	1	0	0	0	AS1	AS2	**0**	A
Progr. divider byte 1	0	n14	n13	n12	n11	n10	n9	n8	A
Progr. divider byte 2	n7	n6	n5	n4	n3	n2	n1	n0	A
Control byte 1	1	5I	T1	T0	PSC	RD2	RD1	OS	A
Control byte 2	X	P6	X	X	X	P2	P1	P0	A
A = Acknowledged; X = not used; unused bits of controlbyte 2 should be 0 for lowest power consumption.									

n0 ... n14: Scaling factor (SF) SF = 16384 * n14 + 8192 * n13 + ... + 2 *n1 + n0

PSC: Prescaler on/off PSC = 1: prescaler on PSC = 0: prescaler off

T0, T1: Testmode selection
T1 = 1: divider test mode on fPRD at pin 6, fRFD at pin 7
T1 = 0: divide test mode off
T0 = 1: charge pump disable
T0 = 0: charge pump enable

P0-2: Port outputs (for MOSMIC'S) P0, 1, 2 = 0: open collector active for **MOSMIC gate 1 logic**

P6: Port outpus P6 = 1: open collector active

5I: Charge pump current switch 5I = 1: high current 5I = 0: low current

OS: Output switch OS = 1: varicap drive disable OS = 0: varicap drive enable

RD1, RD2: Reference divider selection	RD2	RD1	Reference divider ratio
	X	0	640
	0	1	1024
	1	1	512

AS1, AS2: Address selection pin 10	AS1	AS2	Address	Dec. value	Voltage at pin 10
	0	1	1	194	always valid
	0	0	2	192	0 to 10 % Vs
	1	0	3	196	40 to 60 % Vs
	1	1	4	198	90 % Vs to 13.5 V

Mixer-switch output levels:	P2	P1	P0	MS output voltage	TFK MIXER IC's band selection
	0	1	0	< 0.25 V	Band A
	1	0	0	0.4 * Vs	Band B
	0	0	1	Vs – 0.75 V	Band C

Read Mode (Address byte LSB = 1)

After the address transmission (first byte), the status byte can be read from the device on the SDA line (MSB first). Data is valid on the SDA line during logic high of the SCL signal. The controller accepting the data has to pull the SDA line to low-level during all status byte acknowledge periods to read another status byte. If the controller fails to pull the SDA line to low-level during this period, the device will then release the SDA line to allow the controller to generate a STOP condition.

The POR-bit (power-on-reset) is set to a logic 1 when the supply voltage Vs of the device has dropped below 3 V (at 25 °C) and also when the device is initially turned on. The POR-bit is reset to a logic 0 when the read sequence is terminated by a STOP condition. When POR-bit is set high (at low Vs) it is indicated that all the programmed information is lost and the port outputs are all set to high impedance state.

The FL-bit indicates whether the loop is in phase lock condition (logic 1) or not (logic 0).

If the ADC or the ports are to be used as inputs the corresponding outputs must be programmed to a high impedance state (logic 1).

The bits I2, I1 and I0 show the status of the I/O ports P0, P1 and P2 respectively. A logic 0 indicates a LOW level and a logic 1 a HIGH level (TTL levels).

The bits A2, A1 and A0 represent the digital information of the 5 level ADC. This converter can be used to feed AFC information to the controller from the IF section of the receiver, as shown in the typical application circuit on page 14.

Description	I^2C-BUS READ DATA FORMAT								
	MSB							LSB	
Address byte	1	1	0	0	0	AS1	AS2	**1**	A
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	–

POR: Power-on-reset flag: POR = 1 on power on

FL: in-lock flag: FL = 1, when loop is phase locked

I2, I1, I0: digital information of I/O-ports P0, P1 and P2 respectively

A2, A1, A0: digital data of the 5-level ADC. see next table

A/D Converter Levels:	A2	A1	A0	Input voltage to ADC pin 9
	1	0	0	60 % Vs to 13.5 V
	0	1	1	45 % to 60 % Vs
	0	1	0	30 % to 45 % Vs
	0	0	1	15 % to 30 % Vs
	0	0	0	0 V to 15 % Vs

I²C-Bus Pulse Diagram

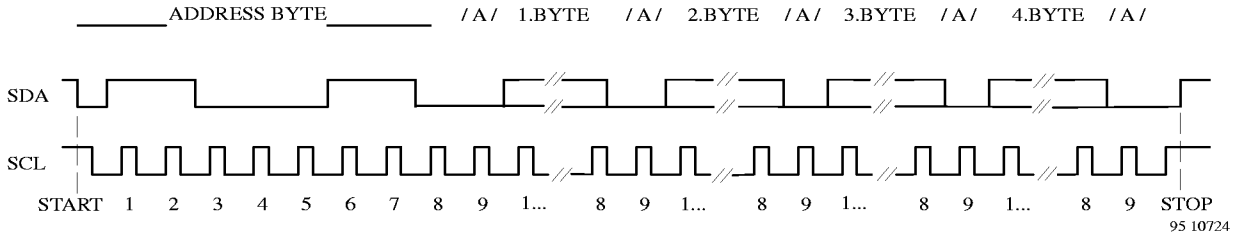


Figure 2.

Data transfer examples	Description	
START – ADR – PDB1 – PDB2 – CB1 – CB2 – STOP	START =	Start condition
START – ADR – CB1 – CB2 – PDB1 – PDB2 – STOP	ADR =	Address byte
START – ADR – PDB1 – PDB2 – CB1 – STOP	PDB1 =	Progr. divider byte 1
START – ADR –PDB1 – PDB2 –STOP	PDB2 =	Progr. divider byte 2
START –ADR – CB1 – CB2 – STOP	CB1 =	Control byte 1
START – ADR – CB1 –STOP	CB2 =	Control byte 2
	STOP =	Stop condition

I²C-Bus Timing

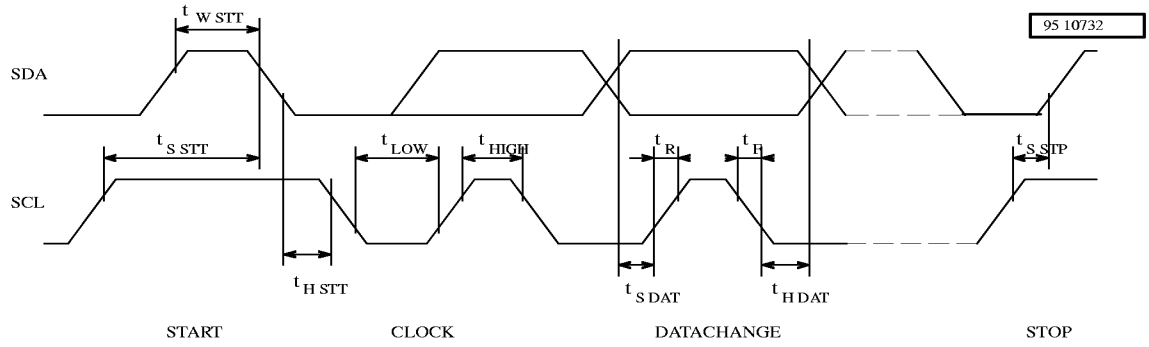


Figure 3.

Parameters	Test Conditions / Pins	Symbol	Min.	Max.	Unit
Rise time SDA, SCL		tR		15	µs
Fall time SDA, SCL		tF		15	µs
Clock frequency SCL		fSCL	0	100	kHz
Clock 'H' pulse		tHIGH	4		µs
Clock 'L' pulse		tLOW	4		µs
Hold time start		tH STT	4		µs
Waiting time start		tW STT	4		µs
Setup time start		tS STT	4		µs
Setup time stop		tS STP	4		µs
Setup time data		tS DAT	0.3		µs
Hold time data		tH DAT	0		µs

3-Wire-Bus Description

When the U6224B is controlled via 3-wire-bus format, then data, clock and enable signals are fed into the SDA, SCL and AS/ENA lines respectively. The diagram '3-WIRE-BUS PULSE DIAGRAM' shows the data format. The data consist of a single word, which contains the programmable divider (14 bit) and port information. Bit no. 15 of the programmable divider is always zero, when 3-wire bus mode is active. Only during the enable high period the data is clocked into the internal data shift register on the negative clock transition. During enable low periods the clock input is disabled. New data words are only accepted by the internal data latches from the shift register on a negative transition of the enable signal when exactly eighteen clock pulses were sent during the high period of the enable. The data sequence and the timing is described in the following diagrams.

In 3-wire-bus mode pin 9 becomes automatically the Locksignal output. An improved lock detect circuit generates a flag when the loop has attained lock. 'In lock' is indicated by a low impedance state (on) of the open collector output.

In 3-wire-bus mode the following conditions are set internally:

- 5I = 1: always high charge pump current active
- T1 = 0: divider test mode off
- T0 = 0: charge pump enable
- RD1, 2 = X: reference divider ratio is selected through RDS input
- PSC = 1: prescaler on
- OS = 0: varicap enable

In 3-wire-bus mode the division ratio of the reference divider may be selected by applying an appropriate voltage at the RDS input pin 3.

RDS: Reference divider selection pin 3	Reference divider ratio	Voltage at pin 3
	1024	0 to 10 % Vs
	512	open or 40 to 60 % Vs
	640	90 to 100 % Vs

The complete PLL function can be disabled by programming a normally not used division ratio of zero. This allows the tuner alignment by supplying the tuning voltage directly through the 30 V supply voltage of the tuner.

3-Wire-Bus Pulse Diagram

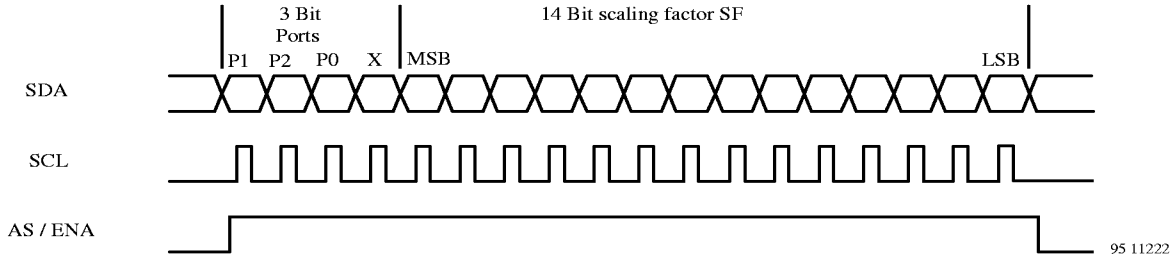


Figure 4.

3-Wire-Bus Timing

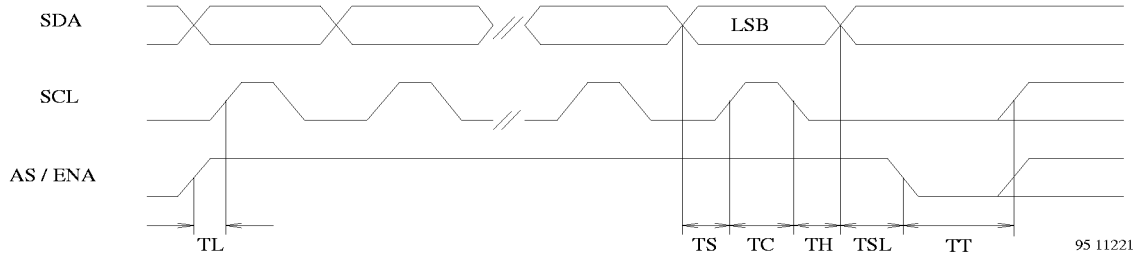


Figure 5.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Setup time		TS	2			µs
Enable hold time		TSL	2			µs
Clock width		TC	2			µs
Enable setup time		TL	10			µs
Enable between two transmissions		TT	10			µs
Data hold time		TH	2			µs

Typical Prescaler Input Sensitivity (Prescaler on: PSC = 1)

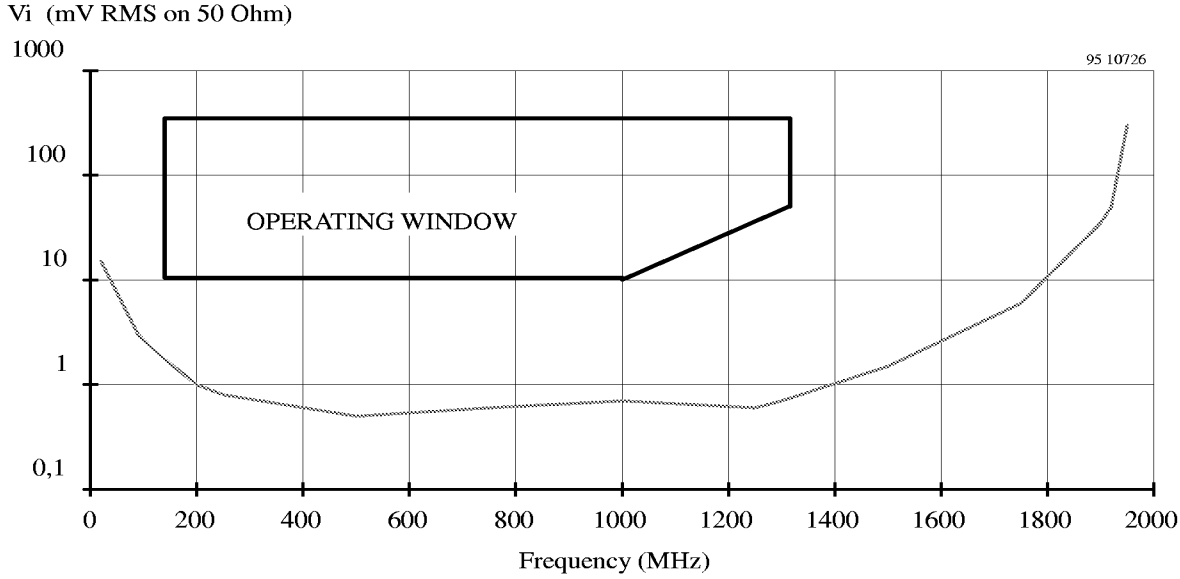


Figure 6.

Typical Prescaler Input Sensitivity (Prescaler off: PSC = 0)

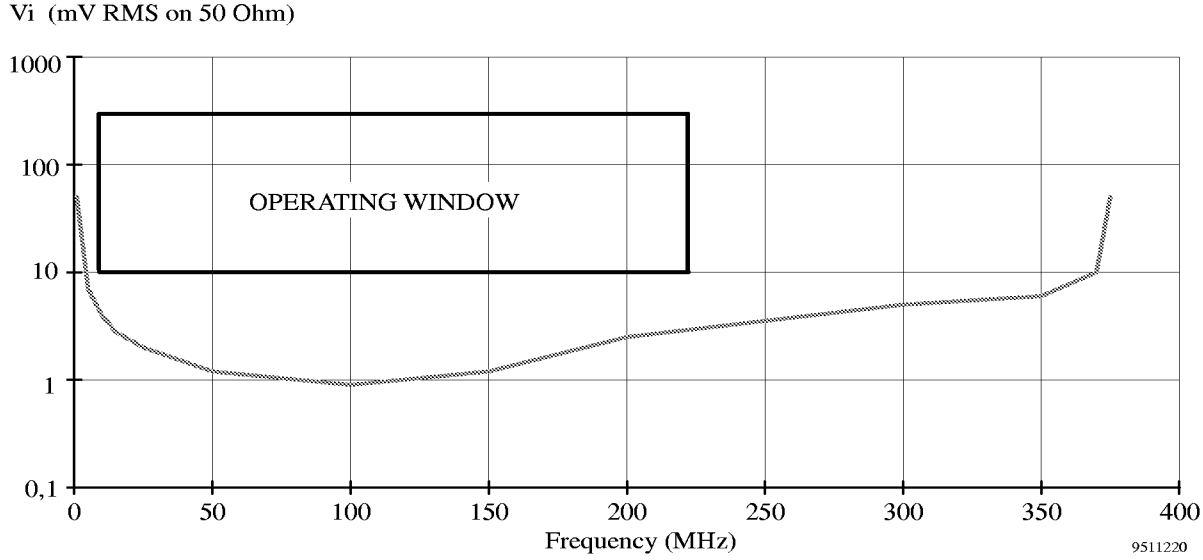


Figure 7.

Input/Output Interface Circuits

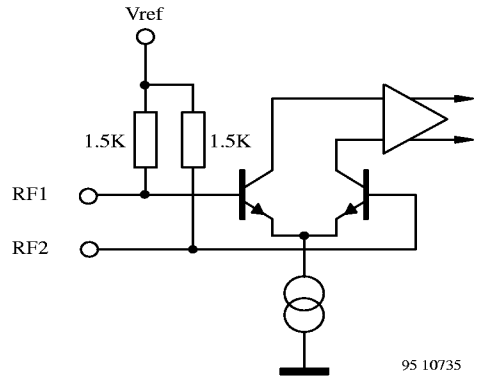


Figure 8. RF Input

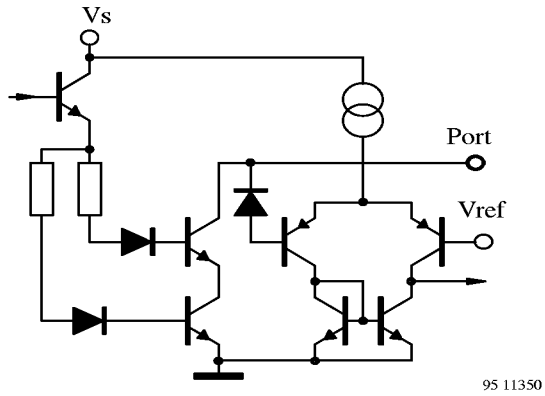


Figure 11. Ports

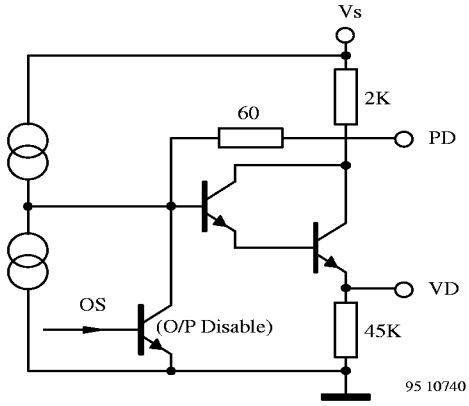


Figure 9. Loop amplifier

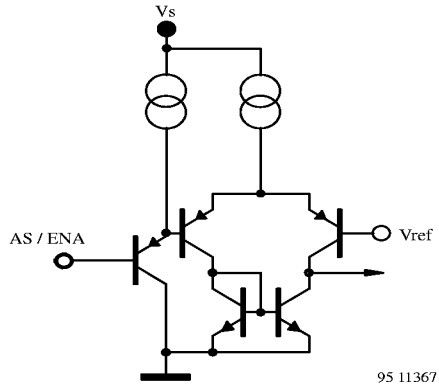


Figure 12. Address select/ Enable input

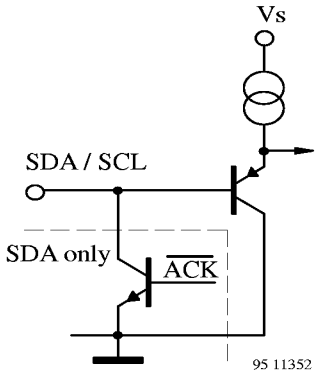


Figure 10. SCL and SDA input

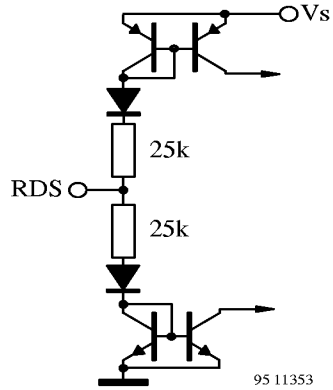


Figure 13. Reference divider select input

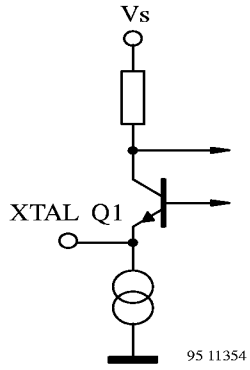


Figure 14. Reference oscillator

Typical Input Impedance

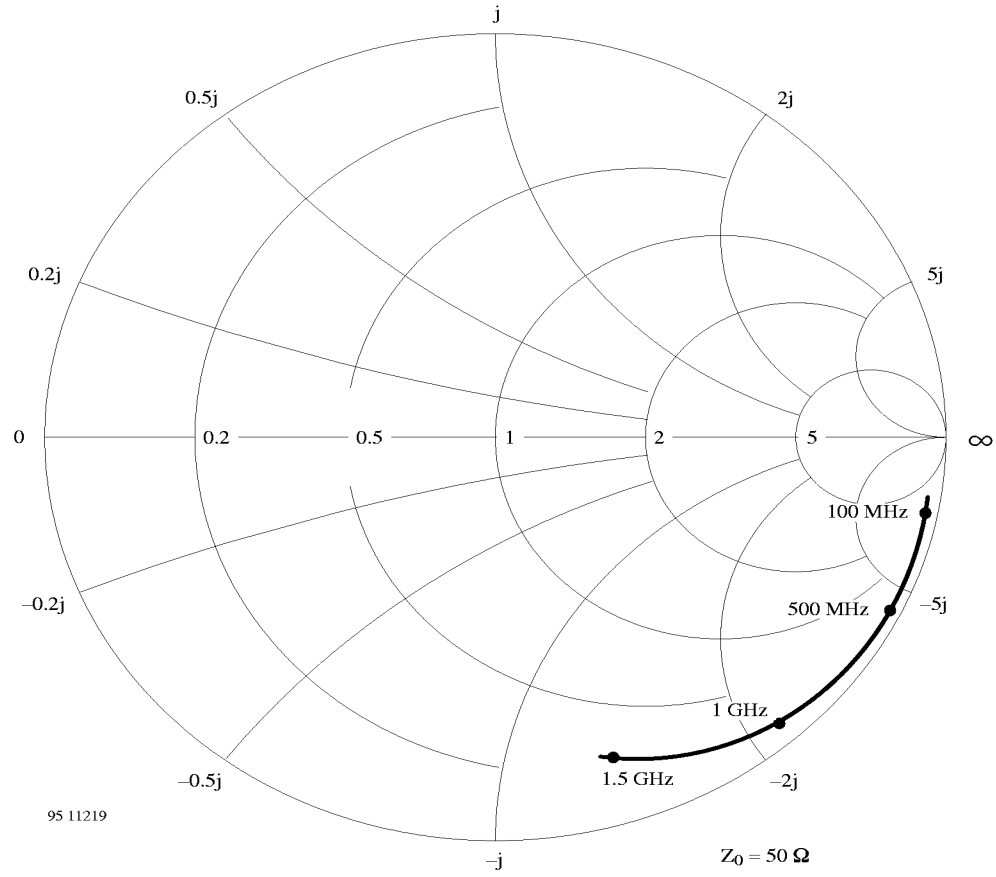


Figure 15.

Application Circuit

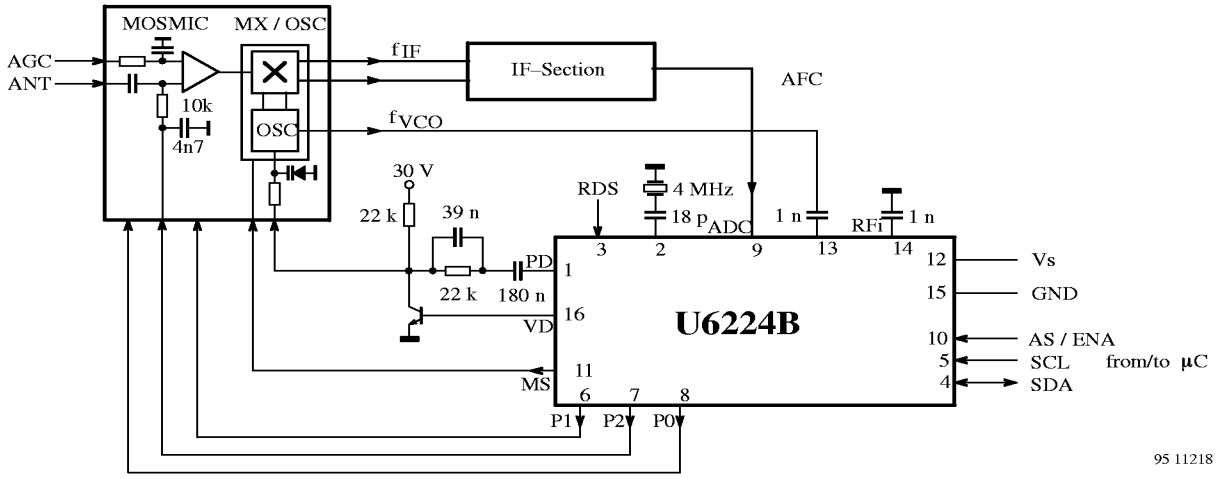


Figure 16.

Dimensions in mm

Package SO-16 small