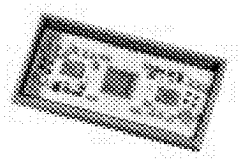
ILC DATA DEVICE CORPORATION®

BUS-65153



MIL-STD-1553B, NOTICE 2 AND MIL-STD-1760B SMALL TERMINAL INTERFACE CIRCUIT "STIC"

DESCRIPTION

The BUS-65153 is a complete, dual redundant MIL-STD-1553B Remote Terminal. Packaged in a 1.9" x 1.0" x 0.2", 70-pin ceramic package, the BUS-65153 provides the transmitter voltage level required by MIL-STD-1760. Also in support of MIL-STD-1760, the RT address inputs are latchable.

The BUS-65153 contains two low power transceivers and a DDC custom designed chip. This chip includes dual encoder/decoder, RT protocol logic, tri-state data buffers, and DMA transfer control logic. The BUS-65153 supports all 13 dual redundant mode codes, any combination of which may be illegalized by an external PROM, PLD, or RAM device.

Parallel data transfers are accomplished via a DMA type interface. Both 8-bit and 16-bit transfers are supported.

The BUS-65153 can be easily interfaced to most CPU's. In addition, the BUS-65153 can interface directly to minimum complexity subsystems such as switches, D/A converters, etc.

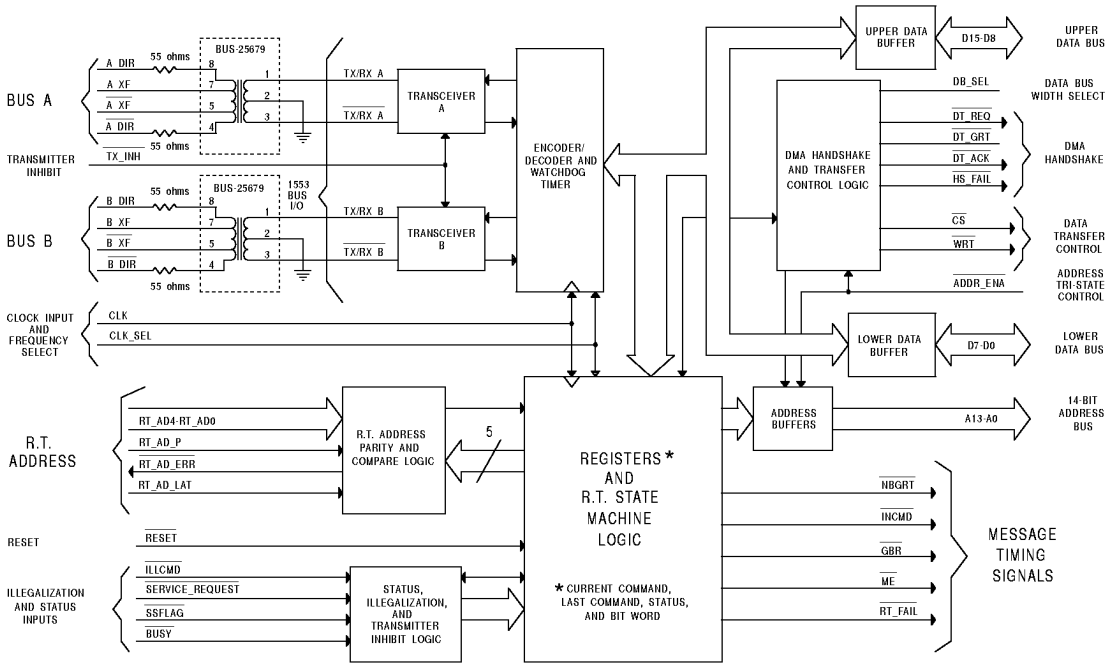
The address bus and transfer control signals may be configured for either two-state or three-state operation. Use of the three-state address mode reduces the number of external components required for a DMA processor interface.

The input clock frequency is user selectable for either 12 or 16 MHz. In the 12 MHz mode, the decoder operates at 24 MHz, providing superior word error rate and zero crossing distortion tolerance. The Busy, Service Request, and Subsystem Flag RT Status Word bits are provided as discrete pins, allowing for easy access by the subsystem.

Various message timing and error flag indicators are provided to facilitate the subsystem interface.

FEATURES

- ***Supports MIL-STD-1553B Notice 2 and MIL-STD-1760 Stores Management***
- ***Complete Integrated Remote Terminal Including:***
  - ***Dual Low-Power Transceiver***
  - ***Complete RT Protocol Logic***
- ***Small, 70-Pin Ceramic Package***
- ***Meets 1553A/McAir Response Time Requirements***
- ***Selectable 8/16-bit DMA Interface***
- ***Optional Tri-State Address Bus and Transfer Control Signals***
- ***Direct Interface to Simple Systems***
- ***Selectable Input Clock, 12 or 16 MHz***
- ***MIL-PRF-38534 Processing Available***



Note: Transformers are external

FIGURE 1. BUS-65153 BLOCK DIAGRAM

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TABLE 1. BUS-65153 SPECIFICATIONS				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
ABSOLUTE MAXIMUN RATINGS				
Supply Voltage				
■ Logic + 5V	- 0.3		7.0	V
Transceiver + 5 V	- 0.5		7.0	V
■ - 15 V	+ 0.3		- 18.0	V
■ - 12 V	+ 0.3		- 18.0	V
Logic				
■ Voltage Input Range	- 0.5		Vcc+0.5	V
RECEIVER				
Differential Input Resistance				
■ (Bus-65153, Bus-65163, BUS- 65154, Bus-65164) (Notes 1 - 6)	11			kΩ
Differential Input Capacitance				
■ (Bus-65153, Bus-65163, BUS-65154, Bus-65164) (Notes 1 - 6)			10	pF
Threshold Voltage, Transformer Coupled, Measured on Stub	0.500		0.860	V_{P-P}
Common Mode Voltage (Note 7)			10	V_{PEAK}
TRANSMITTER				
Differential Output Voltage				
■ Direct Coupled Accross 35 ohms, Measured on Bus	6		9	V_{P-P}
■ Direct Coupled Accross 70 ohms Measured on Stub				
• BUS-65153, BUS-65163 (Note 10)	20	22	27	V_{P-P}
• BUS-65154, BUS-65164	18	21	27	V_{P-P}
Output Noise, Differential (Direct Coupled)			10	mV P-P,diff
Output Offset Voltage, Transformer Coupled Accross 70 Ohms	-250		250	mV
Rise/Fall Time	100	150	300	nsec
LOGIC				
V_{IH}	2.0			V
V_{IL}			0.8	V
I_{IH} (V_{IN}=V_{CC})	-20		20	µA
I_{IL} (V_{IN}=GND)	-20		20	µA
V_{OH} (I_{OH} = 0)	Vcc+0.4			V
V_{OH} (I_{OH} = max)	3.7			V
V_{OL} (I_{OL} = 0)			0.4	V
V_{OL} (I_{OL} = min)			0.5	V
I_{OL}	-3.4			mA
I_{OH}			3.4	mA
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances (BUS-65153, BUS-65163)				
■ + 5 V (Logic)	4.5		5.5	V
■ + 5 V (CH A, CH B)	4.5		5.5	V
■ - 15 V (CH A, CH B)	-15.75		-14.25	V
Voltages/Tolerances (BUS-65154, BUS-65164)				
■ + 5 V (Logic)	4.5		5.5	V
■ + 5 V (CH A, CH B)	4.5		5.5	V
■ - 12 V (CH A, CH B)	-12.6		-11.4	V
Current Drain (BUS-65153, BUS-65163, Note 9)				
■ + 5 V Logic (CH A, CH B)		65	115	mA
■ - 15 V (CH A, CH B)				
• Idle	5	20	50	mA
• 25% Duty Cycle		55	112	mA
• 50% Duty Cycle		90	175	mA
• 100% Duty Cycle		160	300	mA

TABLE 1. BUS-65153 SPECIFICATIONS				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
POWER SUPPLY REQUIREMENTS (CONTINUED)				
Current Drain (BUS-65154, BUS-65164, Note 9)				
■ + 5 V Logic (CH A, CH B)		65	115	mA
■ - 12 V (CH A, CH B)				
• Idle		30	60	mA
• 25% Duty Cycle		87	120	mA
• 50% Duty Cycle		135	185	mA
• 100% Duty Cycle		230	305	mA
POWER DISSIPATION				
BUS-65153, BUS-65163				
■ Total Hybrid				
• Idle		0.625	1.325	W
• 25% Duty Cycle		0.850	1.963	W
• 50% Duty Cycle		1.075	2.600	W
• 100% Duty Cycle		1.525	3.875	W
■ Hottest Die				
• Idle		0.335	0.68	W
• 25% Duty Cycle		0.600	1.06	W
• 50% Duty Cycle		0.860	1.45	W
• 100% Duty Cycle		1.385	2.23	W
BUS-65154, BUS-65164				
■ Total Hybrid				
• Idle		0.685	1.295	W
• 25% Duty Cycle		0.985	1.727	W
• 50% Duty Cycle		1.285	2.160	W
• 100% Duty Cycle		1.885	3.035	W
■ Hottest Die				
• Idle		0.290	0.59	W
• 25% Duty Cycle		0.590	0.92	W
• 50% Duty Cycle		0.890	1.36	W
• 100% Duty Cycle		1.490	2.16	W
CLOCK INPUT				
Frequency				
■ Nominal Value (Selectavle)				
• CLOCKSEL Input = Logic '0'		16.0		MHz
• CLOCKSEL Input = Logic '1'		12.0		MHz
■ Long Term Tolerance				
• 1553A Compliance			0.01	%
• 1553B Compliance			0.1	%
■ Short Term Tolerance, 1 Second				
• 1553A Compliance			0.001	%
• 1553B Compliance			0.01	%
Duty Cycle				
• 16 MHz		33	67	%
• 12 MHz		40	60	%
1553 MESSAGE TIMING				
RT Response Time				
• 16 MHz	6.00	6.5	6.96	µS
• 12 MHz	6.18	6.5	6.76	µS
RT-to-RT No Response Timeout (Note 8)	18.25	18.9	19.5	µS
Transmitter Watchdog Timeout		668		µS
THERMAL				
Thermal Resistance, Junction-to-Case, Hottest Die (θJC)				
■ BUS-65153, BUS-65163		5.54		°C/W
■ BUS-65154, BUS-65164		5.54		°C/W
Operating Junction Temperature	-55		160	°C
Storage Temperature	-65		150	°C
Lead Temperature (Soldering for 10 seconds)			+300	°C

TABLE 1. BUS-65153 SPECIFICATIONS				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
PHYSICAL CHARACTERISTICS				
Size				
■ 70-pin, DIP, Flat Pack	1.9 x 1.0 x 0.215 48.26 x 25.4 x 5.46			in (mm)
Weight				
■ 70-pin, DIP, Flat Pack		0.6 (17)		oz (gm)

Notes: Notes 1 through 6 are applicable to the Receiver Differential Resistance and Differential Capacitance specifications:
(1) Specifications include both transmitter and receiver (tied together internally).
(2) Measurement of impedance is directly between pins TX/RX A(B) and $\overline{\text{TX/RX A(B)}}$ of the BUS-65153 or BUS-65163 hybrid.
(3) Assuming the connection of all power and ground inputs to the hybrid.
(4) The specifications are applicable for both unpowered and powered conditions.
(5) The specifications assume a 2 volt rms balanced, differential, sinusoidal input. The applicable frequency range is 75 KHz to 1 MHz.
(6) Minimum resistance and maximum capacitance parameters are guaranteed,but not tested, over the operating range.
(7) Assumes a common mode voltage within the frequency range of dc to 2 MHz, applied to pins of the isolation transformer on the stub side (either direct or transformer coupled), referenced to hybrid ground. Use a DDC recommended transformer or other transformer that provides an equivalent minimum CMRR.
(8) RT-to-RT Timeout is measured from the Mid-Parity crossing of the Transmit Command word to the Mid-Sync crossing of the Transmitting RT Status word.
(9) Current drain is for total hybrid (e.g., +5V supply current includes the sum of logic +5V supply current, channel A +5V supply current and channel B +5V supply current). Transmitting duty cycles assume one channel transmitting and alternate channel idle.
(10) Compliant with 1760 applications.

INTRODUCTION

GENERAL

The BUS-65153 is a complete MIL-STD-1553 Remote Terminal (RT) bus interface unit. Contained in the hybrid are a dual trapezoidal transceiver and Manchester II encoder/decoder, and Remote Terminal (RT) protocol logic for MIL-STD-1553B. Also included are built-in self-test capability and a parallel subsystem interface. The subsystem interface includes a 14-bit address bus and a data bus that may be configured for either 8-bit or 16-bit DMA transfers.

The transceiver front end of the BUS-65153 is implemented by means of low-power bipolar analog monolithic and thick-film hybrid technology. The transceiver requires +5 V and -15 V only (no +15 V is required) and includes voltage source transmitters. The voltage source transmitters provide superior line driving capability for long cables and heavy amounts of bus loading. In addition, the monolithic transceivers provide a minimum stub voltage level of 20 volts peak-to-peak transformer coupled, making the BUS-65153 suitable for MIL-STD-1760 applications.

The receiver sections of the BUS-65153 are fully compliant with MIL-STD-1553B in terms of front end overvoltage protection, threshold and bit-error rate.

The BUS-65153 implements all MIL-STD-1553 message formats, including all 13 of the 1553B dual redundant mode codes. Any subset of the possible 1553 commands (broadcast, T/$\overline{\text{R}}$ bit, subaddress, word count/mode code) may be optionally illegalized by means of an external PROM, PAL, or RAM device. An extensive amount of message validation is performed for each message received. Each word received is validated for correct sync type and sync encoding, Manchester II encoding, parity, and bit count. All messages are verified to contain a legal, defined Command Word and correct word count. If the BUS-65153 is the receiving RT in an RT-to-RT transfer, it verifies that the T/$\overline{\text{R}}$ bit of the transmit Command Word is a one and that the transmitting RT responds in time and contains the correct RT address in its Status Word.

The 65153 may be operated from either a 12 MHz or 16 MHz clock input. In the 12 MHz mode, the decoder samples incoming data with **both** edges of the clock input. This, in effect, provides for 24 MHz decoder sampling. Benefits of the higher sampling rate include a wider tolerance for zero-crossing distortion and improved bit error rate performance.

The BUS-65153 includes a hardwired R.T. address input. This includes 5 address lines, an address parity input, and an address parity error output. The RT address can also be latched internally by means of the address latching input signal RT_ADD_LAT. The 65153 supports command illegalization. Commands may be illegalized by asserting the output signal $\overline{\text{ILLCMD}}$ low approximately 5 ms after the mid-parity bit zero-crossing of the received Command Word. Command Words may be illegalized as a function of broadcast, T/$\overline{\text{R}}$ bit, subaddress, word count and/or mode code.

An internal Built-in-Test (BIT) Word register is updated at the end of each message. The contents of the BIT Word Register are transmitted in response to a Transmit BIT Word Mode Command. The BUS-65153 provides a number of real-time output signals. These various signals provide indications of message start, message in progress, valid received message, message error, handshake fail, and looptest fail or transmitter timeout.

The BUS-65153 may be used in a wide variety of interface configurations. The 65153 has an 8/16-bit tri-state data bus and an address/control bus that may be pin programmed for either two-state or three-state operation. The three-state mode allows the BUS-65153 to be connected directly to the host processor's data, address, and control buses in a DMA configuration. The BUS-65153 includes standard DMA handshake signals (Request, Grant, and Acknowledge) as well as transfer control outputs ($\overline{\text{CS}}$ and $\overline{\text{WRT}}$). The DMA interface may operate in either a 16-bit or 8-bit mode, supporting both word-wide and byte-wide transfers.

The DMA interface also allows the 65153 to be interfaced directly to a simple system that doesn't have a microprocessor. This provides a low-cost 1553 interface for A/D and D/A converters, switch closures, and actuators.

The BUS-65153 may also be used in a shared RAM interface configuration. By means of tri-state buffers and a very small amount of “glue” logic, the 65153 will store Command Words and access Data Words to/from dedicated “mailbox” areas in a

shared RAM for each broadcast / T-$\overline{R}$ bit / subaddress / mode code.

If a more elaborate shared RAM interface is needed, the BUS-65153 may be interfaced to a BUS-66315 memory management unit. If a BUS-66315 is used, the address bus of the BUS-65153 is not used for accessing the system RAM (although the address outputs may still be used for command illegalizing).

The BUS-66315 provides an RT Lookup Table, allowing the mapping of the various T-R/subaddresses to user programmable areas in the BUS-66315's 64K x 16 shared RAM address space. The BUS-66315 also provides a stack area of RAM. The stack provides a chronology of all messages processed, storing a Block Status Word (message channel, completion, and validity information), an optional Time Tag Word and the received Command Word for each message processed. The BUS-66315 also provides maskable interrupts to the host processor for end-of-message and/or message error conditions.

ADDRESS MAPPING

The memory allocation scheme for the BUS-65153 14-bit address bus is defined as follows:

A13: BROADCAST/$\overline{\text{OWNADDRESS}}$
A12: TRANSMIT/$\overline{\text{RECEIVE}}$
A11-A7: SUBADDRESS 4-0
A6: DATA/$\overline{\text{COMMAND}}$
A5-A1: WORD COUNT/CURRENT WORD COUNT
A0: UPPER/$\overline{\text{LOWER}}$ BYTE (8-bit mode only)

The method of address mapping implemented by the BUS-65153 provides for a "mailbox" allocation scheme for the storage of Command and Data Words. The address outputs A13 through A1 map directly into 8K words (16K bytes) of processor address space. A0 is used for upper/lower byte selection in the 8-bit DMA mode. The same address map is applicable for both the DMA and shared RAM (without the BUS-66315) interface configurations. The BUS-65153's addressing scheme maps messages in terms of broadcast/own address, transmit/receive, subaddress, and mode code. A 64-word message block is allocated for each T/R-subaddress.

The received Command Word for all nonmode code messages is stored at relative word location zero (0) within the respective message block. For mode code messages, the address for the received Command Word is offset from location zero (0) within the message block for subaddress 0 or 31. The value of the address offset is equal to the mode code field of the respective Command Word (0 to 31).

For nonmode code messages, the Data Words to be transmitted or received are accessed from (to) relative locations 32 through 63 within the message block. For mode code messages with a single Data Word that is not read from internal register, the address for the Data Word is offest from location 32 within the 64-word message block for subaddresses 0 and 31. The value of the address offset is equal to the mode code field of the received Command Word.

The Data Words transmitted in response to Transmit Last Command or Transmit BIT Word mode commands are accessed from a pair of internal registers.

DMA INTERFACE

An 8/16-bit data bus, a 14-bit address bus, and six control signals are provided to facilitate communication with the parallel subsystem. The control signals include the standard DMA handshake signals $\overline{\text{DT_REQ}}$, $\overline{\text{DT_GRT}}$, $\overline{\text{DT_ACK}}$ as well as the transfer control outputs $\overline{\text{CS}}$ and $\overline{\text{WRT}}$. $\overline{\text{HS_FAIL}}$ provides an indication to the subsystem of a handshake failure condition.

Data is transferred between the subsystem and the BUS-65153 via a DMA handshake, initiated by the BUS-65153. A READ operation is defined to be the transfer of data from the subsystem to the BUS-65153. Conversely, a WRITE operation transfers data from the BUS-65153 to the subsystem.

If the BUS-65153 is in 16-bit mode, data is transferred as a single 16-bit word. In 8-bit mode, data is transferred in a pair of byte transfers within the same DMA handshake cycle. The upper byte is transferred first with A0=1, followed by the lower byte with A0=0.

HANDSHAKE FAIL

If the BUS-65153 (STIC) asserts $\overline{\text{DT_REQ}}$ and the subsystem does not respond with $\overline{\text{DT_GRT}}$ in time for the BUS-65153 to complete the word transfer, the HS_FAIL output will be asserted low to inform the subsystem of the handshake failure and bit D12 in the internal Built-In-Test (BIT) word is set to logic ©1." If the handshake failure occurs on a data word read transfer (transmit command) the STIC will abort the current message processing and **NOT** transmit erroneous data back to the bus controller. In the case of a handshake failure on a write transfer (receive command word transfer, transmit command transfer, or a receive data word transfer) the STIC will set the handshake failure output and BIT word bit, and continue processing the current message.

DMA READ OPERATION

Whenever the BUS-65153 needs to read a word from the subsystem, it asserts the signal $\overline{\text{DT_REQ}}$ low. If the subsystem asserts $\overline{\text{DT_GRT}}$ in time, the BUS-65153 will then assert A13 through A1 (and A0 for the 8-bit mode), WRT high, along with $\overline{\text{DT_ACK}}$ and $\overline{\text{CS}}$ low to enable data from the subsystem.

After the transfer of each Data Word has been completed, address bus outputs A5 through A1 are incremented. This provides the option of connecting the BUS-65153 address lines directly to the host processor's address bus to access the subsystem RAM, if desired.

DMA WRITE OPERATION

Whenever the BUS-65153 needs to transfer data to the subsystem, it initiates a DMA WRITE cycle. The BUS-65153 asserts $\overline{\text{DT_REQ}}$. The subsystem must respond with $\overline{\text{DT_GRT}}$.

If $\overline{\text{DT_GRT}}$ was received in time, the BUS-65153 will then assert $\overline{\text{DT_ACK}}$. The BUS-65153 will then assert A13 through A1 (and

A0 in 8-bit mode) and WRT low, followed by $\overline{CS}$ low. The subsystem may then use the rising edge of CS to latch the data. Similar to the DMA read operation, the address outputs A5 through A1 are incremented after the completion of a DMA WRITE operation.

MESSAGE PROCESSING OPERATION

Following the receipt and transfer of a valid Command Word, the BUS-65153 will attempt to (1) transfer received 1553 data to the subsystem, (2) read data from the subsystem for transmission on the 1553 bus, (3) transmit status (and possibly built-in-test) information to 1553, and/or (4) set status conditions.

The BUS-65153 responds to all nonbroadcast messages with a 1553 Status Word.

RT ADDRESS

RT Address (RT_AD 4-0, (RT_AD4 = MSB)) and RT Address Parity (RT_AD_P) should be programmed for a unique RT address and reflect an odd parity sum. The BUS-65153 will not respond to any MIL-STD-1553 commands or transfer received data from any nonbroadcast messages if an odd parity sum is not presented by RT_AD4-0 and RT_AD_P. An address parity error will be indicated by a low output on the $\overline{RT_AD_ERR}$ pin. The input signal RT_AD_LAT operates a transparent latch for RTAD4-RTAD0 and RTADP. If RT_AD_LAT is low the output of the latch tracks the value presented to the input pins. If RT_AD_LAT is high, the output of the internal latch becomes latched at the values presented when RT_AD_LAT was low.

COMMAND ILLEGALIZATION

The BUS-65153 provides for command illegalization. If a command is illegalized, the BUS-65153 will set the Message Error bit and transmit its status word to the Bus Controller. No Data Words will be transmitted in response to an illegalized Transmit command. Data Words associated with an illegalized Receive command will, however, be presented to the subsystem. $\overline{ILLCMD}$ is sampled approximately 5 ms following the mid-parity bit zero crossing of the received Command Word (reference FIGURES 4-9). Command illegalization can be implemented using either a two-state or three-state address bus. An external PROM, PLD, or RAM device can be used to define the legality of specific commands. Any subset of the possible 1553 commands can be illegalized as a function of broadcast, $\overline{T}$/R bit, subaddress, word count, and/or mode code.

Illegalizing commands in the two-state mode, based on broadcast, $\overline{T}$/R bit, subaddress, and/or mode code, may be done by means of a programmable device such as a PROM. The address outputs from the STIC may be connected directly to the address inputs to a PROM. Illegalizing commands in the two-

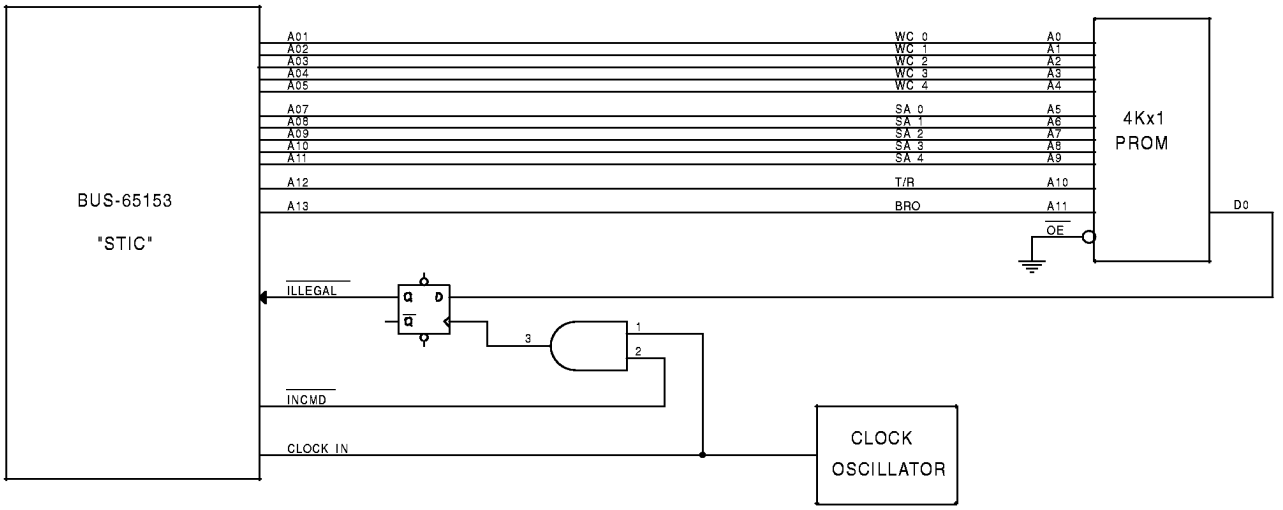


FIGURE 2. BUS-65153 TWO-STATE ILLEGALIZATION

state mode, based on broadcast, T/R bit, subaddress, **and** word count requires an external latch to store the value of the word count field. The word count must be latched after the address lines A5...A1 are updated for the present command and before these address lines are cleared to 00000 for the command word transfer.

The word count address lines (A5...A1) are multiplexed internally between the latched word count field of the command word, and the current word counter. While the signal $\overline{\text{INCMD}}$ is high (logic 1) these address lines reflect the word count field of the present command. While $\overline{\text{INCMD}}$ is low (logic 0) these signals represent the value of the current word counter, which is cleared to zero at the start of a message, and is incremented after each data word transfer.

The output of the illegalization PROM may be latched using a flip-flop and an AND gate (see FIGURE 2). The output signal INCMD from the STIC is used as the clock enable input to the flip-flop. The flip-flop is updated on every rising clock edge while INCMD is high, and is not updated while $\overline{\text{INCMD}}$ is low. This allows the output of the PROM to be updated on the last clock edge before $\overline{\text{INCMD}}$ is asserted low. Once $\overline{\text{INCMD}}$ is asserted, the clock enable input to the flip-flop is removed, thus preserving the value of the latched illegal bit.

Illegalizing commands in the three-state mode of operation also requires the use of a latch. The latch must be updated during a word transfer since the address lines are normally in a high impedance state. FIGURE 3 illustrates a method of latching the output from the PROM using a flip-flop and the signal $\overline{\text{CS}}$.

The signal $\overline{\text{CS}}$ is driven low during every word transfer. The only word transfer that takes place before the illegal command input ($\overline{\text{ILLCMD}}$) input is sampled is the command word transfer. The word count field of the command word may be obtained directly from the lower 5 bits of the data bus. The subaddress, $\overline{\text{T}}$/R, and broadcast signals are available on address lines A07-A13. Note that the signal $\overline{\text{CS}}$ will be asserted twice during a transfer in the 8-bit mode of operation. The word count field is located in the lower byte, which is presented during the second byte transfer. The second CS will, therefore, latch the appropriate value for $\overline{\text{ILLEGAL}}$.

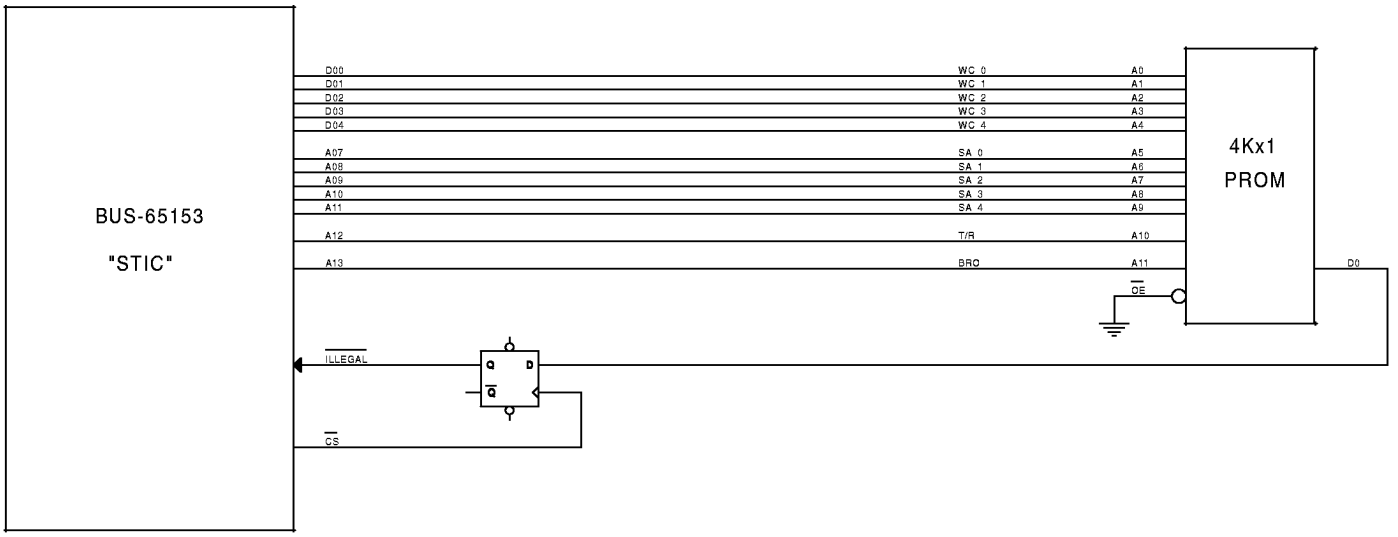


FIGURE 3. BUS-65153 THREE-STATE ILLEGALIZATION

This method of latching the address lines places a constraint on the access time of the PROM and on the maximum request to grant time for the command word transfer. The access time of the PROM must be less than 195 ns. If the data bus grant signal is held off too long, the $\overline{\text{ILLCMD}}$ input will not be updated in time. The maximum request to grant time is equal to the following:

transfer type	tmax
16-bit @12 MHz	2.455 ms
16-bit @16 MHz	2.720 ms
8-bit @12 MHz	1.940 ms
8-bit @16 MHz	2.205 ms

TRANSMIT COMMAND (RT-TO-BC TRANSFER)

If the BUS-65153 receives a valid Transmit Command Word that the subsystem determines is legal (input $\overline{\text{ILLCMD}}$ is high) and the subsystem is not BUSY (input $\overline{\text{BUSY}}$ is high), the BUS-65153 will initiate a transmit data response following transmission of the Status Word. This entails a handshake/read cycle for each Data Word, with the total number of Data Words to be transmitted specified by the Word Count field of the Command Word.

A low on $\overline{\text{ILLCMD}}$ will result in the Message Error bit being set. No Data Words will be transmitted following transmission of the Status Word to an illegalized transmit command. A low on the $\overline{\text{BUSY}}$ input will set the BUSY bit in the Status Word; in this instance, only the Status Word will be transmitted, with no Data Words.

RECEIVE COMMAND (BC-TO-RT TRANSFER)

A DMA handshake will be initiated for each word received over the 1553 data bus. If successful, the respective handshake will be followed by a corresponding write cycle. A handshake timeout will not terminate transfer attempts for the remaining Data Words, error flagging or Status Word transmission. After the reception of a valid nonmode code receive Command Word followed by the correct number of valid Data Words and assuming that all words are successfully transferred to the subsystem, a negative pulse will be asserted on the output Good Block Received ($\overline{\text{GBR}}$).

RT-TO-RT TRANSFER ERRORS

If the $\overline{\text{T}}$/R bit of the "transmit" command in an RT-to-RT transfer is a zero, the transmitting RT does not respond in time or an address mismatch is detected in the transmitting RT's Status Word, the BUS-65153, as receiving RT, will classify the condition as a "Command error" and will not respond.

RT STATUS, ERROR HANDLING, AND MESSAGE TIMING SIGNALS

Message transfer errors are indicated by means of the $\overline{\text{HS_FAIL}}$, $\overline{\text{ME}}$, and $\overline{\text{RT_FAIL}}$ error indication outputs. Additional error detection and indication mechanisms include updating of the internal Status and BIT Word registers.

The BUS-65153 provides a number of timing signals during the processing of 1553 messages. $\overline{\text{NBGRT}}$ provides a negative pulse output following the receipt of a 1553 Command Word. $\overline{\text{INCMD}}$ is asserted low when a new command is received. At the end of a message (either valid or invalid), $\overline{\text{INCMD}}$ transitions from low to high. Following the last data word of a valid nonmode code receive message, $\overline{\text{GBR}}$ is asserted low. $\overline{\text{ME}}$ is asserted as a low output following any detected error in a received message.

LOOPBACK TEST

The BUS-65153 performs a loopback self-test at the end of each nonbroadcast message processed. The loopback test consists of the following verifications: (1) The received version of every transmitted word is verified for validity (encoding, bit count, parity) and correct sync type; (2) The first transmitted word (RT Status Word) is checked for correct RT Address field; and (3) The received version of the last transmitted word is verified by means of a bit-by-bit comparison to the transmitted version of the word. If there is a transmitter timeout (668 ms) and/or the loopback test fails for one or more transmitted words, the Terminal Flag Status Word bit will be set in response to the next nonbroadcast message.

STATUS WORD

The Broadcast Command Received bit is formulated internally. The Message Error Status bit will be set if the current command is a Transmit Status Word or Transmit Last Command mode command and if there was an error in the data portion of the previous receive message. Message Error will also be set if $\overline{\text{ILLCMD}}$ has been sampled low for the current message. $\overline{\text{ILLCMD}}$, Service Request, Busy, and Subsystem Flag will be sampled from their respective Status input pins approximately 5 ms following the mid-parity bit zero crossing of the received Command Word.

BIT WORD

The BUS-65153 provides an internally formulated Built-In-Test word. This word is transmitted to the BC in response to a Transmit Bit Word Mode Code Command.

Internal Built-In-Test (BIT) Word Definition

D15:	Transmitter Timeout
D14:	Loop Test Failure - B Bus
D13:	Loop Test Failure - A Bus
D12:	Handshake Failure
D11:	Bus B Transmitter Shutdown
D10:	Bus A Transmitter Shutdown
D09:	Terminal Flag Inhibited
D08:	Ch A / Ch B
D07:	High Word Count
D06:	Low Word Count
D05:	Incorrect Sync Type Received
D04:	Invalid Word Received - Manchester or Parity Error
D03:	RT-RT Transfer Response Error (no gap, data sync, address mismatch)
D02:	RT-RT Transfer No Response Timeout
D01:	RT-RT Transfer - T/R Error on Second Command or My Valid Address
D00:	Command Word Contents Error

Note: Bits 15 through 9 are cleared only following a $\overline{\text{RESET}}$

input or reception of a Reset Remote Terminal mode command. Bits 8 through 0 are updated as a result of every message processed.

BIT WORD Bit Descriptions

TRANSMITTER TIMEOUT: Set if the STIC's failsafe timer detected a fault condition. The transmitter timeout circuit will automatically shut down the CH. A or CH. B transmitter if it transmits for longer than 668 μS.

CH. B LOOP TEST FAILURE, CH. A LOOP TEST FAILURE: A loopback test is performed on the transmitted portion of every non-broadcast message. A validity check is performed on the received version of every word transmitted by the STIC. In addition, a bit-by-bit comparison is performed on the last word transmitted by the RT for each message. If either the received version of any transmitted word does not match the transmitted version and/or the received version of the last transmitted word is determined to be invalid (sync, encoding, bit count, parity), or a failsafe timeout occurs on the respective channel, the LOOP TEST FAILURE bit for the respective bus channel will be set.

HANDSHAKE FAILURE: If this bit is set, it indicates that the subsystem had failed to respond with the DMA handshake input DTGRT asserted within the allotted time in response to the STIC asserting DTREQ. The allotted time for the subsystem's DTREQ-to-DTGRT response time is approximately 3.0 to 3.7 ms for a DMA write cycle and approximately 15.1 to 15.3 ms for a DMA read cycle.

CH. B TRANSMITTER SHUTDOWN, CH. A TRANSMITTER SHUTDOWN: Indicates that the transmitter on the respective bus channel has been shut down by a Transmitter shutdown mode code command received on the alternate channel. If an Override transmitter shutdown mode code command is received on the alternate channel, this bit will revert back to logic "0".

TERMINAL FLAG INHIBITED: Set to logic "1" if the STIC's Terminal Flag RT Status bit has been disabled by an Inhibit Terminal Flag mode code command. Will revert to logic "0" if an Override inhibit terminal flag mode code command is received.

CH. A/CH. B: Logic "0" if the previous message was received on CH.A, logic "1" if the previous message was received on CH. B.

HIGH WORD COUNT: Set to logic "1" if the previous message had a high word count error.

LOW WORD COUNT: Set to logic "1" if the previous message had a low word count error.

INCORRECT SYNC TYPE RECEIVED: If set, indicates that the STIC detected a Command sync in a received Data Word.

INVALID WORD: Indicates that the STIC received one or more words containing one or more of the following error types: sync field error, Manchester encoding error, parity error, and/or bit count error.

RT-to-RT GAP/SYNC/ADDRESS ERROR: This bit is set if the STIC RT is the receiving RT for an RT-to-RT transfer and one or more of the following occur: (1) If the transmitting RT responds with a response time of less than 4 ms, per MIL-STD-1553B (mid-parity bit to mid-sync); i.e., less than 2 ms dead time; and/or (2) There is an incorrect sync type or format error (encoding, bit count, and/or parity error) in the transmitting RT Status Word; and/or (3) The RT address field of the transmitting RT Status Word does not match the RT address in the transmit Command Word.

RT-to-RT RESPONSE TIMEOUT: If set, indicates that, for the previous message, the STIC was the receiving RT for an RT-to-RT transfer and that the transmitting RT either did not respond or responded later than the STIC's RT-to-RT Timeout time. The STIC's RT-to-RT Response Timeout Time is defined as the time from the mid-bit crossing of the parity bit of the transmit Command Word to the mid-sync crossing of the transmitting RT Status Word. The value of the STIC's RT-to-RT Response Timeout time is 18.9 μS.

RT-to-RT SECOND COMMAND ERROR: If the STIC is the receiving RT for an RT-to-RT transfer, this bit set indicates one or more of the following error conditions in the transmit Command Word: (1) $\overline{T}$/R bit = logic "0"; (2) subaddress = 00000 or 11111; (3) Same RT Address field as the receive Command Word.

COMMAND WORD CONTENTS ERROR: Indicates a received command word is not defined in accordance with MIL-STD-1553B. This includes the following undefined Command Words: (1) The Command Word is a non-mode code, broadcast, transmit command; (2) A message with a T/R bit of "0", a subaddress/mode field of 00000 or 11111 and a mode code field between 00000 and 01111; (3) A mode code command that is not permitted to be broadcast (e.g., Transmit Status) is sent to the broadcast address 11111.

MODE CODES

All 13 of the dual redundant MIL-STD-1553B mode codes are implemented by the BUS-65153. Two mode codes, Transmit Vector Word and Synchronize (with data) involve data transfer with the subsystem. For the Transmit BIT Word mode code, the internally formulated BIT Word is transmitted. TABLE 2 provides a summary of the 1553B mode codes supported by the BUS-65153.

TABLE 2. MIL-STD-1553B MODE CODES

T/R BIT	MODE CODE	FUNCTION	DATA WORD	BROADCAST ALLOWED
1	00000	Dynamic Bus Control	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit Status Word	No	No
1	00011	Initiate Self Test	No	Yes
1	00100	Transmitter Shutdown	No	Yes
1	00101	Override Transmitter Shutdown	No	Yes
1	00110	Inhibit Terminal Flag	No	Yes
1	00111	Override Inhibit Terminal Flag	No	Yes
1	01000	Reset Remote Terminal	No	Yes
1	01001-11111	RESERVED	No	TBD
1	10000	Transmit Vector Word	From Subsystem	No
0	10001	Synchronize with Data	To Subsystem	Yes
1	10010	Transmit Last Command	From Internal Register	No
0	10100	Selected Transmitter Shutdown (See Note)	To Subsystem	Yes
0	10101	Override Selected Transmitter Shutdown (See Note)	To Subsystem	Yes
1	10011	Terrminal BIT Word	From Internal Register	No
0	10110-11111	RESERVED	Yes	TBD
1	10110-11111	RESERVED	Yes	TBD

Note: Terminal responds with Clear Status but no action is taken, assuming a valid Command Word and any valid Data Word is received.

TABLE 3. OVERALL MEMORY MAP
Note: TABLES 3 and 3A-3D are byte-oriented addressing.

ADDRESS (HEX)	FUNCTION
0000-007F	MODE CODE (SUBADDRESS 0000, T/R = 0), See (TABLE 3B)
0080-00FF	RECEIVE, SUBADDRESS 1 (See TABLE 3A)
0100-017F	RECEIVE, SUBADDRESS 2 (See TABLE 3A)
•	•
•	•
•	•
0F00-0F7F	RECEIVE, SUBADDRESS 30 (See TABLE 3A)
0F80-0FFF	MODE CODE (SUBADDRESS 11111), T/R = 1 (SeeTABLE 3C)
1000-107F	MODE CODE (SUBADDRESS 00000), T/R = 1 (SeeTABLE 3D)
1080-10FF	TRANSMIT, SUBADDRESS 1 (See TABLE 3A)
1100-117F	TRANSMIT, SUBADDRESS 2 (See TABLE 3A)
•	•
•	•
•	•
1F00-1F7F	TRANSMIT SUBADDRESS 30 (See TABLE 3A)
1F80-1FFF	MODE CODE (SUBADDRESS 11111), T/R = 1 (SeeTABLE 3E)
2000-207F	BROADCAST MODE CODE (SUBADDRESS 00000), T/R = 0 (Note: Use TABLE 3B, but increase address by 2000)
2080-20FF	BROADCAST, RECEIVE, SUBADDRESS 1 (See TABLE 3A)
2100-217F	BROADCAST, RECEIVE, SUBADDRESS 2 (See TABLE 3A)
•	•
•	•
•	•
2F00-2F7F	BROADCAST, RECEIVE, SUBADDRESS 30 (See TABLE 3A)
2F80-2FFF	BROADCAST MODE CODE (SUBADDRESS 11111), T/R = 0 (Note: Use TABLE 3C, but increase address by 2000)
3000-307F	BROADCAST MODE CODE (SUBADDRESS 00000), T/R = 0 (Note: Use TABLE 3D, but increase address by 2000)
3080-30FF	BROADCAST, TRANSMIT, SUBADDRESS 1 (UNDEFINED)
3100-317F	BROADCAST, TRANSMIT, SUBADDRESS 2 (UNDEFINED)
•	•
•	•
•	•
3F00-3F7F	BROADCAST, TRANSMIT, SUBADDRESS 30 (UNDEFINED)
3F80-3FFF	BROADCAST MODE CODE (SUBADDRESS 11111), T/R = 1 (Note: Use TABLE 3E, but increase address by 2000)

TABLE 3A. TYPICAL MEMORY MAP OF EACH NON-MODE CODE SUBADDRESS, 64 WORD BLOCK	
OFFSET (HEX)	**FUNCTION**
0000, 0001	COMMAND WORD
0002, 003F	NOT USED
0040, 0041	DATA WORD 0
0042, 0043	DATA WORD 1
•	•
•	•
•	•
007E, 007F	DATA WORD 31

TABLE 3B. MODE CODE MEMORY MAP FOR SUBADDRESS 00000,T/R = 0	
ADDRESS (HEX)	**FUNCTION**
0000, 0001	COMMAND WORD, T/R = 0, MODE CODE 00000 (INVALID)
•	•
•	•
•	•
001E, 001F	COMMAND WORD, T/R = 0, MODE CODE 01111 (INVALID)
020E, 0021	COMMAND WORD, T/R = 0, MODE CODE 10000 (RESERVED)
0022, 0023	COMMAND WORD, T/R = 0, MODE CODE 10001 (SYNC WITH DATA)
•	•
•	•
•	•
003E, 003F	COMMAND WORD, T/R = 0, MODE CODE 11111 (RESERVED)
0040, 005F	NOT USED (MODE CODES WITHOUT DATA)
0060, 0063	DATA WORD FOR MODE CODE 10000, T/R = 0 (RESERVED)
0062, 0063	DATA WORD FOR MODE CODE 10001, T/R = 0 (SYNC WITH DATA)
•	•
•	•
•	•
007E, 007F	DATA WORD FOR MODE CODE 11111, T/R = 0 (RESERVED)

TABLE 3C. MODE CODE MEMORY MAP FOR SUBADDRESS 11111 T/R = 0	
ADDRESS (HEX)	**FUNCTION**
0F80, 0F81	COMMAND WORD, T/R = 0, MODE CODE 00000 (UNDEFINED)
•	•
•	•
•	•
009E, 009F	COMMAND WORD, T/R = 0, MODE CODE 01111 (UNDEFINED)
0FA0, 0FA1	COMMAND WORD, T/R = 0, MODE CODE 10000 (RESERVED)
0FA2, 0FA3	COMMAND WORD, T/R = 0, MODE CODE 10001 (SYNC WITH DATA)
•	•
•	•
•	•
0FBE, 0FBF	COMMAND WORD, T/R = 0, MODE CODE 11111 (RESERVED)
0FC0, 0FDF	NOT USED (MODE CODES WITHOUT DATA)
0FE0, 0FE1	DATA WORD FOR MODE CODE 10000, T/R = 0 (RESERVED)
0FE2, 0FE3	DATA WORD FOR MODE CODE 10001, T/R = 0 (SYNC WITH DATA)
•	•
•	•
•	•
0FFE, 0FFF	DATA WORD FOR MODE CODE 11111, T/R = 0 (RESERVED)

TABLE 3D. MODE CODE MEMORY MAP FOR SUBADDRESS 00000, T/R = 1	
ADDRESS (HEX)	**FUNCTION**
1000, 1001	COMMAND WORD, T/R = 1, MODE CODE 00000 (DYNAMIC BUS CONTROL)
•	•
•	•
•	•
101E, 101F	COMMAND WORD, T/R = 1, MODE CODE 01111 (RESERVED)
1020, 1021	COMMAND WORD, T/R = 1, MODE CODE 10000 (TRANSMIT VECTOR WORD)
1022, 1023	COMMAND WORD, T/R = 1, MODE CODE 10001 RESERVED)
•	•
•	•
•	•
103E, 103F	COMMAND WORD, T/R= 1, MODE CODE 11111 (RESERVED)
1040, 105F	NOT USED (MODE CODES WITHOUT DATA)
1060, 1061	DATA WORD FOR MODE CODE 10000, T/R = 1 (TRANSMIT VECTOR WORD)
1062, 1063	DATA WORD FOR MODE CODE 10001, T/R = 1 (RESERVED)
•	•
•	•
•	•
107E, 107F	DATA WORD FOR MODE CODE 11111, T/R = 1 (RESERVED)

TABLE 3E. MODE CODE MEMORY MAP FOR SUBADDRESS 11111, T/R = 1	
ADDRESS (HEX)	**FUNCTION**
1F80, 0F81	COMMAND WORD, T/R = 1, MODE CODE 00000 (DYNAMIC BUS CONTROL)
•	•
•	•
•	•
1F9E, 1F9F	COMMAND WORD, T/R = 1, MODE CODE 01111 (RESERVED)
1FA0, 1FA1	COMMAND WORD, T/R = 1, MODE CODE 10000 (TRANSMIT VECTOR WORD)
1FA2, 1FA3	COMMAND WORD, T/R = 1, MODE CODE 10001(RESERVED)
•	•
•	•·
•	•·
1FBE, 1FBF	COMMAND WORD, T/R = 1, MODE CODE 11111 (RESERVED)
1FC0, 1FDF	NOT USED (MODE CODES WITHOUT DATA)
1FE0, 1FE1	DATA WORD FOR MODE CODE 10000, T/R = 1 (TRANSMIT VECTOR WORD)
1FE2, 1FE3	DATA WORD FOR MODE CODE 10001, T/R = 1 (RESERVED)
•	•
•	•
•	•
	DATA WORD FOR MODE CODE 11111, T/R = 1 (RESERVED)

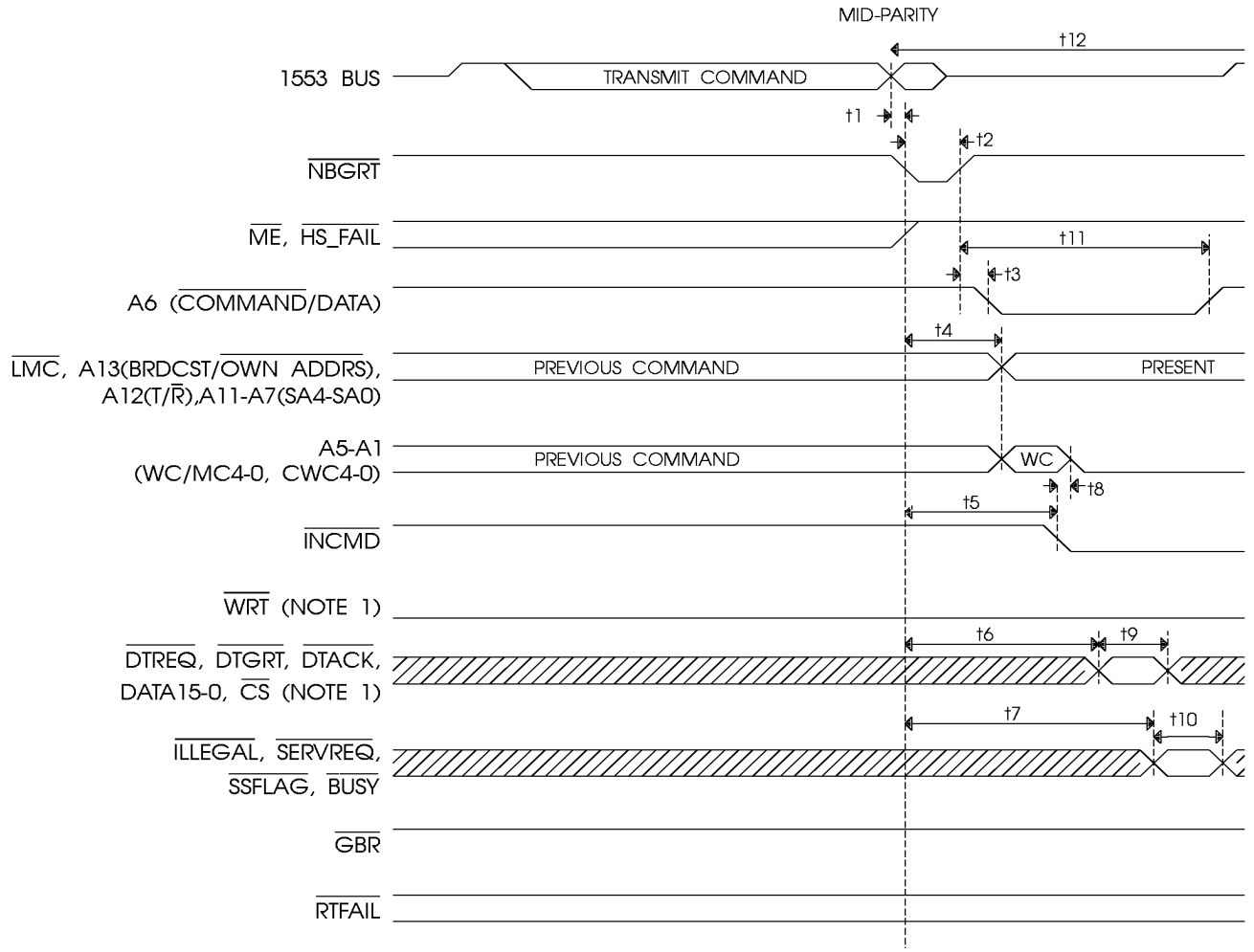


FIGURE 4. RT TO BC (TRANSMIT) TIMING					
SYMBOL	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**
t1(@12MHz)	COMMAND MID-PARITY CROSSING TO FALLING EDGE OF $\overline{\text{NBGRT}}$	0.97		1.56	ms
t1(@16MHz)	COMMAND MID-PARITY CROSSING TO FALLING EDGE OF $\overline{\text{NBGRT}}$	0.87		1.38	ms
t2(@12MHz)	$\overline{\text{NBGRT}}$ PULSE WIDTH	140		190	ns
t2(@16MHz)	$\overline{\text{NBGRT}}$ PULSE WIDTH	100		150	ns
t3	$\overline{\text{NBGRT}}$ RISING EDGE TO $\overline{\text{A6}}$ FALLING EDGE			45	ns
t4(@12MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO ADDRESS VALID	300		410	ns
t4(@16MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO VALID ADDRESS	220		330	ns
t5(@12MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO $\overline{\text{INCMD}}$ FALLING EDGE	800		865	ns
t5(@16MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO $\overline{\text{INCMD}}$ FALLING EDGE	590		655	ns
t6(@12MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO START OF COMMAND WORD TRANSFER CYCLE (Note 2)	1.19		1.28	ms
t6(@16MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO START OF COMMAND WORD TRANSFER CYCLE (Note 2)	0.88		0.97	ms
t7	$\overline{\text{NBGRT}}$ FALLING EDGE TO VALID STATUS INPUTS			4.1	ms
t8	$\overline{\text{INCMD}}$ FALLING EDGE TO CWC VALID	5		60	ns
t9	DATA TRANSFER CYCLE TIME (Notes 2,3,4)	See Note 4			ms
t10	STATUS INPUTS HOLD TIME	500			ns
t11(@12MHz)	$\overline{\text{NBGRT}}$ RISING TO A6 RISING (Note 5)		3		ms
t11(@16MHz)	$\overline{\text{NBGRT}}$ RISING TO A6 RISING (Note 5)		3		ms
t12(@12MHz)	RT RESPONSE TIME	6.18		6.96	ms
t12(@16MHz)	RT RESPONSE TIME	6.0		6.76	ms

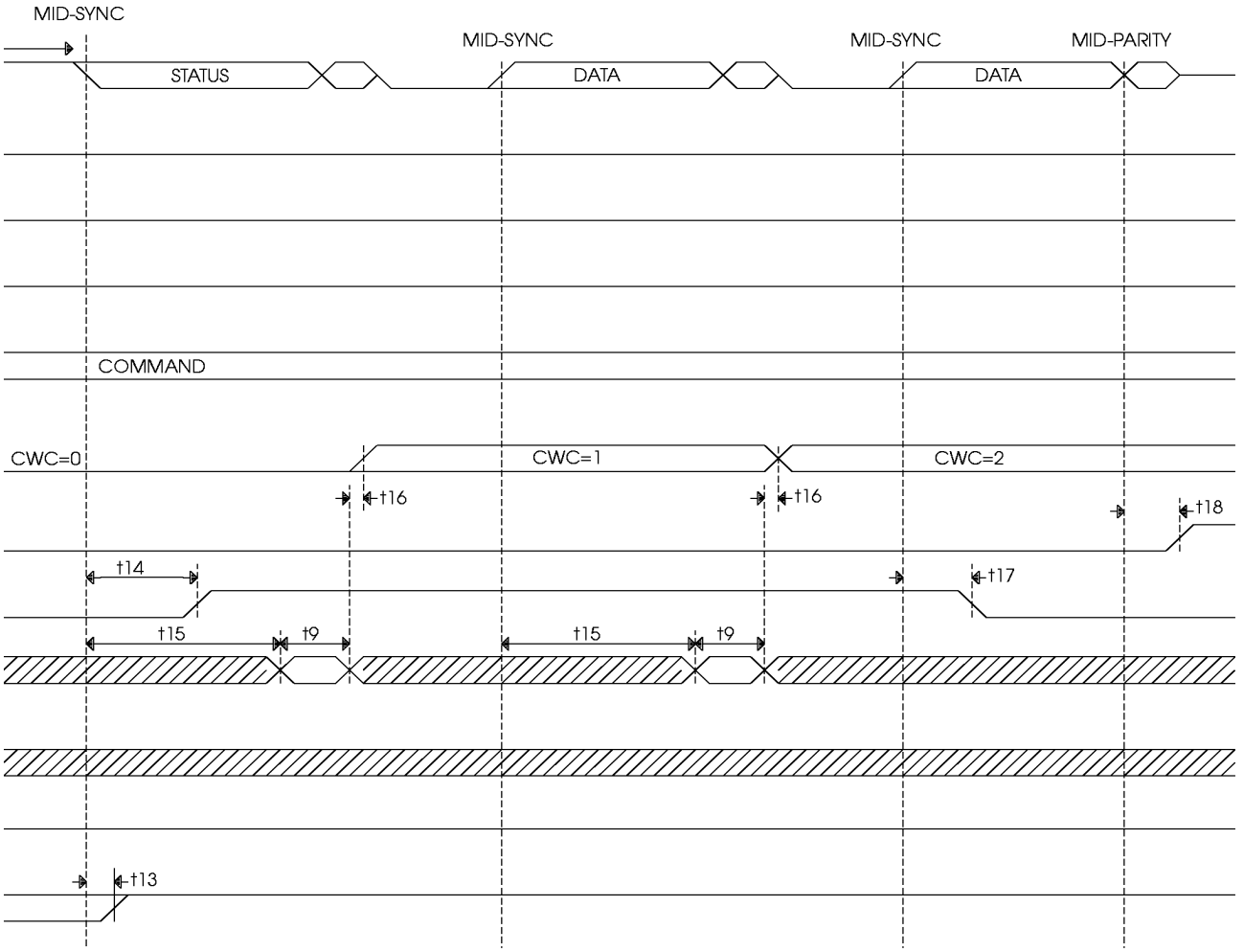


FIGURE 4. RT TO BC (TRANSMIT) TIMING (CONTINUED)					
SYMBOL	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**
t13	MID-SYNC CROSSING OF STATUS RESPONSE TO $\overline{\text{RTFAIL}}$ RISING			100	ns
t14(@12MHz)	MID-SYNC CROSSING OF STATUS RESPONSE TO $\overline{\text{WRT}}$ RISING	0.920		1.405	ms
t14(@16MHz)	MID-SYNC CROSSING OF STATUS RESPONSE TO $\overline{\text{WRT}}$ RISING	0.840		1.305	µs
t15(@12MHz)	MID-SYNC CROSSING OF TRANSMITTED DATA TO START OF DATA TRANSFER CYCLE (Note 2)	1.700		2.085	µs
t15(@16MHz)	MID-SYNC CROSSING OF TRANSMITTED DATA TO START OF DATA TRANSFER CYCLE (Note 2)	1.430		1.795	µs
t16	END OF DATA TRANSFER CYLE TO VALID NEXT WC (Note 3)			60	ns
t17(@12MHz)	MID-SYNC CROSSING OF LAST DATA WORD TO $\overline{\text{WRT}}$ FALLING	0.965		1.365	µs
t17(@16MHz)	MID-SYNC CROSSING OF LAST DATA WORD TO $\overline{\text{WRT}}$ FALLING	0.880		1.260	µs
18(@12MHz)	MID-PARTIY CROSSING OF LAST DATA WORD TO $\overline{\text{INCMD}}$ RISING	1.010		1.470	µs
t18(@16MHz)	MID-PARTIY CROSSING OF LAST DATA WORD TO $\overline{\text{INCMD}}$ RISING	0.910		1.350	µs

Notes:
1)IF ADDR_ENA IS LOGIC “1”, $\overline{\text{CS}}$, $\overline{\text{WRT}}$, AND A13..A0 WILL BE IN A HIGH IMPEDANCE STATE EXCEPT FOR WHEN A WORD TRANSFER IS BEING PERFORMED ($\overline{\text{DT_ACK}}$ = LOGIC “0”).
2)THE LEADING EDGE OF TIME REFERENCE t9 AND THE TRAILING EDGE OF TIME REFERENCES t6 AND t15 ARE DEFINED AS THE FALLING EDGE OF $\overline{\text{DT_REQ}}$.
3)THE TRAILING EDGE OF REFERENCE t9 AND THE LEADING EDGE OF TIME REFERENCE t16 ARE DEFINED AS THE RISING EDGE OF $\overline{\text{DT_REQ}}$.
4)DATA TRANSFER CYCLE TIMING INFORMATION IS DESCRIBED IN OTHER FIGURES.
5)IF THE COMMAND WORD TRANSFER CYCLE IS NOT COMPLETE (i.e., $\overline{\text{DT_REQ}}$ IS STILL LOGIC LOW) BY THE TIME INDICATED BY THE TRAILING EDGE OF t11, A6 WILL BE HELD LOW UNTIL THE AFTER TRANSFER CYCLE IS COMPLETE (60 ns MAX AFTER THE RISING EDGE OF $\overline{\text{DT_REQ}}$).

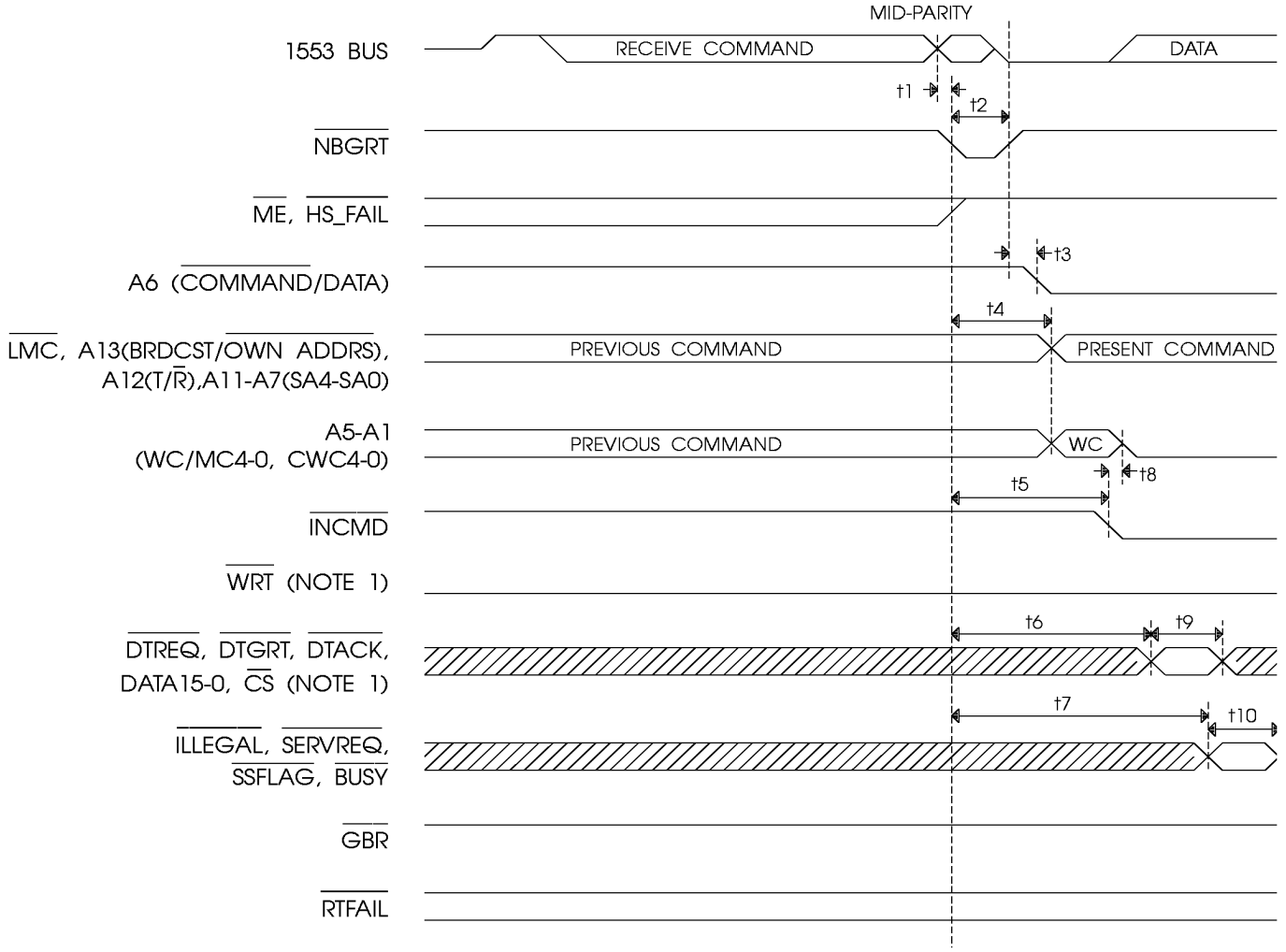


FIGURE 5. BC TO RT (RECEIVE) TIMING					
SYMBOL	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**
t1(@12MHz)	COMMAND MID-PARITY CROSSING TO FALLING EDGE OF $\overline{\text{NBGRT}}$	0.97		1.56	µs
t1(@16MHz)	COMMAND MID-PARITY CROSSING TO FALLING EDGE OF $\overline{\text{NBGRT}}$	0.87		1.38	µs
t2(@12MHz)	$\overline{\text{NBGRT}}$ PULSE WIDTH	140		190	ns
t2(@16MHz)	$\overline{\text{NBGRT}}$ PULSE WIDTH	100		150	ns
t3	$\overline{\text{NBGRT}}$ RISING EDGE TO $\overline{\text{A6}}$ FALLING EDGE			45	ns
t4(@12MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO ADDRESS VALID, $\overline{\text{LMC}}$	300		410	ns
t4(@16MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO VALID ADDRESS, $\overline{\text{LMC}}$	220		330	ns
t5(@12MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO $\overline{\text{INCMD}}$ FALLING EDGE	800		865	ns
t5(@16MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO $\overline{\text{INCMD}}$ FALLING EDGE	590		655	ns
t6(@12MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO START OF DATA TRANSFER CYCLE	1.19		1.28	µs
t6(@16MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO START OF DATA TRANSFER CYCLE (Note 2)	0.88		0.97	µs
t7	$\overline{\text{NBGRT}}$ FALLING EDGE TO VALID STATUS INPUTS			4.1	µs
t8	$\overline{\text{INCMD}}$ FALLING EDGE TO CWC VALID	5		60	ns
t9	DATA TRANSFER CYCLE TIME (Notes 2,3,4)	See Note 4			
t10	STATUS INPUTS HOLD TIME	500			ns
t11(@12MHz)	FIRST DATA WORD MID-PARITY CROSSING TO A6 RISING EDGE	820		1205	ns
t11(@16MHz)	FIRST DATA WORD MID-PARITY CROSSING TO A6 RISING EDGE	720		1025	ns

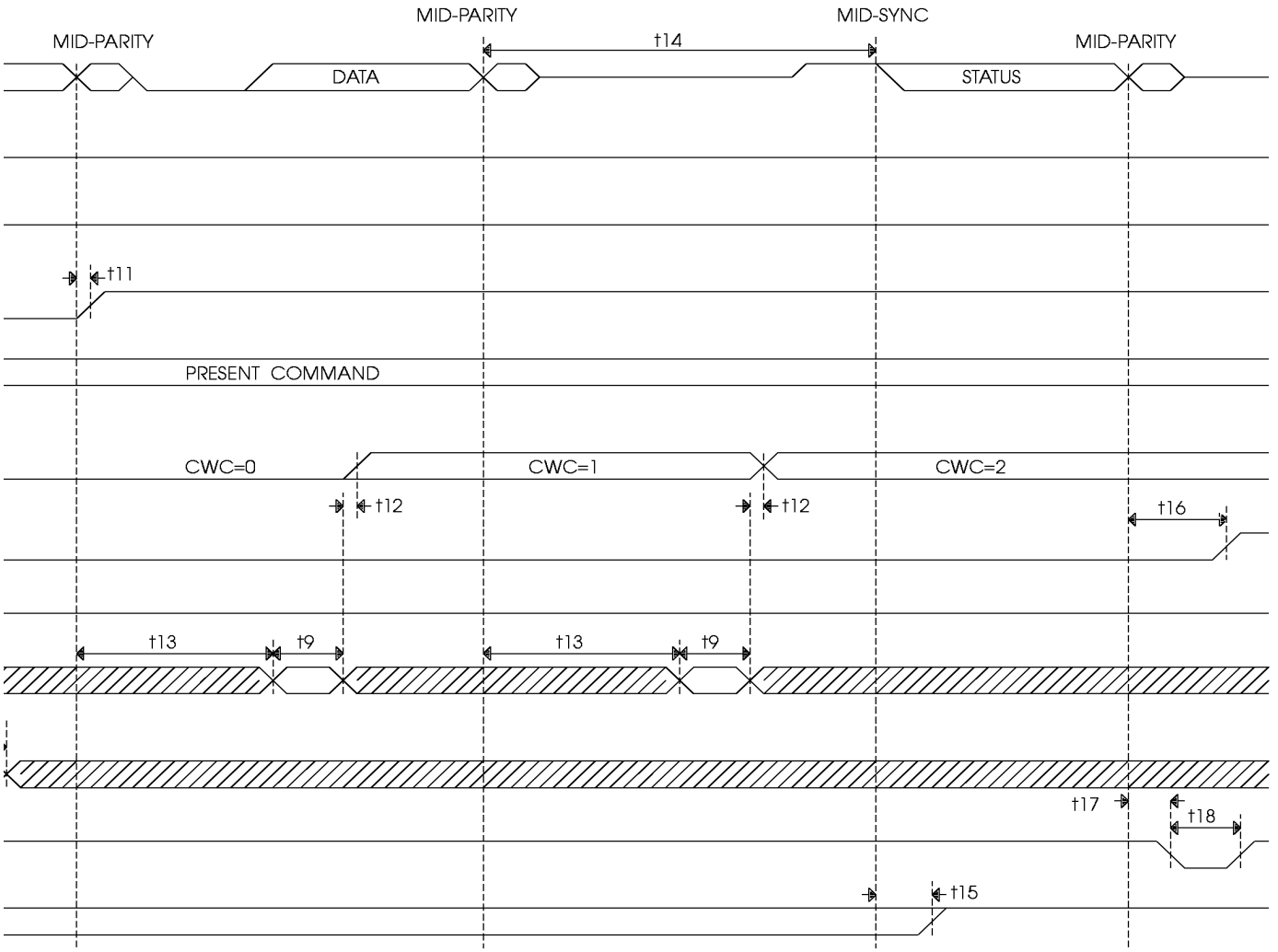


FIGURE 5. BC TO RT (RECEIVE) TIMING					
SYMBOL	**DESCRIPTION**	MIN	**TYP**	MAX	**UNITS**
t12	END OF DATA TRANSFER CYLE TO VALID NEXT WC (Note 3)			60	ns
t13(@12MHz)	MID-PARITY CROSSING OF RECEIVED DATA WORD TO START OF DATA TRANSFER CYCLE (Note 2)	1.52		1.94	ms
t14(@12MHz)	RT RESPONSE TIME	6.18		6.96	µs
t14(@16MHz)	RT RESPONSE TIME	6.0		6.76	µs
t15	MID-SYNC CROSSING OF STATUS RESPONSE TO $\overline{\text{RTFAIL}}$ RISING			100	µs
t16(@12MHz	MID-PARITY CROSSING OF STATUS RESPONSE TO $\overline{\text{INCMD}}$ RISING	3.36		3.57	µs
t16(@16MHz)	MID-PARITY CROSSING OF STATUS RESPONSE TO $\overline{\text{INCMD}}$ RISING	3.26		3.46	µs
t16(@12MHz)	MID-PARITY CROSSING OF STATUS RESPONSE TO $\overline{\text{GBR}}$ FALLING	3.23		3.37	µs
t17(@16MHz)	MID-PARITY CROSSING OF STATUS RESPONSE TO $\overline{\text{GBR}}$ FALLING	3.17		3.29	µs
t18(@12MHz)	$\overline{\text{GBR}}$ PULSE WIDTH	140		190	
t18(@16MHz	$\overline{\text{GBR}}$ PULSE WIDTH	100		150	ns

Notes:
1)IF ADDR_ENA IS LOGIC “1”, $\overline{\text{CS}}$, $\overline{\text{WRT}}$, AND A13..A0 WILL BE IN A HIGH IMPEDANCE STATE EXCEPT FOR WHEN A WORD TRANSFER IS BEING PERFORMED ($\overline{\text{DT_ACK}}$ = LOGIC “0”).
2)THE LEADING EDGE OF TIME REFERENCE t9 AND THE TRAILING EDGE OF TIME REFERENCES t6 AND t13 ARE DEFINED AS THE FALLING EDGE OF $\overline{\text{DT_REQ}}$.
3)THE TRAILING EDGE OF REFERENCE t9 AND THE LEADING EDGE OF TIME REFERENCE t12 ARE DEFINED AS THE RISING EDGE OF $\overline{\text{DT_REQ}}$.
4)DATA TRANSFER CYCLE TIMING INFORMATION IS DESCRIBED IN OTHER FIGURES.

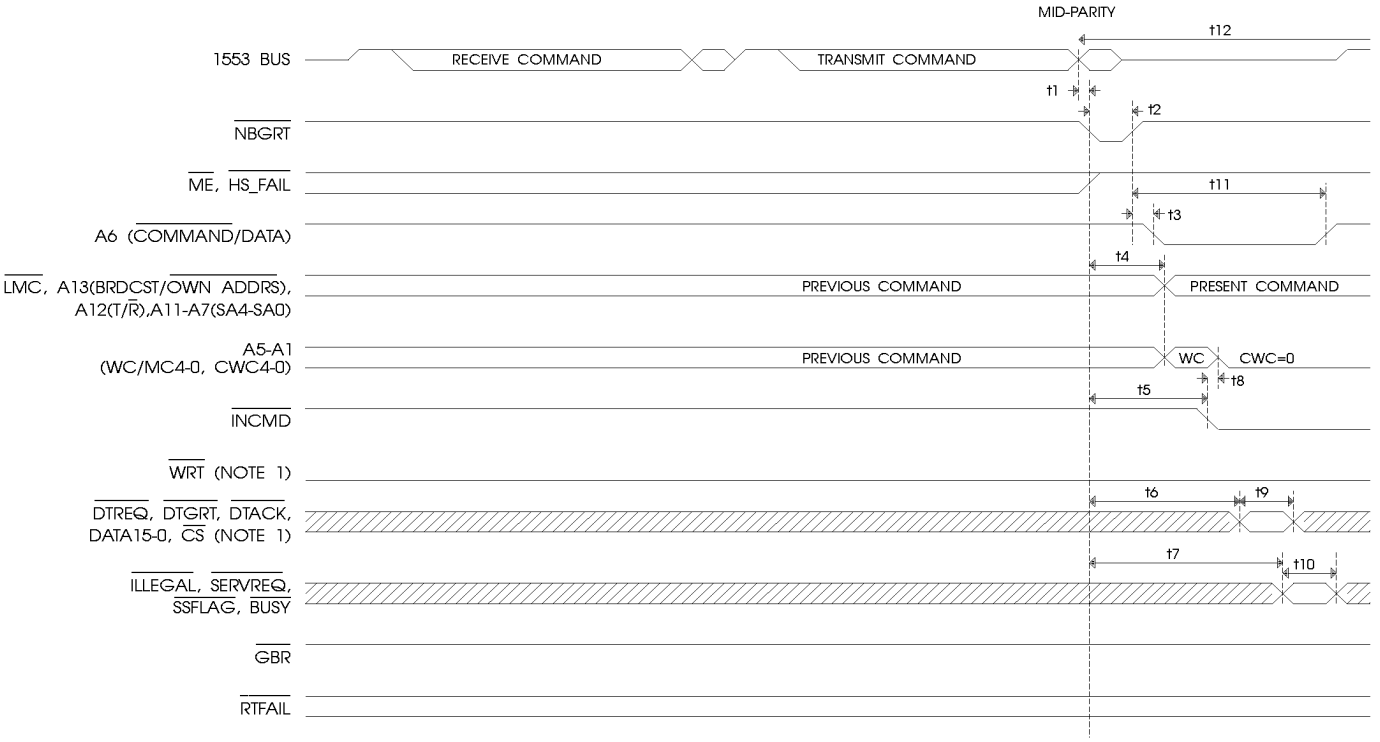


FIGURE 6. RT TO RT (TRANSMIT) TIMING					
SYMBOL	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**
t1(@12MHz)	COMMAND MID-PARITY CROSSING TO FALLING EDGE OF $\overline{\text{NBGRT}}$	0.97		1.56	µs
t1(@16MHz)	COMMAND MID-PARITY CROSSING TO FALLING EDGE OF $\overline{\text{NBGRT}}$	0.87		1.38	µs
t2(@12MHz)	$\overline{\text{NBGRT}}$ PULSE WIDTH	140		190	ns
t2(@16MHz)	$\overline{\text{NBGRT}}$ PULSE WIDTH	100		150	ns
t3	$\overline{\text{NBGRT}}$ RISING EDGE TO $\overline{\text{A6}}$ FALLING EDGE			45	ns
t4(@12MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO ADDRESS VALID	300		410	ns
t4(@16MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO VALID ADDRESS	220		330	ns
t5(@12MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO $\overline{\text{INCMD}}$ FALLING EDGE	800		865	ns
t5(@16MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO $\overline{\text{INCMD}}$ FALLING EDGE	590		655	ns
t6(@12MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO START OF COMMAND WORD TRANSFER CYCLE (Note 2)	1.19		1.28	µs
t6(@16MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO START OF COMMAND WORD TRANSFER CYCLE (Note 2)	0.88		0.97	µs
t7	$\overline{\text{NBGRT}}$ FALLING EDGE TO VALID STATUS INPUTS			4.1	µs
t8	$\overline{\text{INCMD}}$ FALLING EDGE TO CWC VALID	5		60	ns
t9	DATA TRANSFER CYCLE TIME (Notes 2,3,4)	See Note 4			
t10	STATUS INPUTS HOLD TIME	500			ns
t11(@12MHz)	$\overline{\text{NBGRT}}$ RISING TO A6 RISING (Note 5)		3		µs
t11(@16MHz)	$\overline{\text{NBGRT}}$ RISING TO A6 RISING (Note 5)		3		µs
t12(@12MHz)	RT RESPONSE TIME	6.18		6.96	µs
t12(@16MHz)	RT RESPONSE TIME	6.0		6.76	µs

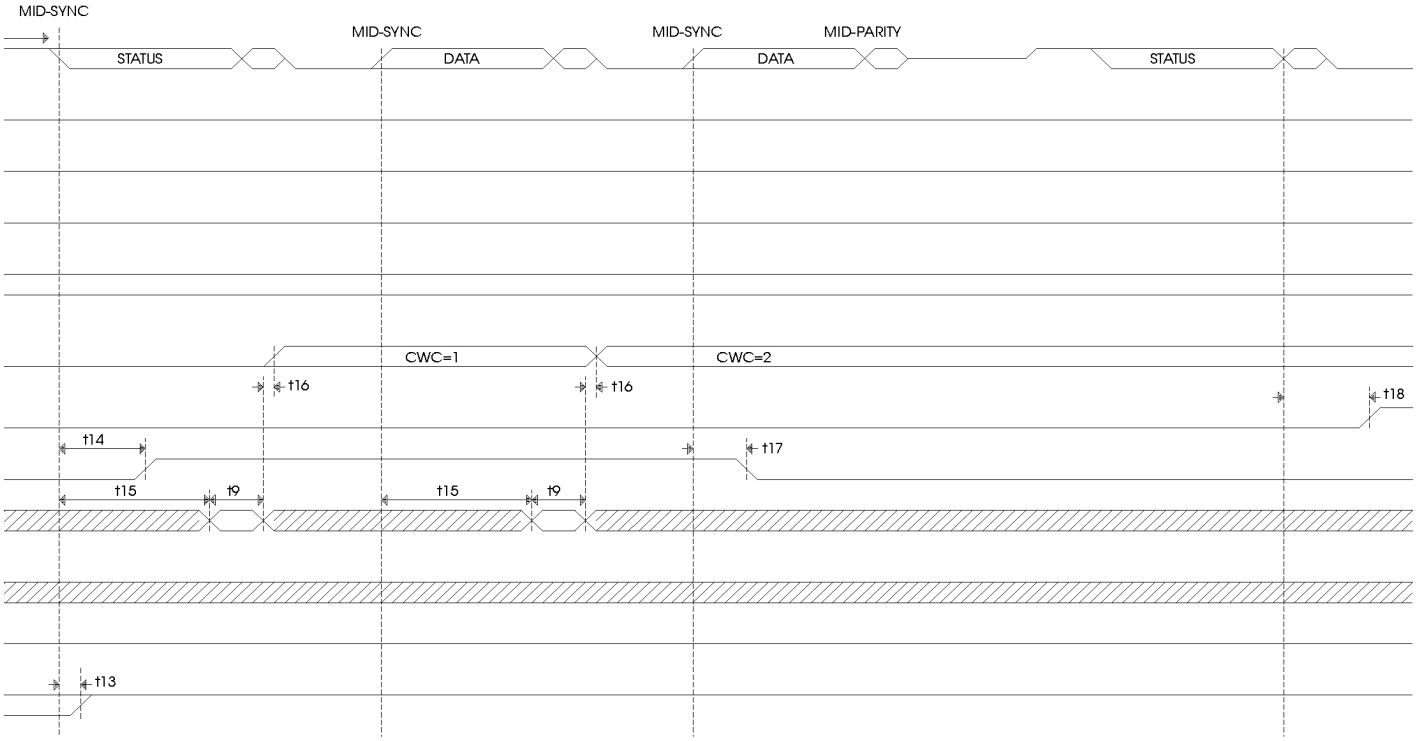


FIGURE 6. RT TO RT (TRANSMIT) TIMING (CONTINUED)					
SYMBOL	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**
t13	MID-SYNC CROSSING OF STATUS RESPONSE TO $\overline{\text{RTFAIL}}$ RISING			100	ns
t14(@12MHz)	MID-SYNC CROSSING OF STATUS RESPONSE TO $\overline{\text{WRT}}$ RISING	0.920		1.405	µs
t14(@16MHz)	MID-SYNC CROSSING OF STATUS RESPONSE TO $\overline{\text{WRT}}$ RISING	0.840		1.305	µs
t15(@12MHz)	MID-SYNC CROSSING OF TRANSMITTED DATA TO START OF DATA TRANSFER CYCLE (Note 2)	1.700		2.085	µs
t15(@16MHz)	MID-SYNC CROSSING OF TRANSMITTED DATA TO START OF DATA TRANSFER CYCLE (Note 2)	1.430		1.795	µs
t16	END OF DATA TRANSFER CYLE TO VALID NEXT WC (Note 3)			60	ns
t17(@12MHz	MID-SYNC CROSSING OF LAST DATA WORD TO $\overline{\text{WRT}}$ FALLING	0.965		1.365	µs
t17(@16MHz)	MID-SYNC CROSSING OF LAST DATA WORD TO $\overline{\text{WRT}}$ FALLING	0.880		1.260	µs
t18(@12MHz)	MID-PARTIY CROSSING OF LAST DATA WORD TO $\overline{\text{INCMD}}$ RISING	1.010		1.470	µs
18(@16MHz)	MID-PARTIY CROSSING OF LAST DATA WORD TO $\overline{\text{INCMD}}$ RISING	0.910		1.350	µs

Notes:
1)IF ADDR_ENA IS LOGIC “1”, $\overline{\text{CS}}$, $\overline{\text{WRT}}$, AND A13..A0 WILL BE IN A HIGH IMPEDANCE STATE EXCEPT FOR WHEN A WORD TRANSFER IS BEING PERFORMED ($\overline{\text{DT_ACK}}$ = LOGIC “0”).
2)THE LEADING EDGE OF TIME REFERENCE t9 AND THE TRAILING EDGE OF TIME REFERENCES t6 AND t15 ARE DEFINED AS THE FALLING EDGE OF $\overline{\text{DT_REQ}}$.
3)THE TRAILING EDGE OF REFERENCE t9 AND THE LEADING EDGE OF TIME REFERENCE t16 ARE DEFINED AS THE RISING EDGE OF $\overline{\text{DT_REQ}}$.
4)DATA TRANSFER CYCLE TIMING INFORMATION IS DESCRIBED IN OTHER FIGURES.
5)IF THE COMMAND WORD TRANSFER CYCLE IS NOT COMPLETE (i.e., $\overline{\text{DT_REQ}}$ IS STILL LOGIC LOW) BY THE TIME INDICATED BY THE TRAILING EDGE OF t11, A6 WILL BE HELD LOW UNTIL THE AFTER TRANSFER CYCLE IS COMPLETE (60 ns MAX AFTER THE RISING EDGE OF $\overline{\text{DT_REQ}}$).

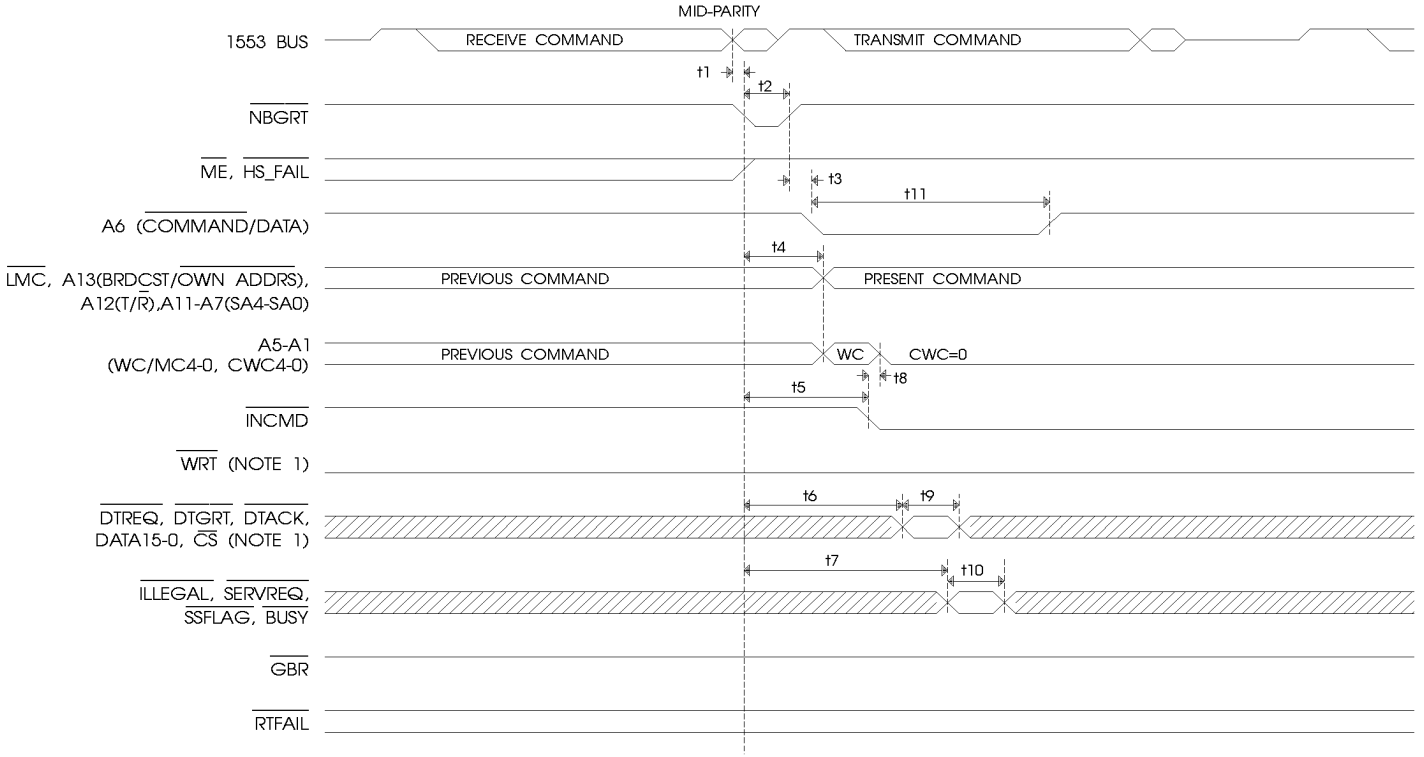


FIGURE 7. RT TO RT (RECEIVE) TIMING					
SYMBOL	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**
t1(@12MHz)	COMMAND MID-PARITY CROSSING TO FALLING EDGE OF $\overline{\text{NBGRT}}$	0.97		1.56	µs
t1(@16MHz)	COMMAND MID-PARITY CROSSING TO FALLING EDGE OF $\overline{\text{NBGRT}}$	0.87		1.38	µs
t2(@12MHz)	$\overline{\text{NBGRT}}$ PULSE WIDTH	140		190	ns
t2(@16MHz)	$\overline{\text{NBGRT}}$ PULSE WIDTH	100		150	ns
t3	$\overline{\text{NBGRT}}$ RISING EDGE TO $\overline{\text{A6}}$ FALLING EDGE			45	ns
t4(@12MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO ADDRESS VALID, $\overline{\text{LMC}}$	300		410	ns
t4(@16MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO VALID ADDRESS, $\overline{\text{LMC}}$	220		330	ns
t5(@12MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO $\overline{\text{INCMD}}$ FALLING EDGE	800		865	ns
t5(@16MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO $\overline{\text{INCMD}}$ FALLING EDGE	590		655	ns
t6(@12MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO START OF DATA TRANSFER CYCLE	1.19		1.28	µs
t6(@16MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO START OF DATA TRANSFER CYCLE (Note 2)	0.88		0.97	µs
t7	$\overline{\text{NBGRT}}$ FALLING EDGE TO VALID STATUS INPUTS			4.1	µs
t8	$\overline{\text{INCMD}}$ FALLING EDGE TO CWC VALID	5		60	ns
t9	DATA TRANSFER CYCLE TIME (Notes 2,3,4)	See Note 4			
t10	STATUS INPUTS HOLD TIME	500			ns
t11(@12MHz)	A6 PULSE WIDTH	820		1205	ns
t11(@16MHz)	A6 PULSE WIDTH	720		1025	ns

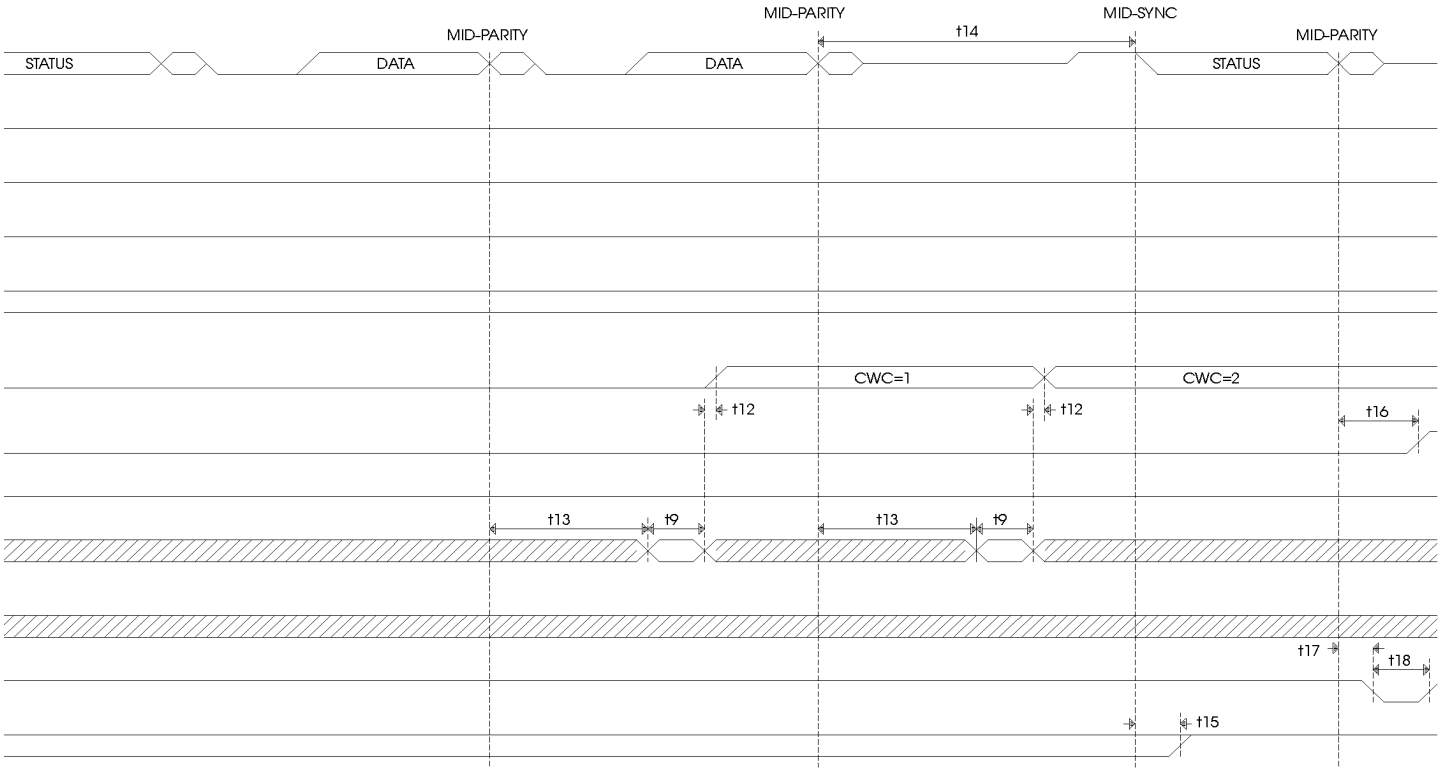


FIGURE 7. RT TO RT (RECEIVE) TIMING (CONTINUED)					
SYMBOL	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**
t12	END OF DATA TRANSFER CYLE TO VALID NEXT WC (Note 3)			60	ns
t13(@12MHz)	MID-PARITY CROSSING OF RECEIVED DATA WORD TO START OF DATA TRANSFER CYCLE (Note 2)	1.52		1.94	µs
t13(@16MHz)	MID-PARITY CROSSING OF RECEIVED DATA WORD TO START OF DATA TRANSFER CYCLE (Note 2)	1.23		1.57	µs
t14(@12MHz)	RT RESPONSE TIME	6.18		6.96	µs
t14(@16MHz)	RT RESPONSE TIME	6.0		6.76	µs
t15	MID-SYNC CROSSING OF STATUS RESPONSE TO $\overline{\text{RTFAIL}}$ RISING			100	ns
t16(@12MHz)	MID-PARITY CROSSING OF STATUS RESPONSE TO $\overline{\text{INCMD}}$ RISING	3.36		3.57	µs
t16(@16MHz)	MID-PARITY CROSSING OF STATUS RESPONSE TO $\overline{\text{INCMD}}$ RISING	3.26		3.45	µs
t17(@12MHz)	MID-PARITY CROSSING OF STATUS RESPONSE TO $\overline{\text{GBR}}$ FALLING	3.23		3.37	µs
t17(@16MHz)	MID-PARITY CROSSING OF STATUS RESPONSE TO $\overline{\text{GBR}}$ FALLING	3.17		3.29	µs
18(@12MHz)	$\overline{\text{GBR}}$ PULSE WIDTH	140		190	ns
t18(@16MHz)	$\overline{\text{GBR}}$ PULSE WIDTH	100		150	ns

Notes:
1)IF ADDR_ENA IS LOGIC “1”, $\overline{\text{CS}}$, $\overline{\text{WRT}}$, AND A13..A0 WILL BE IN A HIGH IMPEDANCE STATE EXCEPT FOR WHEN A WORD TRANSFER IS BEING PERFORMED ($\overline{\text{DT_ACK}}$ = LOGIC “0”).
2)THE LEADING EDGE OF TIME REFERENCE t9 AND THE TRAILING EDGE OF TIME REFERENCES t6 AND t13 ARE DEFINED AS THE FALLING EDGE OF $\overline{\text{DT_REQ}}$.
3)THE TRAILING EDGE OF REFERENCE t9 AND THE LEADING EDGE OF TIME REFERENCE t12 ARE DEFINED AS THE RISING EDGE OF $\overline{\text{DT_REQ}}$.
4)DATA TRANSFER CYCLE TIMING INFORMATION IS DESCRIBED IN OTHER FIGURES.

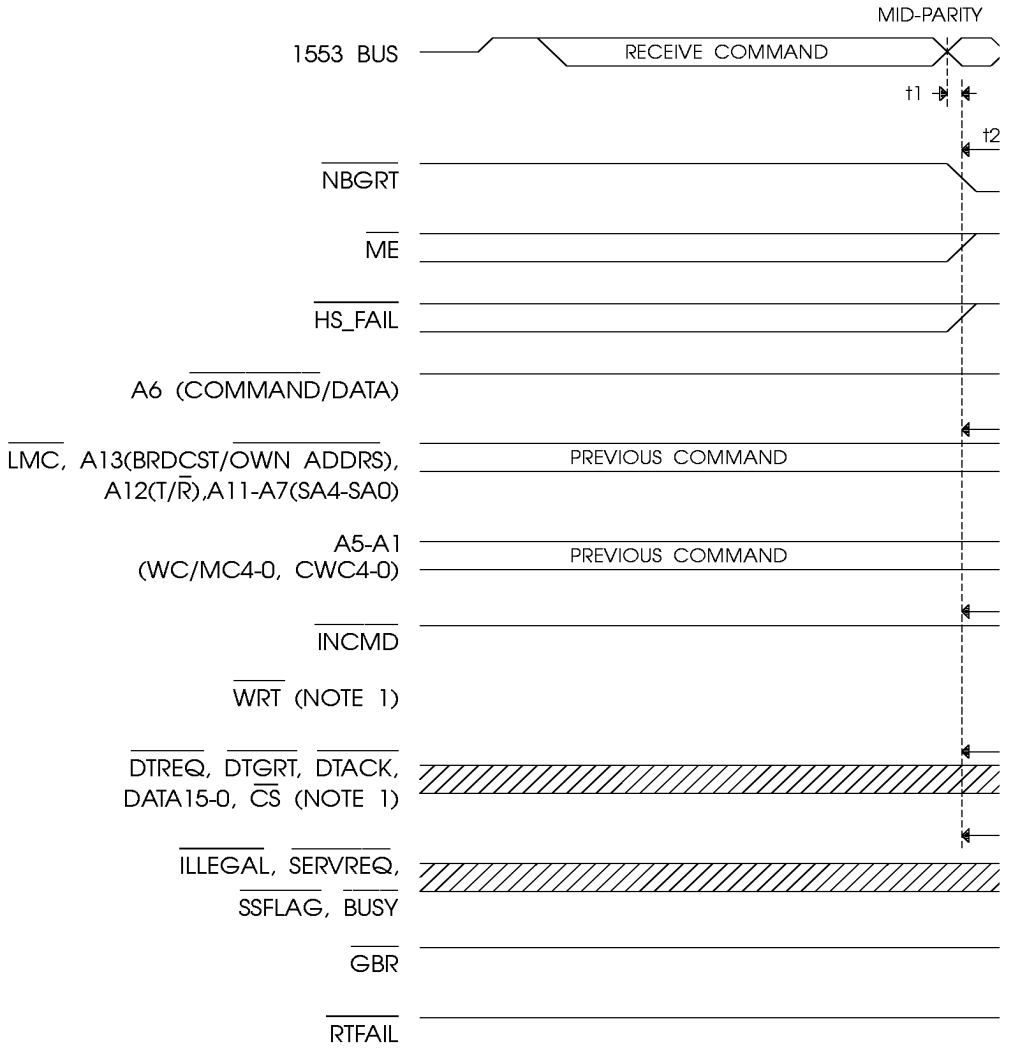


FIGURE 8. BC TO RT (RECEIVE) MESSAGE ERROR TIMING					
SYMBOL	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**
t1(@12MHz)	COMMAND MID-PARITY CROSSING TO FALLING EDGE OF $\overline{\text{NBGRT}}$	0.97		1.56	µs
t1(@16MHz)	COMMAND MID-PARITY CROSSING TO FALLING EDGE OF $\overline{\text{NBGRT}}$	0.87		1.38	µs
t2(@12MHz)	$\overline{\text{NBGRT}}$ PULSE WIDTH	140		190	ns
t2(@16MHz)	$\overline{\text{NBGRT}}$ PULSE WIDTH	100		150	ns
t3	$\overline{\text{NBGRT}}$ RISING EDGE TO $\overline{\text{A6}}$ FALLING EDGE			45	ns
t4(@12MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO ADDRESS VALID, $\overline{\text{LMC}}$	300		410	ns
t4(@16MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO VALID ADDRESS, $\overline{\text{LMC}}$	220		330	ns
t5(@12MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO $\overline{\text{INCMD}}$ FALLING EDGE	800		865	ns
t5(@16MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO $\overline{\text{INCMD}}$ FALLING EDGE	590		655	ns
t6(@12MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO START OF DATA TRANSFER CYCLE	1.19		1.28	µs
t6(@16MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO START OF DATA TRANSFER CYCLE (Note 2)	See Note 4			
t7	$\overline{\text{NBGRT}}$ FALLING EDGE TO VALID STATUS INPUTS			4.1	µs
t8	$\overline{\text{INCMD}}$ FALLING EDGE TO CWC VALID	5		60	ns
t9	DATA TRANSFER CYCLE TIME (Notes 2,3,4)				

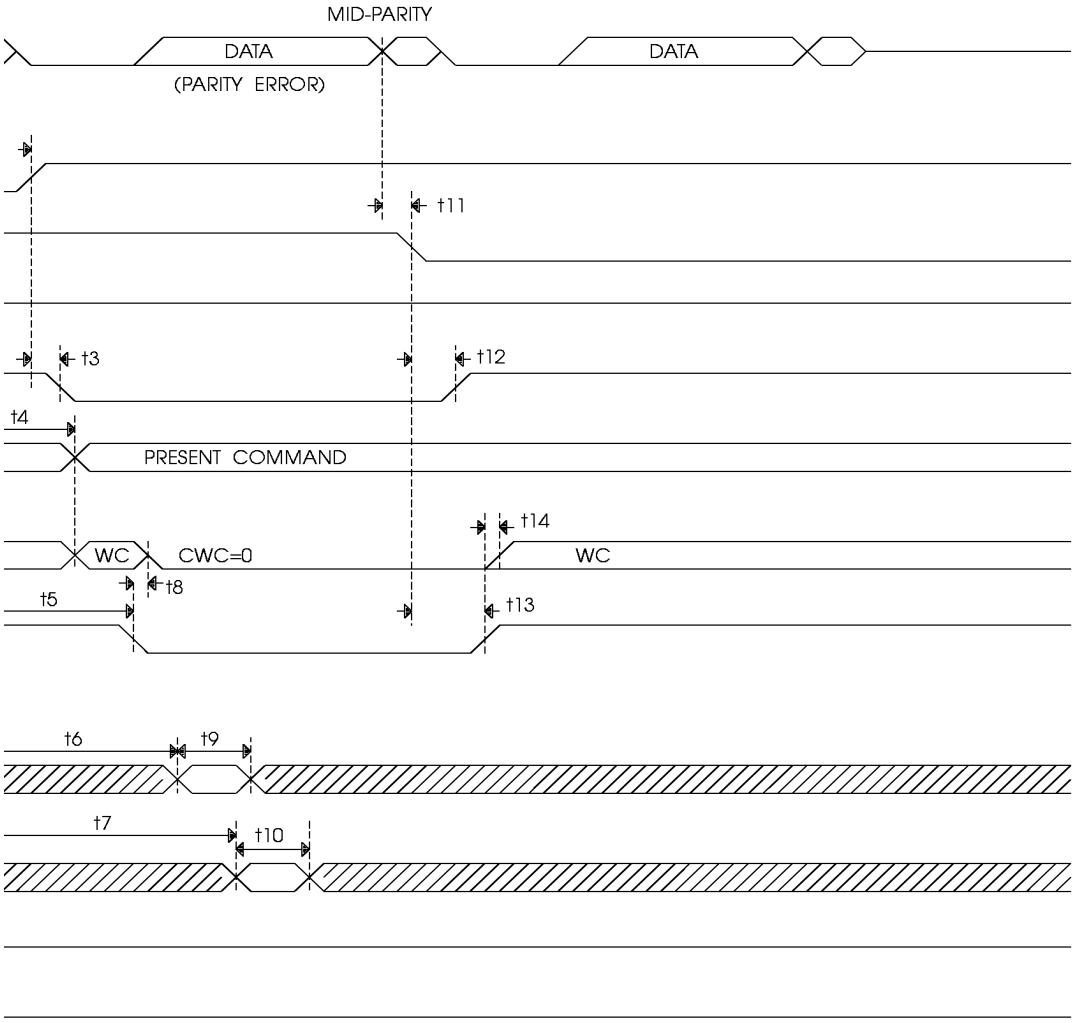


FIGURE 8. BC TO RT (RECEIVE) MESSAGE ERROR TIMING					
SYMBOL	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**
t10	STATUS INPUTS HOLD TIME	500			ns
t11(@12MHz)	MID-PARITY CROSSING OF DATA WORD WITH EVEN PARITY TO FALLING EDGE OF $\overline{ME}$	5.95		6.26	ms
t11(@16MHz)	MID-PARITY CROSSING OF DATA WORD WITH EVEN PARITY TO FALLING EDGE OF $\overline{ME}$	5.87		6.245	µs
t12	$\overline{ME}$ FALLING EDGE TO A6 HIGH			45	ns
t13(@12MHz)	$\overline{ME}$ FALLING EDGE TO $\overline{INCMD}$ RISING EDGE	300		360	ns
t13(@16MHz)	$\overline{ME}$ FALLING EDGE TO $\overline{INCMD}$ RISING EDGE	220		280	ns
t14	INCMD RISING EDGE TO WORD COUNT VALID			75	ns

Notes:
1)IF ADDR_ENA IS LOGIC “1”, $\overline{CS}$, $\overline{WRT}$, AND A13..A0 WILL BE IN A HIGH IMPEDANCE STATE EXCEPT FOR WHEN A WORD TRANSFER IS BEING PERFORMED ($\overline{DT_ACK}$ = LOGIC “0”).
2)THE LEADING EDGE OF TIME REFERENCE t9 AND THE TRAILING EDGE OF TIME REFERENCE t6 IS DEFINED AS THE FALLING EDGE OF $\overline{DT_REQ}$.
3)THE TRAILING EDGE OF REFERENCE t9 IS DEFINED AS THE RISING EDGE OF $\overline{DT_REQ}$.
4)DATA TRANSFER CYCLE TIMING INFORMATION IS DESCRIBED IN OTHER FIGURES.

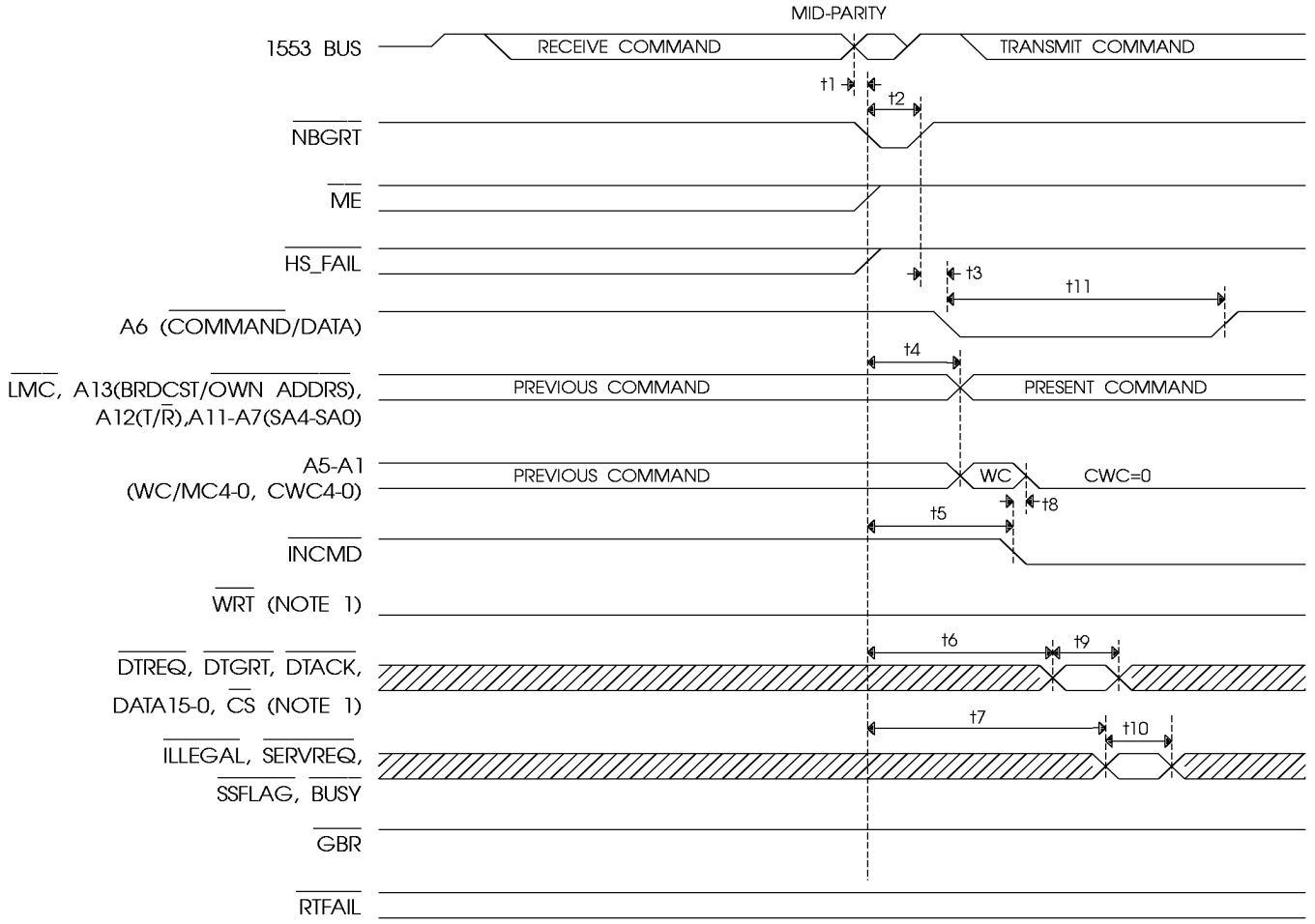


FIGURE 9. RT TO RT (RECEIVE) TIMEOUT TIMING					
SYMBOL	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**
t1(@12MHz)	COMMAND MID-PARITY CROSSING TO FALLING EDGE OF $\overline{\text{NBGRT}}$	0.97		1.56	ms
t1(@16MHz)	COMMAND MID-PARITY CROSSING TO FALLING EDGE OF $\overline{\text{NBGRT}}$	0.87		1.38	ms
t2(@12MHz)	$\overline{\text{NBGRT}}$ PULSE WIDTH	140		190	ns
t2(@16MHz)	$\overline{\text{NBGRT}}$ PULSE WIDTH	100		150	ns
t3	$\overline{\text{NBGRT}}$ RISING EDGE TO $\overline{\text{A6}}$ FALLING EDGE			45	ns
t4(@12MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO ADDRESS VALID, $\overline{\text{LMC}}$	300		410	ns
t4(@16MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO VALID ADDRESS, $\overline{\text{LMC}}$	220		330	ns
t5(@12MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO $\overline{\text{INCMD}}$ FALLING EDGE	800		865	ns
t5(@16MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO $\overline{\text{INCMD}}$ FALLING EDGE	590		655	ns
t6(@12MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO START OF DATA TRANSFER CYCLE	1.19		1.28	ms
t6(@16MHz)	$\overline{\text{NBGRT}}$ FALLING EDGE TO START OF DATA TRANSFER CYCLE (Note 2)	0.88		0.97	ms
t7	$\overline{\text{NBGRT}}$ FALLING EDGE TO VALID STATUS INPUTS			4.1	ms
t8	$\overline{\text{INCMD}}$ FALLING EDGE TO CWC VALID	5		60	
t9	DATA TRANSFER CYCLE TIME (Notes 2,3,4)	See Note 4			

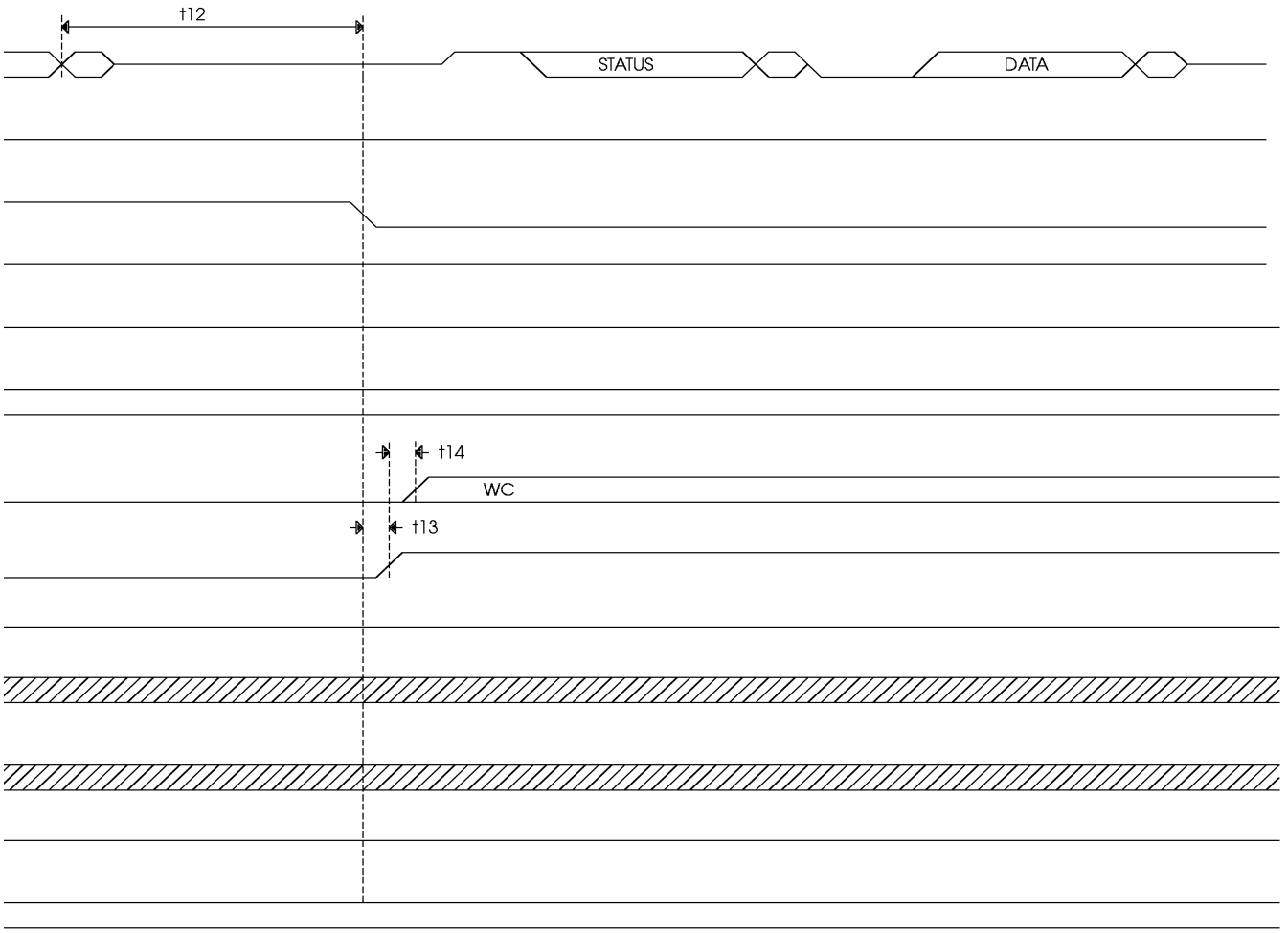


FIGURE 9. RT TO RT (RECEIVE) TIMEOUT TIMING (CONTINUED)					
SYMBOL	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**
t10	STATUS INPUTS HOLD TIME	500			ns
t11(@12MHz)	A6 PULSE WIDTH	820		1205	ns
t11(@16MHz)	A6 PULSE WIDTH	720		1025	ns
t12	RT-RT NO RESPONSE TIMEOUT (MESSAGE ERROR)	18.25		19.5	ms
t13(@12MHz)	$\overline{ME}$ FALLING EDGE TO $\overline{INCMD}$ RISING EDGE	300		360	ns
t13(@16MHz)	$\overline{ME}$ FALLING EDGE TO $\overline{INCMD}$ RISING EDGE	220		280	ns
t14	$\overline{INCMD}$ RISING EDGE TO WORD COUNT VALID			75	ns

Notes:
1)IF ADDR_ENA IS LOGIC “1”, $\overline{CS}$, $\overline{WRT}$, AND A13..A0 WILL BE IN A HIGH IMPEDANCE STATE EXCEPT FOR WHEN A WORD TRANSFER IS BEING PERFORMED ($\overline{DT_ACK}$ = LOGIC “0”).
2)THE LEADING EDGE OF TIME REFERENCE t9 AND THE TRAILING EDGE OF TIME REFERENCE t6 IS DEFINED AS THE FALLING EDGE OF $\overline{DT_REQ}$.
3)THE TRAILING EDGE OF REFERENCE t9 IS DEFINED AS THE RISING EDGE OF $\overline{DT_REQ}$.
4)DATA TRANSFER CYCLE TIMING INFORMATION IS DESCRIBED IN OTHER FIGURES.

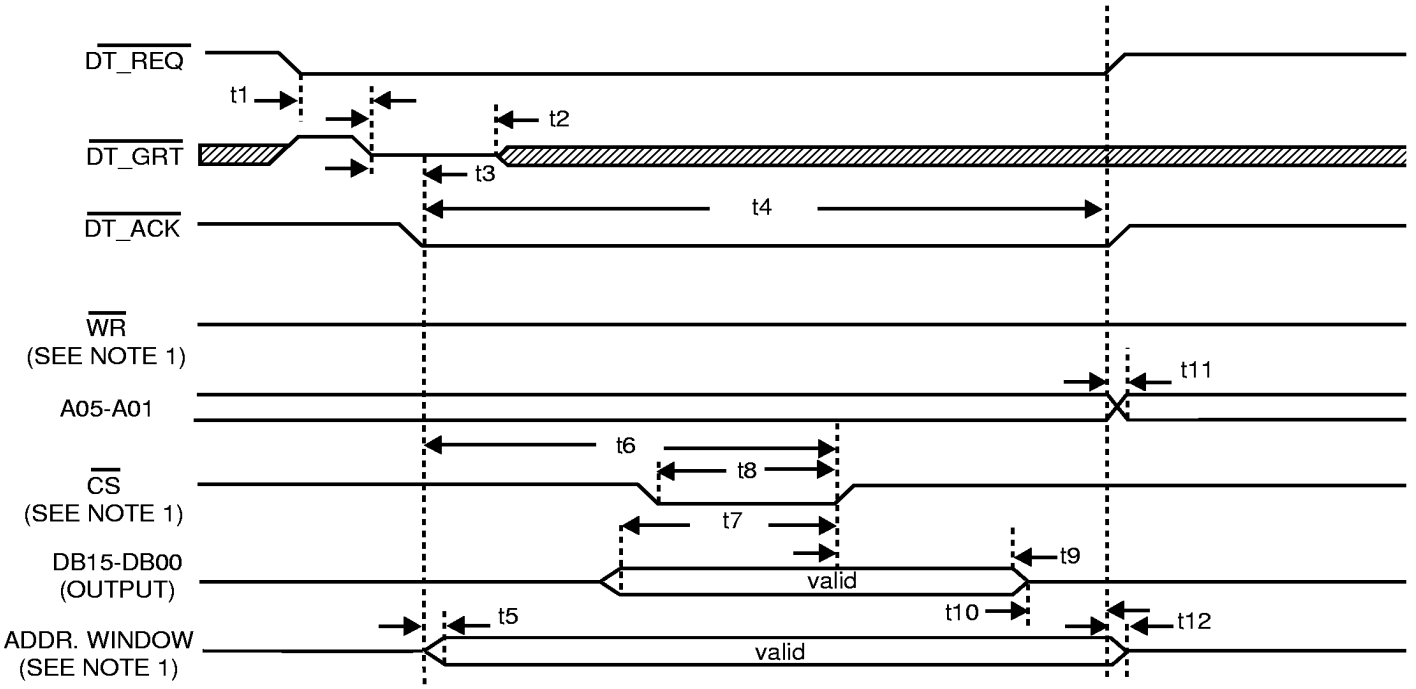


FIGURE 10. DMA WRITE 16-BIT					
SYMBOL	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**
t1(@12MHz)	DMA REQUEST TO DMA GRANT (COMMAND WORD)			3.0	µs
t1(@16MHz)	DMA REQUEST TO DMA GRANT (COMMAND WORD)			3.3	µs
t1(@12MHz)	DMA REQUEST TO DMA GRANT (DATA WORD)			3.5	µs
t1(@16MHz)	DMA REQUEST TO DMA GRANT (DATA WORD)			3.7	µs
t2	DMA GRANT PULSE WIDTH	130			ns
t3	DMA GRANT DELAY TO DMA ACKNOWLEDGE			130	ns
t4	$\overline{\text{DT_ACK}}$ PULSE WIDTH	485		515	ns
t5	$\overline{\text{DT_ACK}}$ LOW DELAY TO ADDRESS ENABLED (Note 1)			35	ns
t6(@12MHz)	$\overline{\text{DT_ACK}}$ LOW DELAY TO RISING EDGE OF $\overline{\text{CS}}$	315		365	ns
t6(@16MHz)	$\overline{\text{DT_ACK}}$ LOW DELAY TO RISING EDGE OF $\overline{\text{CS}}$	360		410	ns
t7(@12MHz)	DATA VALID SETUP TIME TO RISING EDGE OF $\overline{\text{CS}}$	195			ns
t7(@16MHz)	DATA VALID SETUP TIME TO RISING EDGE OF $\overline{\text{CS}}$	255			ns
t8(@12MHz)	$\overline{\text{CS}}$ LOW PULSE WIDTH	150		185	ns
t8(@16MHz)	$\overline{\text{CS}}$ LOW PULSE WIDTH	170		205	ns
t9(@12MHz)	DATA HOLD TIME FOLLOWING RISING EDGE OF $\overline{\text{CS}}$	70			ns
t9(@16MHz)	DATA HOLD TIME FOLLOWING RISING EDGE OF $\overline{\text{CS}}$	50			ns
t10	DATA TRI-STATE SETUP TIME PRIOR TO RISING EDGE OF $\overline{\text{DT_REQ}}$, $\overline{\text{DT_ACK}}$	10			ns
t11	$\overline{\text{DT_REQ}}$ HIGH DELAY TO ADDRESS UPDATE (Note 1)			60	ns
t12	$\overline{\text{DT_ACK}}$ HIGH DELAY TO ADDRESS, $\overline{\text{WRT}}$, $\overline{\text{CS}}$ TRI-STATE (Note 1)			45	ns

Note:
1)Diagram assumes $\overline{\text{ADDR_ENA}}$ is set to logic “0”. If is was set to logic “1”, then A13-A00, $\overline{\text{CS}}$, and $\overline{\text{WRT}}$ would normally be high impedance until activated by $\overline{\text{DT_ACK}}$ as shown by “ADDR. WINDOW” timing.

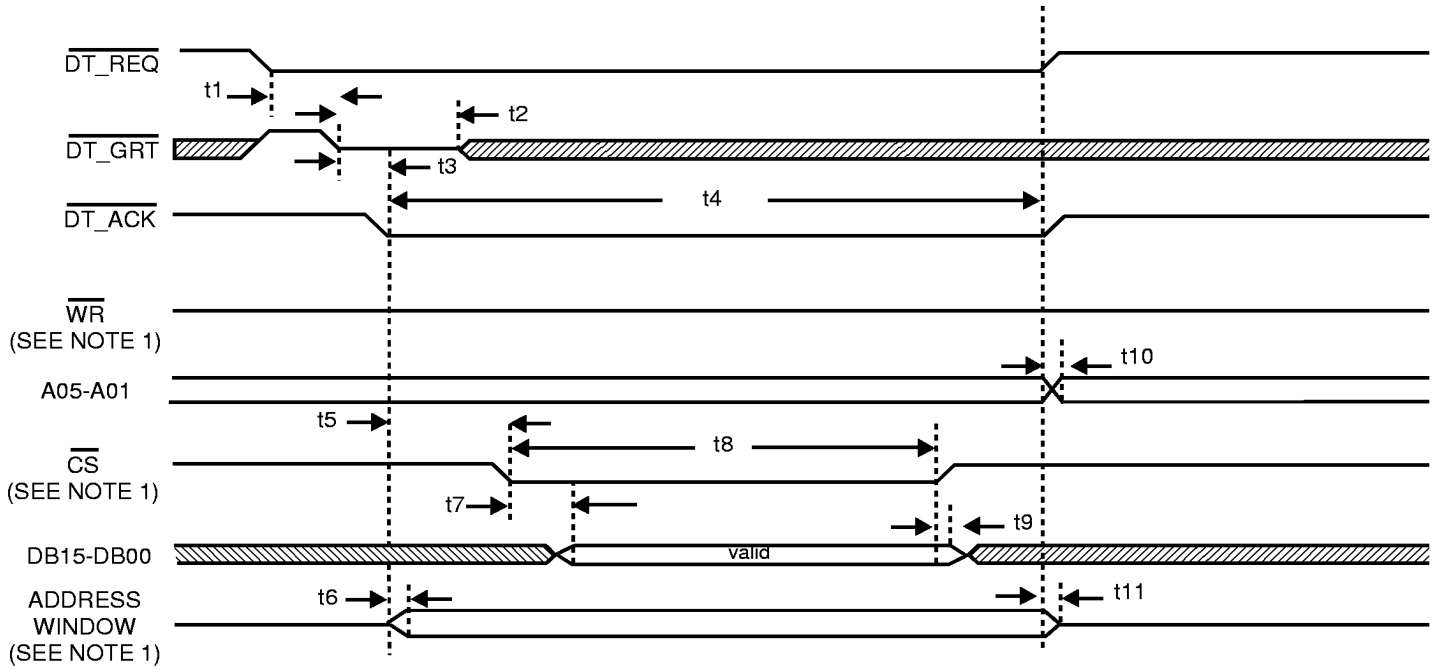


FIGURE 11. DMA READ 16-BIT					
SYMBOL	**DESCRIPTION**	**NIN**	**TYP**	**MAX**	**UNITS**
t1(@12MHz)	DMA REQUEST TO DMA GRANT			15.1	µs
t1(@16MHz)	DMA REQUEST TO DMA GRAN)			15.3	µs
t2	DMA GRANT PULSE WIDTH	130			ns
t3	DMA GRANT DELAY TO DMA ACKNOWLEDGE			130	ns
t4	$\overline{\text{DT_ACK}}$ PULSE WIDTH	485		515	ns
t5(@12MHz)	$\overline{\text{DT_ACK}}$ LOW DELAY TO $\overline{\text{CS}}$ LOW	70		115	ns
t5(@16MHz)	$\overline{\text{DT_ACK}}$ LOW DELAY TO $\overline{\text{CS}}$ LOW	50		95	ns
t6	$\overline{\text{DT_ACK}}$ LOW DELAY TO ADDRESS, $\overline{\text{WRT}}$, $\overline{\text{CS}}$, ENABLED (Note 1			35	ns
t7(@12MHz)	DATA VALID SETUP TIME TO RISING EDGE OF $\overline{\text{CS}}$			180	ns
t7(@16MHz)	DATA VALID SETUP TIME TO RISING EDGE OF $\overline{\text{CS}}$			240	ns
t8(@12MHz)	$\overline{\text{CS}}$ LOW PULSE WIDTH	315		345	ns
t8(@16MHz)	$\overline{\text{CS}}$ LOW PULSE WIDTH	360		390	ns
t9(@12MHz)	DATA HOLD TIME FOLLOWING $\overline{\text{CS}}$ HIGH	0			ns
t10	$\overline{\text{DT_REQ}}$ HIGH DELAY TO ADDRESS UPDATE (Note 1)			60	ns
112	$\overline{\text{DT_ACK}}$ HIGH DELAY TO ADDRESS, $\overline{\text{WRT}}$, $\overline{\text{CS}}$ TRI-STATE (Note 1)			45	ns

Note:
1)Diagram assumes $\overline{\text{ADDR_ENA}}$ is set to logic “0”" If is was set to logic “1”, then A13-A00, $\overline{\text{CS}}$, and $\overline{\text{WRT}}$ would normally be high impedance until activated by $\overline{\text{DT_ACK}}$ as shown by “ADDRESS WINDOW” timing.

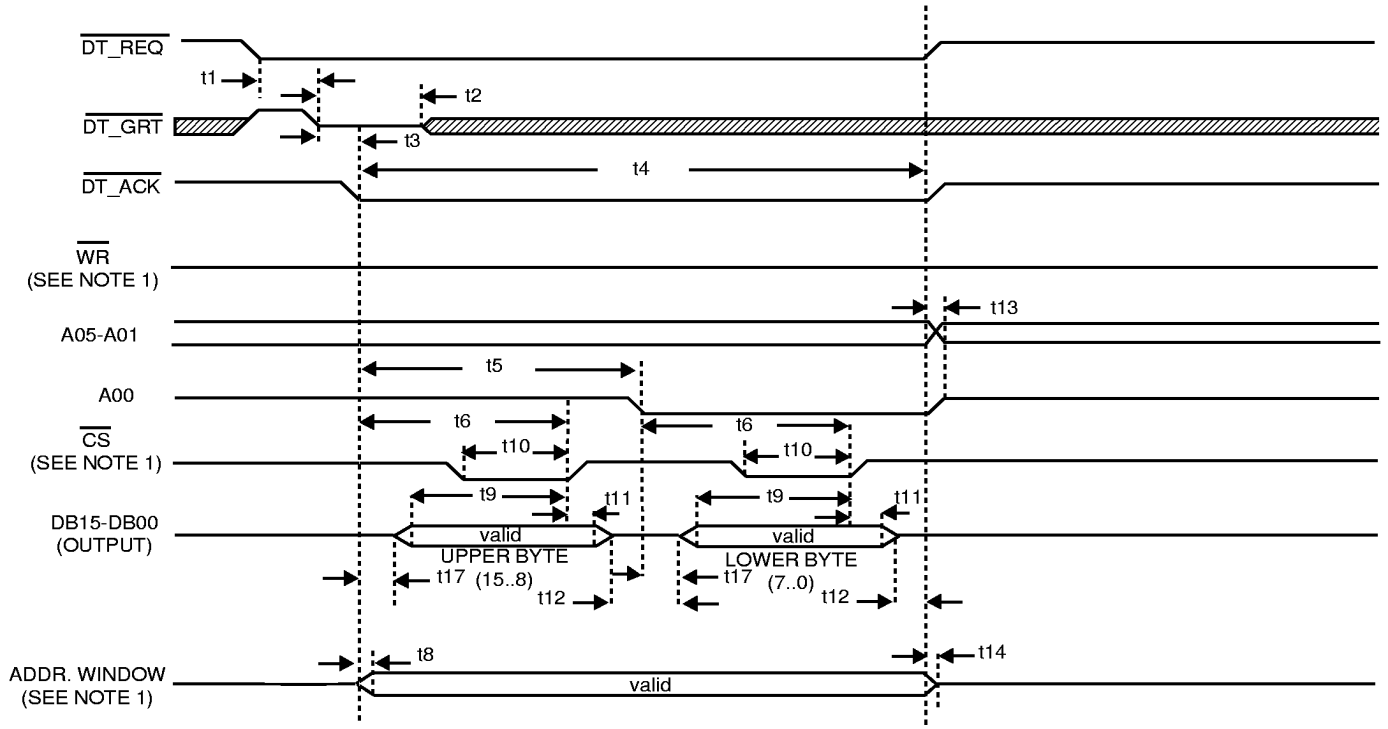


FIGURE 12. DMA WRITE 8-BIT					
SYMBOL	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**
t1(@12MHz)	DMA REQUEST TO DMA GRANT (COMMAND WORD)			3.0	µs
t1(@16MHz)	DMA REQUEST TO DMA GRANT (COMMAND WORD)			3.3	µs
t1(@12MHz)	DMA REQUEST TO DMA GRANT (DATA WORD)			3.5	µs
t1(@16MHz)	DMA REQUEST TO DMA GRANT (DATA WORD)			3.7	µs
t2	DMA GRANT PULSE WIDTH	130			ns
t3	DMA GRANT DELAY TO DMA ACKNOWLEDGE			130	ns
t4	$\overline{\text{DT_ACK}}$ PULSE WIDTH	985		1015	ns
t5	$\overline{\text{DT_ACK}}$ LOW DELAY TO A0 LOW (UPPER BYTE TRANSFER CYCLE TIME	485		515	ns
t6(@12MHz)	START OF BYTE TRANSFER CYCLETO RISING EDGE OF $\overline{\text{CS}}$	315		365	ns
t6(@16MHz)	START OF BYTE TRANSFER CYCLETO RISING EDGE OF $\overline{\text{CS}}$	360		410	ns
t7	DATA TRI-STATE HOLD TIME FOLLOWING START OF BYTE TRANSFER	50			???ns
t8	$\overline{\text{DT_ACK}}$ LOW DELAY TO ADDRESS, $\overline{\text{WRT}}$, $\overline{\text{CS}}$ ENABLED (Note 1)	35			???ns
t9(@12MHz)	DATA SETUP TIME PRIOR TO RISING EDGE OF $\overline{\text{CS}}$	195			ns
t9(@16MHz)	DATA SETUP TIME PRIOR TO RISING EDGE OF $\overline{\text{CS}}$	255			ns
t10(@12MHz)	$\overline{\text{CS}}$ PULSE WIDTH	150			ns
t10(@16MHz)	$\overline{\text{CS}}$ PULSE WIDTH	170			ns
t11(@12MHz)	DATA HOLD TIME FOLLOWING RISING EDGE OF $\overline{\text{CS}}$	70			ns
t11(@16MHz)	DATA HOLD TIME FOLLOWING RISING EDGE OF $\overline{\text{CS}}$	50			ns
t12	DATA TRI-STATE SETUP TIME PRIOR TO END OF BYTE TRANSFER CYCLE	10			ns
t13	$\overline{\text{DT_REQ}}$ HIGH DELAY TO ADDRESS UPDATE (Note 1)			60	ns
t14	$\overline{\text{DT_ACK}}$ HIGH DELAY TO ADDRESS, $\overline{\text{WRT}}$, $\overline{\text{CS}}$ HIGH IMPEDANCE (Note 1)			45	ns

Note:
1)Diagram assumes $\overline{\text{ADDR_ENA}}$ is set to logic “0”. If is was set to logic “1”, then A13-A00, $\overline{\text{CS}}$, and $\overline{\text{WRT}}$ would normally be high impedance until activated by $\overline{\text{DT_ACK}}$ as shown by “ADDR. WINDOW” timing.

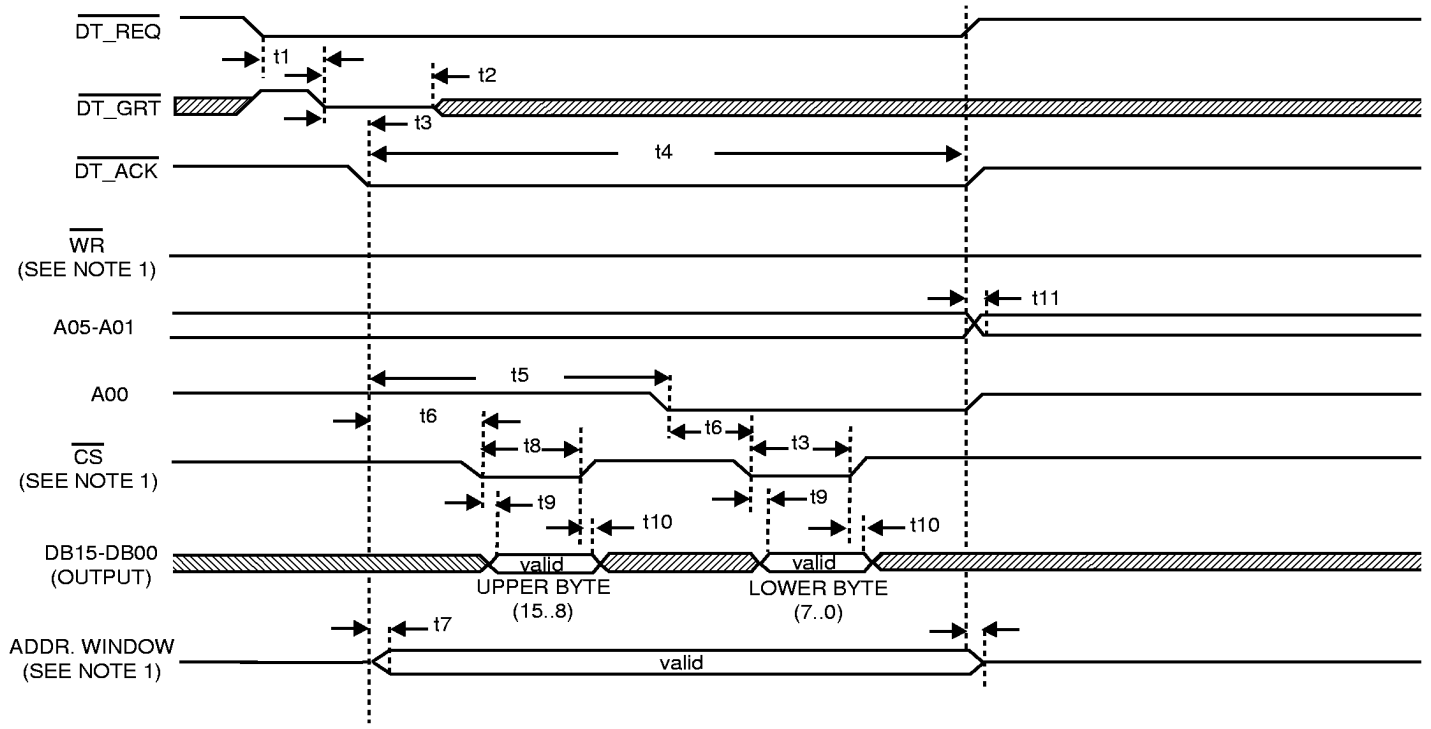


FIGURE 13. DMA READ 8-BIT					
SYMBOL	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**
t1(@12MHz)	DMA REQUEST TO DMA GRANT			15.1	µs
t1(@16MHz)	DMA REQUEST TO DMA GRAN)			15.3	µs
t2	DMA GRANT PULSE WIDTH	130			ns
t3	DMA GRANT DELAY TO DMA ACKNOWLEDGE			130	ns
t4	$\overline{\text{DT_ACK}}$ PULSE WIDTHACK PULSE WIDTH	985		1015	ns
t5	$\overline{\text{DT_ACK}}$ DELAY TO A0 LOW (UPPER BYTE TRANSFER CYCLE TIME)	485		515	ns
t6(@12MHz)	START OF BYTE TRANSFER CYCLE TO FALLING EDGE OF $\overline{\text{CS}}$	70		115	ns
t6(@16MHz)	START OF BYTE TRANSFER CYCLE TO FALLING EDGE OF $\overline{\text{CS}}$	50		95	ns
t7	$\overline{\text{DT_ACK}}$ LOW DELAY TO ADDRESS, $\overline{\text{WRT}}$, $\overline{\text{CS}}$ ENABLED (Note 1)			35	ns
t8(@12MHz)	$\overline{\text{CS}}$ PULSE WIDTH	315		345	ns
t8(@16MHz)	$\overline{\text{CS}}$ PULSE WIDTH	360		390	ns
t10	DATA HOLD TIME FOLLOWING $\overline{\text{CS}}$ HIGH	0			ns
t11	$\overline{\text{DT_REQ}}$ HIGH DELAY TO ADDRESS UPDATE (Note 1)			60	ns
112	$\overline{\text{DT_ACK}}$ HIGH DELAY TO ADDRESS, $\overline{\text{WRT}}$, $\overline{\text{CS}}$ TRI-STATE (Note 1)			45	ns

Note:
1)Diagram assumes $\overline{\text{ADDR_ENA}}$ is set to logic “0”. If is was set to logic “1”, then A13-A00, $\overline{\text{CS}}$, and $\overline{\text{WRT}}$ would normally be high impedance until activated by $\overline{\text{DT_ACK}}$ as shown by “ADDR. WINDOW” timing

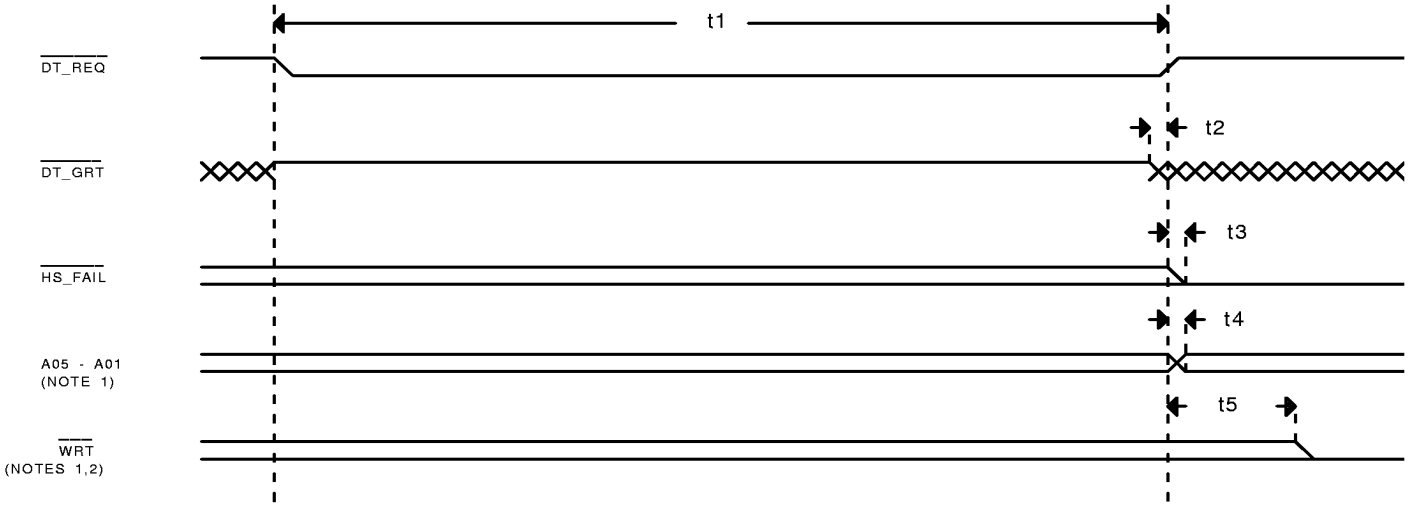


FIGURE 14. DMA HANDSHAKE FAILURE						
SYMBOL	**TRANSFER**	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**
t1(@12MHz)	COMMAND WORD WRITE	$\overline{\text{DT_REQ}}$ PULSE WIDTH	3.2		3.3	µs
t1(@16MHz)	COMMAND WORD WRITE	$\overline{\text{DT_REQ}}$ PULSE WIDTH	3.5		3.6	µs
t1(@12MHz)	DATA WORD WRITE	$\overline{\text{DT_REQ}}$ PULSE WIDTH	3.7		3.8	µs
t1(@16MHz)	DATA WORD WRITE	$\overline{\text{DT_REQ}}$ PULSE WIDTH	3.9		4.0	µs
t1(@12MHz)	DATA WORD WRITE	$\overline{\text{DT_REQ}}$ PULSE WIDTH			15.3	µs
t1(@16MHz)	DATA WORD WRITE	$\overline{\text{DT_REQ}}$ PULSE WIDTH			15.5	µs
t2	ALL	DT_GRT HIGH HOLD TIME FROM $\overline{\text{DT_REQ}}$ RISING	-60			ns
t3	ALL	$\overline{\text{HS_FAIL}}$ FALLING EDGE FROM $\overline{\text{DT_REQ}}$ RISING EDGE			25	ns
t4	ALL	WORD COUNT VALID FROM $\overline{\text{DT_REQ}}$ RISING EDGE			60	ns
t6(@12MHz)	DATA WORD READ	$\overline{\text{DT_REQ}}$ RISING EDGE TO $\overline{\text{WRT}}$ LOW	300		400	ns
t6(@16MHz)	DATA WORD READ	$\overline{\text{DT_REQ}}$ RISING EDGE TO $\overline{\text{WRT}}$ LOW	220		310	ns

Notes:
1)Diagram assumes $\overline{\text{ADDR_ENA}}$ is set to logic “0”. If it was set to logic “1” then A13-A00, $\overline{\text{CS}}$ and $\overline{\text{WRT}}$ would normally be in high impedance until activated by $\overline{\text{DT_ACK}}$ as shown by “ADDR. WINDOW” timing.
2)If the transfer requested was a read operation, and a handshake failure occurred, then the WRT signal would return to the write state and the BUS-65153's transmission of the 1553 Bus would terminate at the conclusion of the preset word.

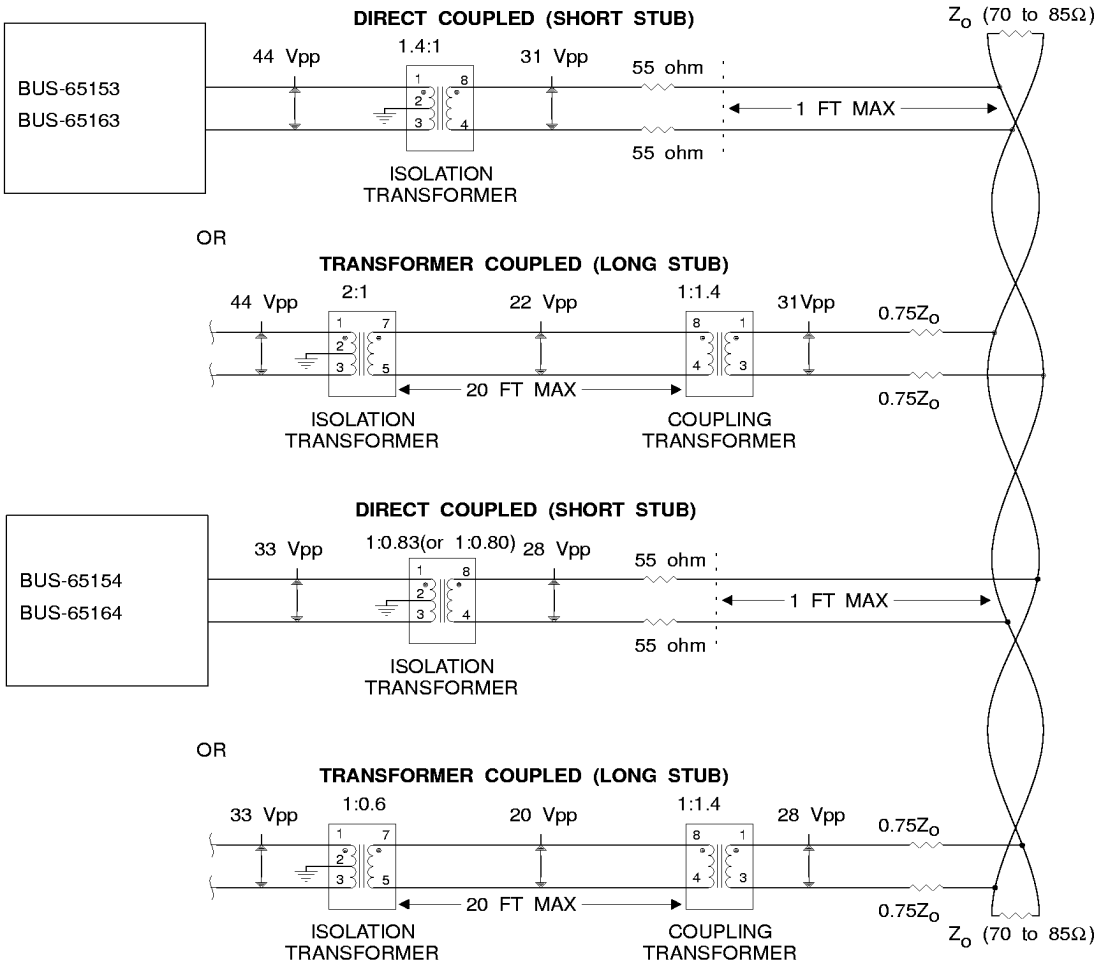


FIGURE 15. BUS-65153 AND BUS-65154 TO MIL-STD-1553 INTERFACE

INTERFACE TO MIL-STD-1553 BUS

Interfacing the BUS-65153 to a MIL-STD-1553 bus requires a pair of pulse transformers. These transformers, or QPL equivalents, are available from Beta Transformer Technology Corporation, a subsidiary of DDC. The BUS-65153 hybrid and Beta Transformers may be wired for either direct coupled or stub coupled configurations. The recommended transformer for each of the BUS-65153 transceiver options is listed in TABLE 4.

The interface between a BUS-65153 and a MIL-STD-1553 bus is illustrated in FIGURE 15.Notes for TABLE 4:

TABLE 4. RECOMMENDED BETA TRANSFORMEER	
DEVICE	**TRANSFORMER**
BUS-65153/63	BUS-25679, B-2203, LPB-5002 LPB-5009, or M21038/27-02
BUS-65154/64	BUS-29854, B-2204 LPB-5001, LPB-5008 or M21038/27-03

Notes for TABLE 4:
(1)Shown for one of two redundant buses that interface to the BUS-65153 hybrid.
(2)Transmitted voltage level on 1553 bus is 6 Vp-p min, 7 Vp-p nominal, 9 Vp-p max.
(3)Required tolerance on isolation resistors is 2%. Instantaneous power dissipation (when transmitting) is approximately 0.5 W (typ), 0.8 W (max).
(4)Transformer pin numbering is correct for DDC BUS-25679 or BUS-29854 transformer. For the Beta transformer (e.g., B-2203) or the QPL-21038-31 transformer (e.g., M21038/27-02), the winding sense and turns ratio are mechanically the same, but the pin numbering is reversed. Therefore, it is necessary to reverse pins 8 and 4 or pins 7 and 5 in the diagram for the Beta or QPL transformers.
(5) The B-2204, B-2388, and B-2344 transformers have a slightly different turns ratio on the direct coupled taps then the turns ratio of the BUS-29854 direct coupled taps. They do, however, have the same transformer coupled ratio. For transformer coupled applications, either transformer may be used. The transceiver in the BU-65170X2 and the BU-61580X2 was designed to work with a 1:0.83 ratio for direct coupled applications. For direct coupled applications, the 1.20:1 turns ratio is recommended, but the 1.25:1 may be used. The 1.25:1 turns ratio will result in a slightly lower transmitter amplitude. (Approximately 3.6% lower) and a slight shift in the ACE's receiver threshold.

SIMPLE SYSTEM INTERFACE

FIGURE 16 illustrates the capability of the STIC to operate in a system with no host processor. A simple linear addressing scheme is used that can be easily decoded to form read and write signals for direct access to data buffers or data latches. A double buffered mechanism may be used on received data in order to maintain data validity and consistency.

The latched discrete outputs section of the drawing uses two sets of latches. The first latch is updated when the received data word is transferred from the STIC. The second latch is not updated until the message is validated, as indicated by the signal Good Block Received ($\overline{GBR}$). If an error, such as parity or Manchester, occurs on a received data word, all the data associated with that message will be ignored, thus fulfilling the data validity/consistancy requirement.

DMA INTERFACE

The STIC may be interfaced to a host processor by means of a simple DMA interface. The address and control lines may be placed in a three-state mode by setting the $\overline{ADDR_ENA}$ signal to logic "1". While the STIC is not accessing the RAM (i.e., $\overline{DT_ACK}$ is logic "1") the address, data, and control lines ($\overline{CS}$, $\overline{WRT}$) are held in a high impedance state. The signals $\overline{CS}$ and $\overline{WRT}$ require pull-up resistors.

The STIC may be programmed to operate in either a 16-bit transfer mode (FIGURE 17) or an 8-bit transfer mode (FIGURE 18). In 16-bit mode (DB_SEL set to logic "0") the signal A0 is not used (always logic "1") and 16-bit transfers are performed on data lines D0..D15. In 8-bit mode (DB_SEL set to logic "1") the signal A0 is used to indicate whether the upper (MSB) data byte (A0 set to logic "1") or the lower (LSB) data byte (A0 set to logic "0") is being transferred. The upper and lower data bytes are not multiplexed internally, therefore, the signals must be connected externally. D0 must be connected to D8, D1 must be connected to D9, ... , and D7 must be connected to D15

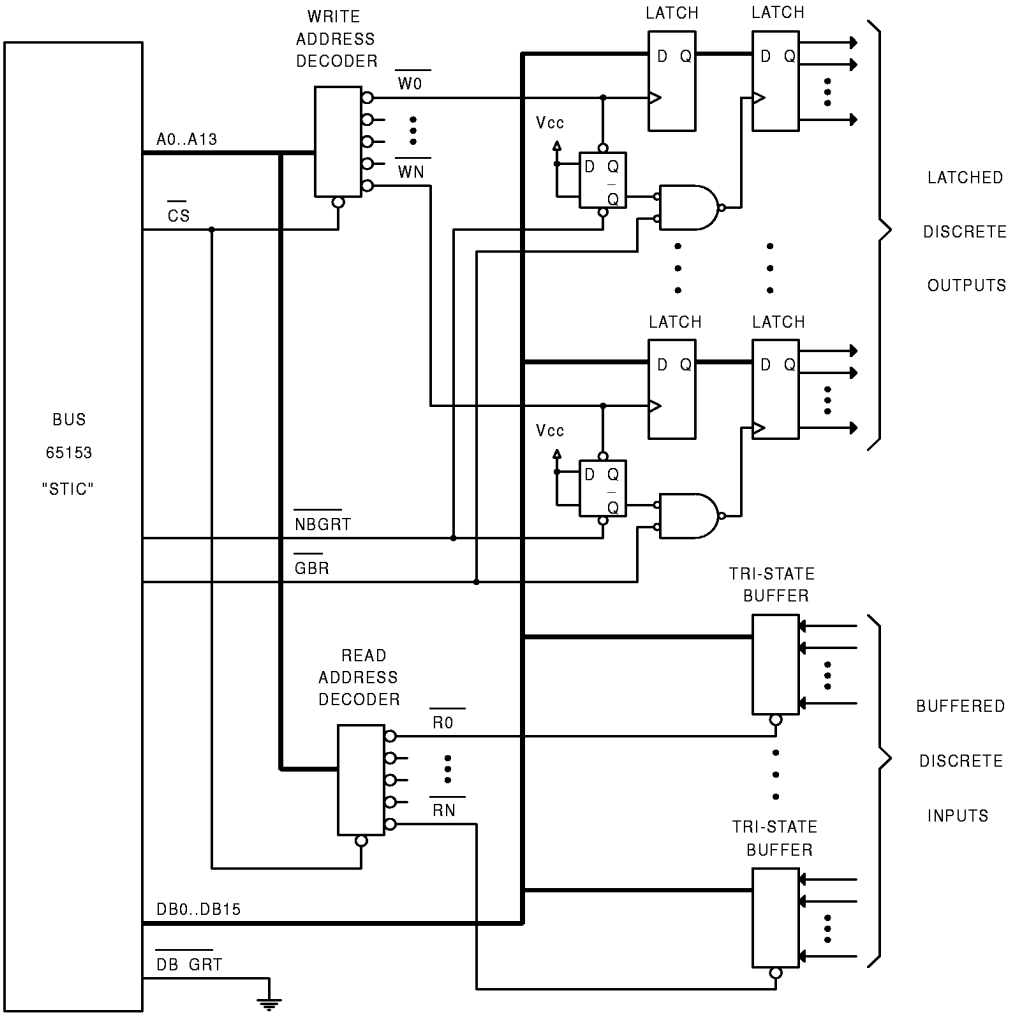


FIGURE 16. BUS-65153 MINIMUM COMPLEXITY SYSTEM

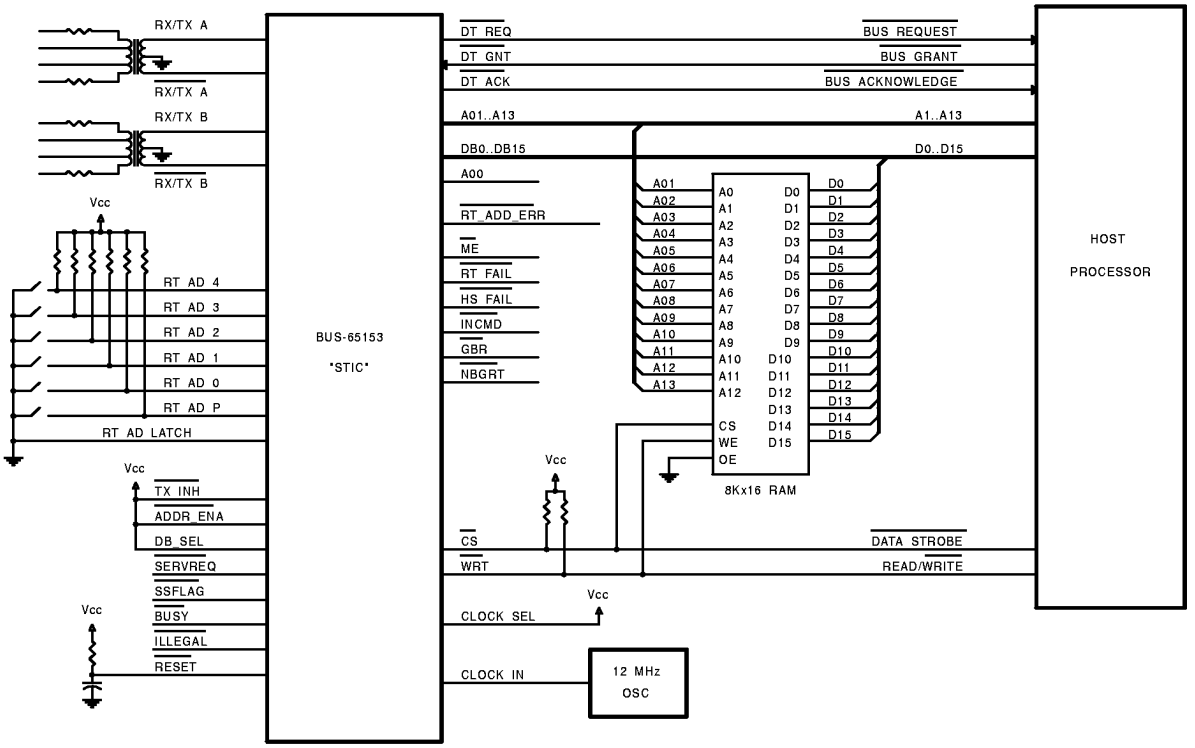


FIGURE 17. BUS-65153 16-BIT DMA INTERFACE

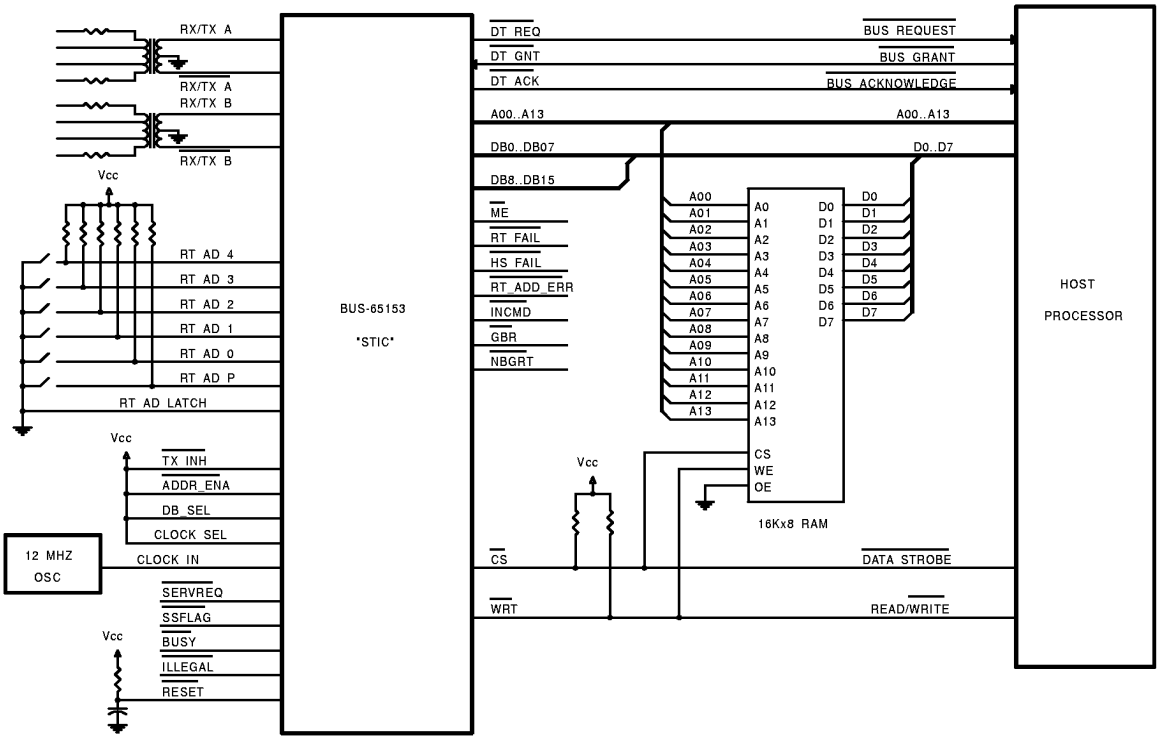


FIGURE 18. BUS-65153 8-BIT DMA INTERFACE

P.C. BOARD LAYOUT GUIDELINES

GROUND PLANES

As is the rule in all high speed digital circuits, it is good practice to use ground and power supply planes under the STIC hybrid as well as the associated components.

> IT IS VERY IMPORTANT THAT THERE BE NO GROUND AND/OR POWER SUPPLY PLANES UNDERNEATH ANY OF THE ANALOG BUS SIGNAL TRACES-THIS APPLIES TO THE TX/RX SIGNALS RUNNING FROM THE STIC HYBRID TO THE TRANSFORMERS AS WELL AS FROM THE TRANSFORMERS TO ANY CONNECTORS OR CABLES LEAVING THE BOARD

The reason for not using supply or ground planes under the analog signal traces is that the effect of the distributed capacitance will be to lower the input impedance of the terminal, as seen from the 1553 bus. MIL-STD-1553 requires a minimum input impedance of 2000 ohms for direct coupled terminals and 1000 ohms for transformer (stub) coupled terminals. If there are ground planes under the analog bus signal traces, it is likely that the terminal will not meet this requirement.

POWER AND GROUND DISTRIBUTION

Another important consideration is power and ground distribution. Refer to FIGURE 19. For the STIC hybrid/transformer combination, the high current path when the STIC is transmitting will be from the -15 volt power supply, through the transmitter output stage, through one leg of the isolation transformer to the transformer center tap. It is important to realize that the high current return path is **through the transformer center tap and not through the STIC's GND pin.**

It is an important layout consideration to minimize the power supply distribution impedance along this path. Any resistance will result in voltage drops for the power supply input voltage, and can ultimately lower the transmitter output voltage, possibly below the minimum level required by MIL-STD-1553.

1553 BUS CONNECTIONS

The isolation transformers should be placed **as physically close as possible** to the respective TX/RX pins on the STIC and the distance from the isolation transformers to any connectors or cables leaving the board should be **as short as possible.** In addition to limiting the voltage drops in the analog signal traces when transmitting, reducing the hybrid-to-transformer and transformer-to-connector spacings serves to minimize crosstalk from other signals on the board.

The general practice in connecting the stub side of a transformer (or direct) coupled terminal to an external system connector is to make use of 78 ohm twisted-pair shielded cable. This minimizes impedance discontinuities. The decision of whether to isolate or make connections between the center tap of the isolation transformer's secondary, the stub shield, the bus shield, and/or chassis ground must be made on a system basis, as determined by an analysis of EMI/RFI and lightning considerations.

In most systems, it is specified that the 1553 terminal's input impedance must be measured at the system connector. This is

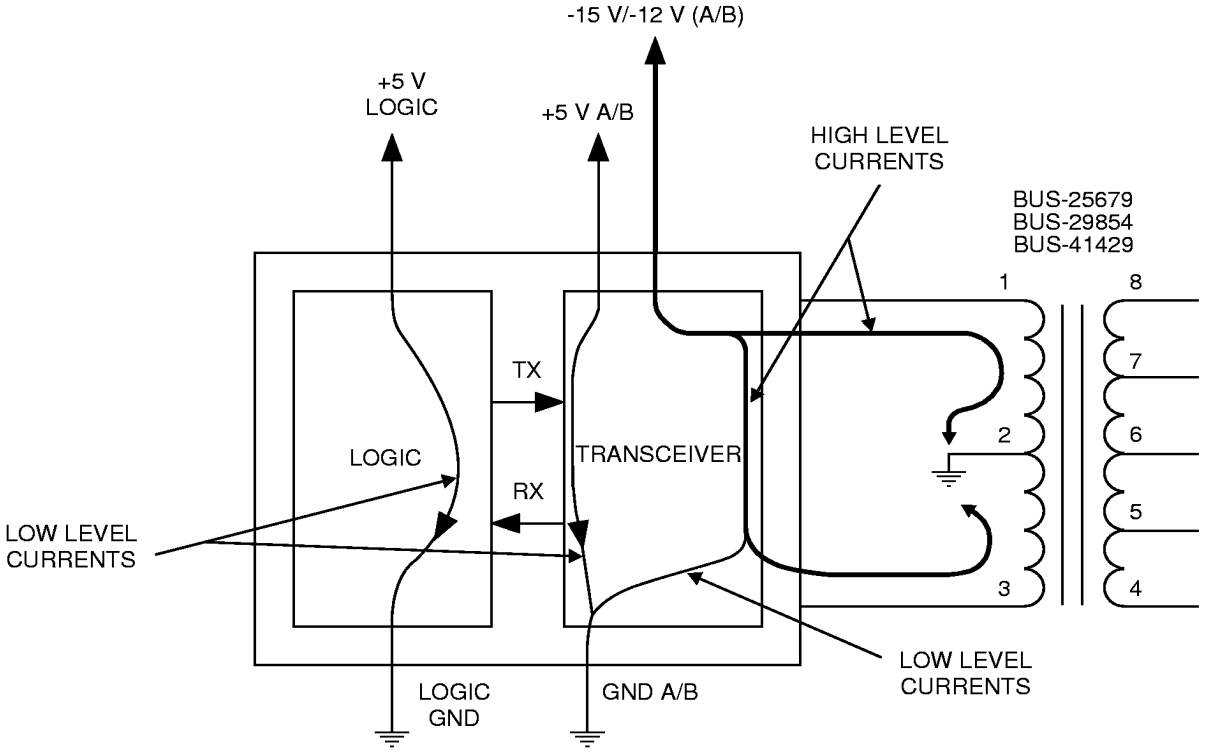


FIGURE 19. POWER/GROUND CURRENT DISTRIBUTION

despite the fact that the MIL-STD-1553B requirement is for it to be measured looking directly in from the bus side of the isolation transformer.

The effect of a relatively long stub cable will be to reduce the measured impedance. In order to keep the impedance above the required level of 1000 ohms (for transformer-coupled stubs), the length of any cable between the 1553 RT and the system connector should be minimized.

"SIMULATED BUS" (LAB BENCH) INTERCONNECTIONS

For purposes of software development and system integration, it is generally not necessary to integrate the required couplers, terminators, etc., that comprise a complete MIL-STD-1553B bus. In most instances, a simplified electrical configuration will suffice. The three connection methods illustrated in FIGURE 20 allow the STIC to be interfaced over a ©simulated bus[a] to simulation and test equipment. It is important to note that **the termination resistors indicated are necessary** in order to ensure reliable communications between the STIC and the simulation/test equipment.

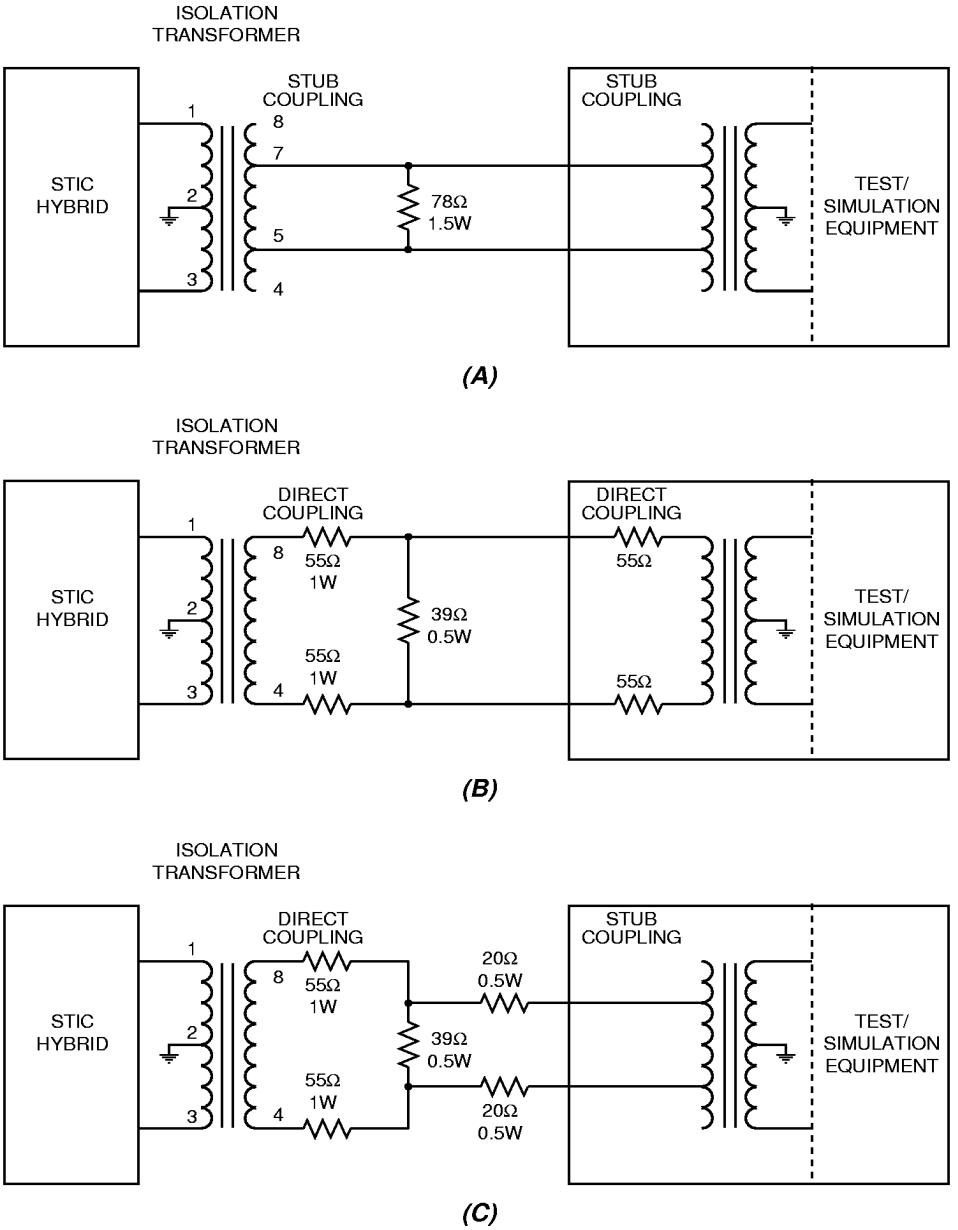


FIGURE 20. "SIMULATED BUS" (LAB BENCH) INTERCONNECTIONS
A) DIRECT COUPLED TO DIRECT COUPLED
(B) TRANSFORMER COUPLED TO TRANSFORMER COUPLED
(C) DIRECT COUPLED TO TRANSFORMER COUPLED

TABLE 5. BUS-65153 PIN DESCRIPTIONS			
POWER AND GROUND			
PIN NO	NAME	I/O	DESCRIPTION
18	GND	-	Analog and Digital Ground
35	+5 VA	I	Logic and CH. A Transceiver +5V Supply Input
70	+5 VOLTS B	I	CH.B Transceiver +5V Supply Input
36	-15 (-12) VOLTS	I	CH. A and CH. B Transceiver -15V (-12V) Supply Input

DATA BUS (16)			
PIN NO	NAME	I/O	DESCRIPTION
10	DB15 (MSB)	I/O	8/16-bit data bus. DB15 through DB00 may be configured as either a 16-bit or an 8-bit data bus. In the 8-bit mode, DB15 thru DB8 should be connected directly to DB7 thru DB0, respectively (DB15 to DB7, DB14 to DB6 , ... , DB8 to DB0). DB15-DB00 is maintained in a high-impedance state except when the BUS-65153 is performing a data write transfer. In the 8-bit mode, the upper byte is transferred first, followed by the lower byte.
11	DB14	I/O	
12	DB13	I/O	
13	DB12	I/O	
14	DB11	I/O	
15	DB10	I/O	
16	DB09	I/O	
17	DB08	I/O	
19	DB07	I/O	
20	DB06	I/O	
21	DB05	I/O	
22	DB04	I/O	
23	DB03	I/O	
24	DB02	I/O	
25	DB01	I/O	
26	DB00 (LSB)	I/O	

(TABLE 5 CONTINUES ON THE NEXT PAGE.)

TABLE 5. BUS-65153 PIN DESCRIPTIONS - CONTINUED			
ADDRESS BUS (14)			
PIN NO.	NAME	I/O	DESCRIPTION
50	A13	O	Broadcast. Latched output signal that represents the RT Address field of the present Command Word. That is, it was either a broadcast message (all ones in the RT Address Field) or a command addressed explicitly to this terminal (the address field of the command word matches the terminals's RTADD04 to RTADD0 inputs and RTAD4-0, RTADP has an odd parity sum.). It is updated after $\overline{NBGRT}$ but before $\overline{INCMD}$ goes active. A logic "1" indicates a broadcast command, a logic "0" indicates a command to the BUS-65153's RT Address. Cleared by $\overline{RESET}$. (Note 1)
52	A12	O	Transmit/Receive - Latched output signal that represents the latched T/$\overline{R}$ bit (bit 10) of the present Command Word. It is updated after $\overline{NBGRT}$ but before $\overline{INCMD}$ goes active. A logic "1" indicates a transmit command, a logic "0" indicates a receive command. Cleared by $\overline{RESET}$. (Note 1)
53	A11 (MSB)	O	A11 through A07 : Subaddress [4:0] - These outputs are the latched data from the Subaddress field of the received Command Word. They are updated after $\overline{NBGRT}$ but before $\overline{INCMD}$ goes active. They are cleared by $\overline{RESET}$. A11 corresponds to SA4 which is the MSB and A07 corresponds to SA0 which is the LSB. (Note 1)
54	A10	O	
55	A09	O	
56	A08	O	
57	A07 (LSB)	O	
58	A06	O	Command Word Transfer - Active low level output signal that is asserted when the 1553 Command Word is being transferred to the subsystem over the parallel data bus. A06 is high during all Data Word transfers. (Note 1)
59	A05 (MSB)	O	A05 through A01 (LSB):Word Count [4:0] / Current Word Count [4:0]. Multiplexed output signals which are defined as follows: these outputs are the latched data from the Word Count field of the received Command Word. They are updated after $\overline{NBGRT}$ but before $\overline{INCMD}$ goes active. They are cleared by $\overline{RESET}$. For the Command Word transfer (A06 = 0) of a nonmode code Command Word, A05-A00 will be 00000. For a mode code Command Word transfer, A05-A00 will reflect the mode code field of the Command Word. If the present command is not a mode code and $\overline{INCMD}$ is active then these lines become the output of a current word counter. That is, when $\overline{INCMD}$ goes active, these outputs go to logic "0" and are then incremented after every Data Word transfer or handshake timeout. For a mode code transfer, the single Data Word is accessed at an address location that is offset by a value of 32 above that of the location for the corresponding Command Word. When $\overline{INCMD}$ goes inactive, A05-A01 become the latched Word Count field again. A5 corresponds to WC4 which is the MSB and A1 corresponds to WC0 which is the LSB. (Note 1)
60	A04	O	
61	A03	O	
62	A02	O	
63	A01 (LSB)	O	
64	A00	O	MSB/LSB - Output signal that is used during 8-bit data transfers to indicate which byte of the present 16-bit word is being transferred. A logic "1" indicates the upper byte (MSB) and a logic "0" indicates the lower byte (LSB). The upper byte is transferred first. If a 16-bit data structure is used (DB_SEL = logic "0"), this bit will always be logic "1" (Note 1)

CLOCK, RESET, AND TRANSMITTER INHIBIT (4)			
PIN NO.	NAME	I/O	DESCRIPTION
51	CLOCK IN	I	12 or 16 MHz clock input.
43	CLOCKSEL	I	Clock Frequency Select. If high, selects 12 MHz clock input. If low, selects a 16 MHz clock input.
45	$\overline{RESET}$	I	Master Reset - Active low input signal (2 clock cycles minimum) used to reset the entire circuit.
49	$\overline{TXINH}$	I	Transmitter Inhibit. A low level on this input disables both 1553 transmitters.

Notes:
1. A13 through A0, $\overline{CS}$, and $\overline{WRT}$ will be placed in a high impedance state if $\overline{ADDR_ENA}$ is high and $\overline{DTACK}$ is inactive (high).
2. The RT Status Word inputs $\overline{ILLCMD}$, $\overline{SERVREQ}$, $\overline{SSFLAG}$, and $\overline{BUSY}$ are sampled approximately 5 ms following the mid-parity bit zero crossing of the received Command Word.

(TABLE 5 CONTINUES ON THE NEXT PAGE.)

TABLE 5. BUS-65153 PIN DESCRIPTIONS - CONTINUED			
DMA HANDSHAKE AND TRANSFER CONTROL (8)			
PIN NO.	**NAME**	**I/O**	**DESCRIPTION**
69	$\overline{\text{DT_REQ}}$	O	Data Transfer Request. Active low level output signal used to inform the subsystem that the BUS-65153 needs control of the data bus to perform a transfer. Stays low until $\overline{\text{DT_GRT}}$ is received and the transfer is completed or until a handshake failure timeout has occurred.
1	$\overline{\text{DT_GRT}}$	I	Data Transfer Grant. Active low level input signal from the subsystem that, in response to a Data Transfer Request, passes control of the parallel data bus to the BUS-65153.
2	$\overline{\text{DT_ACK}}$	O	Data Transfer Acknowledge - Active low level output signal used to inform the subsystem that the BUS-65153 has received $\overline{\text{DT_GRT}}$ in response to $\overline{\text{DT_REQ}}$. $\overline{\text{DT_ACK}}$ remains active until the transfer is complete.
3	$\overline{\text{CS}}$	O	Chip Select - Active low level output pulse present in the middle of every data transfer cycle. When the BUS-65153 is writing data to the subsystem, this signal occurs when the data is valid and should be used to latch the data (recommend using rising edge). When the BUS-65153 is reading data from the subsystem, this signal is used to inform the subsystem when to drive the data bus. (Note 1)
4	$\overline{\text{WRT}}$	O	Read/Write - Output signal that controls the direction of the data transfers. The direction is normally outward (write = logic “0”) and only turns inward (read = logic “1”) when the first Data Word is needed from the subsystem. The output will return low (write) after the transmission of the last data word on the 1553 bus. (Note 1)
6	$\overline{\text{HS_FAIL}}$	O	Handshake Failure - Active low level output used to flag the subsystem that $\overline{\text{DT_GRT}}$ was not received in response to $\overline{\text{DT_REQ}}$ in time to perform a data transfer. Latched low and cleared by the next $\overline{\text{NBGRT}}$ or $\overline{\text{RESET}}$.
7	$\overline{\text{ADDR_ENA}}$	I	Address Enable. Active low level input signal used to control the operation of $\overline{\text{WRT}}$, $\overline{\text{CS}}$, and address bus A13 through A00. If a logic “0” is applied, the above signals are always active. If a logic “1” is applied, these signals are kept in their high impedance state except for when a data transfer is being performed ($\overline{\text{DT_ACK}}$ = logic “0”)
8	DB_SEL	I	Data Bus Select - Input signal used to select the data bus structure (8- or 16-bit width) Logic “0” selects 16-bit data bus Logic “1” selects 8-bit data bus Note: For 8-bit data bus operation, D15 to D08 should be connected directly to D07 to D00, respectively.

INTERFACE TO 1553 PULSE TRANSFORMERS (4)			
PIN NO.	**NAME**	**I/O**	**DESCRIPTION**
5	RX/TXB	I/O	Channel B Non-Inverted 1553 Serial Data.
9	$\overline{\text{RX/TXB}}$	I/O	Channel B Inverted 1553 Serial Data
40	RX/TXA	I/O	Channel A Non-Inverted 1553 Serial Data
44	$\overline{\text{TX/TXA}}$	I/O	Channel A Inverted 1553 Serial Data

RT ADDRESS (8)			
PIN NO.	**NAME**	**I/O**	**DESCRIPTION**
27	$\overline{\text{RT_ADD_ERR}}$	O	Remote Terminal Address Parity Error Output Signal that reflects the parity combination of the RT_AD_[4:0] inputs and RT_AD_P input. High level indicates odd parity, low level indicates even parity. Note, if $\overline{\text{RT_ADD_ERR}}$ is low, then the BUS-65153 will not recognize any valid Command Word directed to its own RT address.
28	RT_ADD_LAT	I	Remote Terminal Address Latch. When low, the internal RDAD4-0 and RTADP register tracks whatever is applied to the respective input pins. When RT_ADD_LAT is high, the information that was on RTAD4-0 and RTADP the last time that RT_ADD_LAT was low is latched internally. The internal RTAD4-0 and RTADP are cleared to logic 0 when $\overline{\text{RESET}}$ is low.
29	RT_ADD_P	I	Remote Terminal Address [4:0] - Input signal of the address parity bit. The combination of RT_AD_[0:4], and RT_AD_P must comprise an odd parity sum in order to enable recognition of the terminal's address.
30	RTADD00 (LSB)	I	Remote Terminal Address inputs.
31	RTADD01	I	
31	RTADD02	I	
33	RTADD03	I	
34	RTADD04 (MSB)	I	

Notes:
1. A13 through A0, $\overline{\text{CS}}$, and $\overline{\text{WRT}}$ will be placed in a high impedance state if $\overline{\text{ADDR_ENA}}$ is high and $\overline{\text{DTACK}}$ is inactive (high).
2. The RT Status Word inputs $\overline{\text{ILLCMD}}$, $\overline{\text{SERVREQ}}$, $\overline{\text{SSFLAG}}$, and $\overline{\text{BUSY}}$ are sampled approximately 5 ms following the mid-parity bit zero crossing of the received Command Word.

(TABLE 5 CONTINUES ON THE NEXT PAGE.)

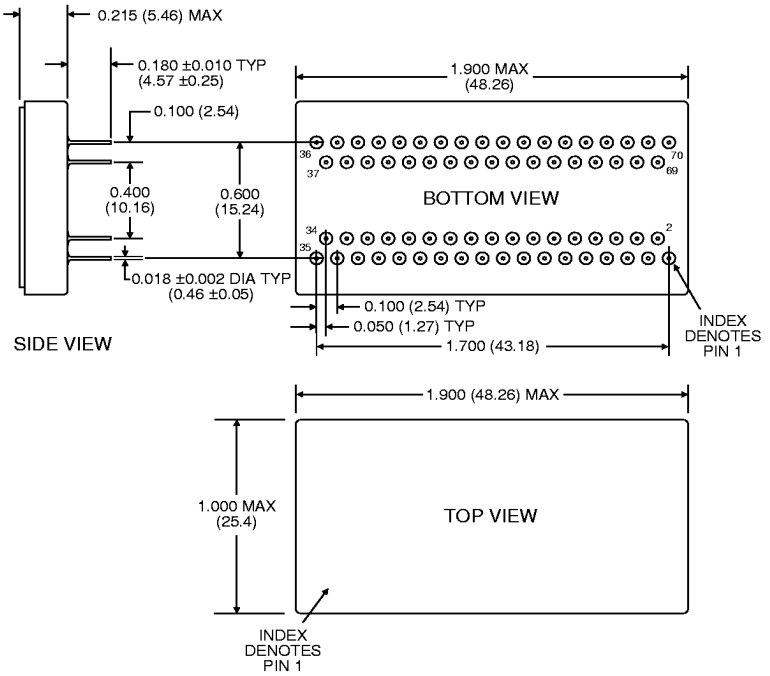
TABLE 5. BUS-65153 PIN DESCRIPTIONS - CONTINUED			
RT STATUS WORD INPUTS (4)			
PIN NO.	NAME	I/O	DESCRIPTION
65	$\overline{\text{ILLCMD}}$	O	Illegal Command Input. Active low Input used to illegalize any command. If low when sampled, the Message Error bit (bit 10) in the Status Word will be set. The response to an illegal transmit command will be a Status Word only. The only effect of illegalizing a receive command will to inhibit $\overline{\text{GBR}}$. An illegalized mode code will not perform the actual mode functions. (Note 2)
66	$\overline{\text{SERVREQ}}$	I	Service Request - Input signal used to control the Service Request bit (bit 8) in the Status Word. If low when sampled, the Service Request bit will be set. If high, it will be logic"0". (Note 2)
67	$\overline{\text{SSFLAG}}$	I	Subsystem Flag - Input signal used to control the Subsystem Flag bit (bit 2) in the Status Word. If low when sampled, the Subsystem Flag bit will be set. If high, the Subsystem Flag bit will be logic "0". (Note 2)
68	$\overline{\text{BUSY}}$	I	Input signal used to control the Busy bit (bit 3) in the Status Word. If low when sampled, the Busy bit will be set. If high, it will be cleared. Note, if the Busy bit is set and the command was a transmit command, only the Status Word would be transmitted. Has no effect on data received following a receive command. (Note 2)

MESSAGE TIMING OUTPUT SIGNALS (5)			
PIN NO.	NAME	I/O	DESCRIPTION
37	$\overline{\text{GBR}}$	O	Good Block Received - Low level output pulse (2 clock cycles wide) that is used to flag the subsystem that a valid, legal, nonmode receive command with the correct number of data words has been received without a message error and successfully transferred to the subsystem
38	$\overline{\text{RTFAIL}}$	O	Remote Terminal Failure - Latched low level output that goes low if a loopback failure (or transmitter shutdown timeout) has occurred during a transmission cycle. A loopback failure occurs under any of the following conditions: (1) the first transmitted word (Status Word) contains an incorrect RT address field, (2) the received version of any transmitted word is either invalid or contains the incorrect sync type, (3) the received 16-bit data pattern for the last transmitted word does not match that of the transmitted version of the word and/or (4) A transmitter timeout (668 ms) has occurred. Reset by the start of the next transmission cycle (Status Word) or a low level on the $\overline{\text{RESET}}$ input. An $\overline{\text{RTFAIL}}$ condition (low level output on $\overline{\text{RTFAIL}}$) will cause the Terminal Flag bit in the RT Status Register to be set. When this occurs, the RT Flag Status Word bit will be set in response to the next valid nonbroadcast command.
39	$\overline{\text{NBGRT}}$	O	New Bus Grant - Low level output pulse (2 clock cycles wide), that is used to indicate the start of a new protocol sequence in response to the Command Word just received from the 1553 bus.
41	$\overline{\text{INCMD}}$	O	In Command - Active low level output signal used to inform the subsystem that the BUS-65153 is presently servicing a command that came in on the 1553 bus.
42	$\overline{\text{ME}}$	O	Message Error - Active low level output signal used to flag the subsystem that there was a message error on the 1553 bus communication (word, gap, or word count error). This output goes low upon detecting the error and is reset at the start of the next $\overline{\text{NBGRT}}$ pulse or master reset. If this output goes low, all further command servicing is aborted.

FACTORY TEST INPUTS (3)			
PIN NO.	NAME	I/O	DESCRIPTION
46	FACTORY TEST POINT	I	Connect to + 5 volts.
47	FACTORY TEST POINT	I	Connect to + 5 volts.
48	FACTORY TEST POINT	I	Connect to + 5 volts.

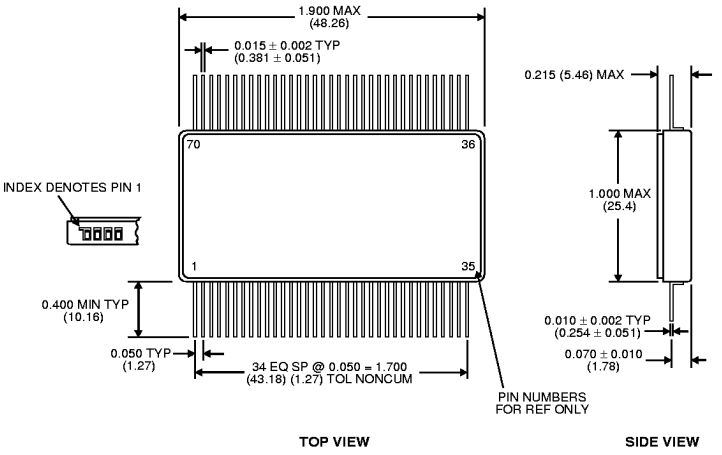
Notes:
1. A13 through A0, $\overline{\text{CS}}$, and $\overline{\text{WRT}}$ will be placed in a high impedance state if $\overline{\text{ADDR_ENA}}$ is high and $\overline{\text{DTACK}}$ is inactive (high).
2. The RT Status Word inputs $\overline{\text{ILLCMD}}$, $\overline{\text{SERVREQ}}$, $\overline{\text{SSFLAG}}$, and $\overline{\text{BUSY}}$ are sampled approximately 5 ms following the mid-parity bit zero crossing of the received Command Word.

TABLE 6. BUS-65153/63 PIN LISTING			
PIN	NAME	PIN	NAME
1	$\overline{\text{DT_GRT}}$	36	-15 (-12)VOLTS
2	$\overline{\text{DT_ACK}}$	37	$\overline{\text{GBR}}$
3	$\overline{\text{CS}}$	38	$\overline{\text{RTFAIL}}$
4	$\overline{\text{WRT}}$	39	$\overline{\text{NBGRT}}$
5	RX/TX B	40	RX/TX A
6	$\overline{\text{HS_FAIL}}$	41	$\overline{\text{INCMD}}$
7	$\overline{\text{ADDR_ENA}}$	42	$\overline{\text{ME}}$
8	DB_SEL	43	CLOCKSEL
9	$\overline{\text{RX/TX B}}$	44	$\overline{\text{RX/TX A}}$
10	DB!5 (MSB)	45	$\overline{\text{RESET}}$
11	DB14	46	FACTORY TEST POINT
12	DB13	47	FACTORY TEST POINT
13	DB12	48	FACTORY TEST POINT
14	DB11	49	$\overline{\text{TXINH}}$
15	DB10	50	AT3
16	DB09	51	CLOCK IN
17	DB08	52	AT2
18	GND	53	AT11 (MSB)
19	DB07	54	A10
20	DB06	55	A09
21	DB05	56	A08
22	DB04	57	A07 (LSB)
23	DB03	58	A06
24	DB02	59	A05 (MSB)
25	DB01	60	A04
26	DB00 (LSB)	61	A03
27	$\overline{\text{RT_ADD_ERR}}$	62	A02
28	RT_ADD_LAT	63	A01 (LSB)
29	RT_ADD_P	64	A00
30	RTADD00 (LSB)	65	$\overline{\text{ILLCMD}}$
31	RTADD01	66	$\overline{\text{SERVREQ}}$
32	RTADD02	67	$\overline{\text{SSFLAG}}$
33	RTADD03	68	$\overline{\text{BUSY}}$
34	RTADD04 (MSB)	69	$\overline{\text{DT_REQ}}$
35	+ 5 VA	70	+ 5 VOLTS B



NOTES:
1. DIMENSIONS ARE IN INCHES (MILLIMETERS).
2. PACKAGE MATERIAL: ALUMINA (AL_2O_3).
3. LEAD MATERIAL: KOVAR, PLATED BY 150µ MINIMUM NICKEL, PLATED BY 50µ MINIMUM GOLD.

FIGURE 21. BUS-65153/54 DIP MECHANICAL OUTLINE



NOTES:
1. DIMENSIONS ARE IN INCHES (MILLIMETERS).
2. PACKAGE MATERIAL: ALUMINA (AL_2O_3).
3. LEAD MATERIAL: KOVAR, PLATED BY 150µ MINIMUM NICKEL, PLATED BY 50µ MINIMUM GOLD.

FIGURE 22. BUS-65163/64 FLAT PACK MECHANICAL OUTLINE

ORDERING INFORMATION

BUS-651XX-XX0X

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- K = One Lot Date Code
- W = One Lot Date Code and PreCap Source
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, PreCap Source and 100% Pull Test
- Blank = None of the Above

Process Requirements:
- 0 = Standard DDC Processing, no Burn-In (See table below.)
- 1 = MIL-PRF-38534 Compliant
- 2 = B*
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See table below.)

Temperature Grade/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

Power Supply and Packaging
- 53 = +5 V/-15 V DIP
- 54 = +5 V/-12 V DIP
- 63 = +5 V/-15 V Flat Pack
- 64 = +5 V/-12 V Flat Pack

*Standard DDC Processing with burn-in and full temperature test — see table below.

Also available as DESC P/N 5962-92162-01HXC.

Data Bus Transformers:

For BUS-65153/63 use BUS-25679, B-2203, LPB-5002, LPB-5009, or M21038/27-02.

For BUS-65154/64 use BUS-29854, B-2204, LPB-5001, LPB-5008, or M21038/27-03.

STANDARD DDC PROCESSING		
TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	A
BURN-IN	1015, Table 1	—