UA1000 SERIES

Gate Arrays

Features

- Silicon-gate 3-micro (drawn) single metal HCMOS technology
- Speeds higher than 74 TTL-3.0ns through 2-input NAND gate and interconnection, $T_A = 25°C$, fanout = 2, $V_{DD} = 5V$
- Optimal block structure of 2n and 2p transistors
- Low power consumption
- Configurable output drive up to 24 mA under worst case commercial conditions
- All non-power pads configurable as input, output or bidirectional I/O
- All inputs and outputs protected from over-voltage and latch up
- Replacement for all 7400 and 4000 SSI/MSI
- Fully supported by UMC's CAD system
- Stand-by current to 1μA

Product Outline

Device Number	Gate Complexity	I/O Buffer	V_{DD} Pads	V_{SS} Pads	Max. Pads	Gate Speed (ns)[1]	
						Typ.	Max[2]
UA1020	200	28	2	2	32	3.0	4.0

Notes: 1. 2-input NAND gate, fanout = 2, and typical interconnection.
2. $T_A = 0$ to $70°C$, $V_{DD} = 5V \pm 5\%$.
3. Including 2 pads without I/O buffer.