UA1300 SERIES

Gate Arrays

Features

- Silicon-gate 2.0 micron (drawn) double metal HCMOS technology.
- Speeds higher than 74/TTL-1.7ns through 2-input NAND gate and interconnection, $T_A = 25°C$, fanout = 2, $V_{DD} = 5V$
- Optimal block structure of 2N and 2 P transistors
- Complexities ranging from 1300 to 3060 gate counts
- Pin counts ranging up to 96
- Fully supported by DAISY system
- Extensive macrocell and macrofunction libraries
- All non-power pads configurable as inputs, outputs, or bidirectional I/O
- Configurable output drive up to 12 mA under worst-case commercial conditions
- All inputs and outputs protected from over-voltage and latch up

Product Outline

Device Number	Gate Complexity	I/O Buffer	V_{DD} Pads	V_{SS} Pads	Max. Pads	Gate Speed (ns)[1]	
						Typ.	Max[2]
UA1313	1320	50	2	2	54	1.7	2.5
UA1318	1820	66	2	2	70		
UA1322	2240	80	2	2	84		
UA1330	3060	92	2	2	96		

Notes: 1. 2-input NAND gate, fanout = 2, and typical interconnection.
2. $T_A = 0$ to $70°C$, $V_{DD} = 5V \pm 5\%$.
3. Including 2 pads without I/O buffer.