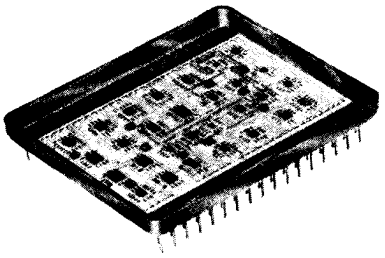
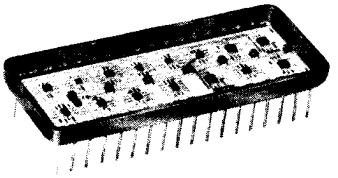
BUS-66106® AND BUS-66111

ILC DATA DEVICE CORPORATION

MIL-STD-1553 BUS CONTROLLER PROTOCOL HYBRIDS



BUS-66106



BUS-66111

DESCRIPTION

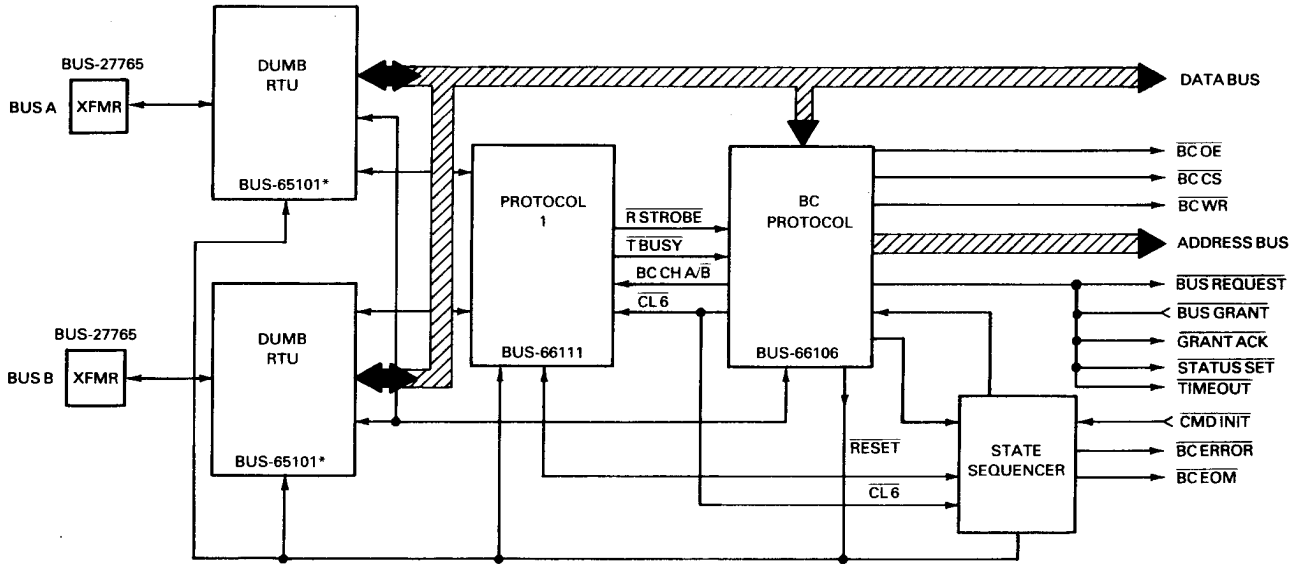
BUS-66106 and BUS-66111 comprise a pair of hybrids which generate the complete protocol, timing and control function required by a Bus Controller (BC) in full compliance with MIL-STD-1553 or MacAir A5690. When used with a Dumb RTU and State Sequencer, as shown in Figure 1, these BC Protocol hybrids provide a complete Bus Controller function which supports all message formats. A significant feature is that the RTU status word response is validated by the BC Protocol hybrids with no subsystem intervention.

BUS-66106 and BUS-66111 BC Protocol hybrids provide a simple and flexible interface to the subsystem. Message transfers are accomplished by means of a DMA type handshaking. Output flags are provided to the subsystem at the end of each message, when a BC error has occurred, a status word bit has been set, and a Terminal Fail-Safe Timeout has occurred. The BC Protocol hybrids provide control lines for implementation of online wraparound built-in test of the Bus Controller.

The BUS-66106 is packaged in a 68 pin 1.6 x 1.9 inch hybrid, and the BUS-66111 is packaged in a 36 pin DDIP 0.8 x 1.9 inch hybrid. A complete dual redundant Bus Controller and Remote Terminal Unit, using these hybrids, is available from DDC on a 6.3 x 9.2 inch VME Eurocard as part number BUS-65500.

FEATURES

- *GENERATES PROTOCOL, TIMING AND CONTROL FOR MIL-STD-1553 OR MACAIR A5690 BUS CONTROLLER*
- *SUPPORTS ALL MESSAGE FORMATS*
- *VALIDATES RTU STATUS RESPONSE AND DATA WORDS*
- *TRANSFERS MESSAGES WITH DMA TYPE HANDSHAKING*
- *PROVIDES FLAGS FOR:*
  END OF MESSAGE
  ERROR
  STATUS BIT SET
  TIMEOUT
- *IMPLEMENTS WRAPAROUND BUILT-IN TEST*



*FOR MACAIR A5690, USE BUS-65201

FIGURE 1. BLOCK DIAGRAM – BUS CONTROLLER HYBRID SET

SPECIFICATIONS – BUS-66106
Values at nominal supply voltage.

PARAMETER	UNITS	VALUE
Logic		
I_{IH}, I_{IL}, I_{OH}, I_{OL}		See Pin Function and Loading Table.
V_{OL}	V	0.4 max.
V_{OH}	V	2.5 min.
V_{IL}	V	0.7 max.
V_{IH}	V	2.0 min.
Power Supplies		
Voltage	V	5.0±10%
Current Drain	mA	800 max.
Temperature Range (Case)		
Operating	°C	−55 to +125
Storage	°C	−65 to +150
Physical Characteristics		
Size	in. (mm)	1.85 x 1.59 x 0.21 (46.9 x 40.38 x 5.33)
Weight	oz. (gm)	2.0 (56)

SPECIFICATIONS – BUS-66111
Values at nominal supply voltage.

PARAMETER	UNITS	VALUE
Logic		
I_{IH}, I_{IL}, I_{OH}, I_{OL}		See Pin Function and Loading Table.
V_{OL}	V	0.4 max.
V_{OH}	V	2.5 min.
V_{IL}	V	0.7 max.
V_{IH}	V	2.0 min.
Power Supplies		
Voltage	V	5.0±10%
Current Drain	mA	200 max.
Temperature Range (Case)		
Operating	°C	−55 to +125
Storage	°C	−65 to +150
Physical Characteristics		
Size	in. (mm)	1.895 x 0.775 x 0.21 (48.1 x 19.7 x 5.3)
Weight	oz. (gm)	1.0 (28)

GENERAL

BUS-66106 and BUS-66111 are Bus Controller Protocol hybrids designed for use in MIL-STD-1553 Bus Controllers. BUS-66111 functions as a multiplexer for the handshaking signals required by the Dumb RTUs interfacing to the dual serial MUX data bus. It generates control signals for the BUS-66106, as well as providing the fault processing function.

BUS-66106 provides the protocol timing and control for a MIL-STD-1553 Bus Controller. It supports all 1553 message formats while validating the RTU status word response without help from the subsystem. Its subsystem interface includes a 16 bit data highway, a 6 bit address bus and control lines for a DMA type handshake during message transfer.

A typical implementation of the Bus Controller function would include Dumb RTU BUS-65101, BC Protocol BUS-66106 and BUS-66111, a Programmable Logic Sequencer and possibly a dual port memory for interim message storage. DDC has packaged a complete dual redundant Bus Controller and Remote Terminal Unit on a 6.3 x 9.2 inch VME Eurocard, which is supplied as part number BUS-65500.

BUS-66106 OPERATION

The BUS-66106 contains three registers, a 16 bit Data Buffer, a Status Word Comparator, two counters and Timing Logic. (See Block Diagram, Figure 3.)

The 16 bit Tri-State Data Bus is buffered to prevent loading of the bus. The incoming data can be stored in one of the three registers, depending on the four mode signals originating in the State Sequencer. The three registers are:

- Command 1 Register
- Command 2 Register
- Control Word Register

BUS CONTROL ACTIVE FLAG

Upon receipt of the $\overline{\text{CMND INIT}}$ pulse (500ns minimum width) the Bus Controller activates the Bus Control Active output and starts the transmit cycle. The Bus Controller remains active until one of the following occurs, making the Bus Control Active Flag go high within one microsecond:

(1) Bus cycle Enable Input is taken low.

(2) Transmission by the Bus Controller is complete (Broadcast Mode).

(3) Transmission by the Bus controller is complete, a no response-time has occurred and an interrupt has been generated.

(4) During an RT to RT Transfer, the transmission by the Bus Controller is complete, the transmission by the first RT is complete, a no-response time-out has occurred and an interrupt has been generated.

(5) The complete transmit-receive cycle is complete and any required interrupts have been generated.

(6) A Bus Controller failure has been detected and the Bus Controller Error Flag has been set.

Upon receipt of the $\overline{\text{START}}$ signal from the sequencer, with BUS CYCLE ENABLE input HIGH, a Data Transfer from the Subsystem is requested by a $\overline{\text{BUS REQUEST}}$ output. When the $\overline{\text{B GRANT}}$ signal is received from the Subsystem, the first Data Word is read out of the Subsystem's memory and stored in the Control Word Register. The Control Word Register outputs are analyzed to detect what type of transfer is required, and then another $\overline{\text{START}}$ signal is received from the Sequencer. This causes the next location of the Subsystem's memory, which contains the Command Word, to be read. The Command Word is then latched in both Command 1 Register and in the external Encoder Register. Subsequently, the encoder is enabled and the Command Word is transmitted via the data bus. After each word transfer is completed, a COMPLETE output is generated to the Sequencer.

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CONTROL WORD FORMAT

The format of the Control Word initiated by the Subsystem must be as follows:

BITS	FUNCTION
0	RT to RT Transfer
1	Broadcast Transfer
2	Mode Code Transfer
3-6	Not Used
7	Data Bus Channel Selection CHA/B
8-15	Not Used

To select one of the above transfers, the appropriate bit should be set to a high level. In the case of Bit 7, the Channel Selection, a high level will select BUS A and a low level will select BUS B.

If an RT to RT transfer is required, then the second Command Word is read out of the memory, after the first Command Word, and latched in the Command 2 Register as well as in the external Encoder's Register, prior to transmission.

Depending on the Command Word involved, data words are either read out of memory and latched by the external Encoder Register ready for transmission, or enabled by the external Decoder Register and written into memory after reception.

SUB-SYSTEM BUFFER CONTENTS

The Command Words and Data Words should be stored in the Sub-System Data Buffer in the same format as they are to appear on the Multiplex Data Bus.

The following data format for the Subsystem data buffer is implemented by the BUS-66106.

ADDRESS	DATA BUFFER CONTENTS	CONTROL CODE (3 LSB's)
(1)	Receive Command	000
000000	Control Word	
000001	Receive Command	
000010	Data Word 1	
000011	Data Word 2	
.	.	
.	.	
.	.	
.	Data Last Word	
.	Data Last Word (Wrapped)	
.	Status Received (If Any)	
(2)	Transmit Command	000
000000	Control Word	
000001	Transmit Command	
000010	Transmit Command (Wrapped)	
000011	Status Received	
000100	Data Word 1 Received	
000101	Data Word 2 Received	
.	.	
.	.	
.	.	
.	.	
.	Data Last Word Received	
(3)	RT To RT Command	001
000000	Control Word	
000001	Receive Command	
000010	Transmit Command	
000011	Transmit Command (Wrapped)	
000100	Status Word 1 (From Trans.) Received	
000101	Data Word 1 Received	
000110	Data Word 2 Received	
.	.	
.	.	
.	.	
.	Data Last Word Received	
.	Status 2 (From Rec.) Received	
(4)	Mode Code With Data (Rec.) Command	100
000000	Control Word	
000001	Mode Command	
000010	Data Word	
000011	Data Word (Wrapped)	
000100	Status Received (If Any)	
(5)	Mode Code With Data (Trans.) Command	100
000000	Control Word	
000001	Mode Command	
000010	Mode Command (Wrapped)	
000011	Status Received	
000100	Data Word Received	
(6)	Mode Code With No Data	100
000000	Control Word	
000001	Mode Command	
000010	Mode Command (Wrapped)	
000011	Status Received	
(7)	Broadcast Mode	010
000000	Control Word	
000001	Receive Command	
000010	Data Word 1	
000011	Data Word 2	
.	.	
.	.	
.	.	
.	Data Last Word	
.	Data Last Word (Wrapped)	

When a reply is expected from the Remote Terminal, the Timeout Counter is enabled and if no reply is received within 15μs, the $\overline{\text{BC TIMEOUT}}$ flag is set.

The first word received from the Remote Terminal is always a Status Word. When this word is received within 15μs, its address field is compared with the address field in the respective Command Word Register. It is also checked for any bits set HIGH. A $\overline{\text{STAT SET}}$ flag is set LOW if any bit was set in the Status Word or if the RT address field did not match.

INTERRUPT FLAGS

The BUS-66106 Hybrid, in conjunction with the Protocol Sequencer, provides the following flags:

(1) BC TIME OUT
This Flag will be set low if no response was obtained from a Remote Terminal within 15 microseconds (this interrupt does not occur in the case of a Broadcast Message) or an Invalid Status or Data Word was received, or if there was a word count error.

(2) STATUS SET
This Flag will be set low if the Status Word received had a wrong address or if one of the Subsystem Flags is set.

(3) BC ERROR
This Flag will be set low if there was an error during the BC operation.
Additionally, the BUS-66111 generates a BCU Fail Flag, which will be set high if an error occurred during the operation of the Dumb RTU Hybrid.

(4) BC EOM
This Flag will be set low when the message has been processed by the BUS-66106.

(5) BCU FAIL
This BUS-66111 output Flag indicates a fault condition occurred during normal BCU operation.

SELF-TESTING CAPABILITY

The BUS-66106 implements a Long Loop Test wherein the last word transmitted by the Bus Controller of every message is received back (wrapped) and stored in the Data Buffer in the next location following the last word transmitted.

The Subsystem can compare the wrapped word with the last transmitted word to check the operational status of the receive and transmit circuitry.

BUS-66111 OPERATION

A $\overline{\text{R STROBE}}$ output is generated 1μs after the reception of a RCVR BUSY signal by the BUS-66111 from one of the Dumb RTUs interfacing with the two data buses. This pulse is only generated if the FAIL-SAFE FLAG inputs are active LOW.

The $\overline{\text{R STROBE}}$ pulse is used to sample the error condition, initiate the data transfer and simultaneously step the protocol sequencer device. $\overline{\text{R STROBE}}$ is generated for every RCVR BUSY input.

After the internal multiplexer is selected by the BC CH $\overline{\text{A}}$/B input, the following signals from one of the Dumb RTUs are selected:

- $\overline{\text{VALID WORD}}$
- FAIL-SAFE FLAG
- REC SYNC TYPE
- XMIT BUSY
- FAULT

The 6 Bit Address Counter is incremented for every word read out or stored into the subsystem's memory. This counter also checks for the correct number of words transmitted. The BCL WORD flag is set when the number of words transmitted or received is the same as that indicated by the Word Count field in the Command Word Register.

All the DMA handshake signals are generated by the general timing logic. The timing for the subsystem's DMA handshake signals is shown on Figures 6 and 7.

The RCVR BUSY signal is sampled periodically to generate a NO DT (IDLE/$\overline{\text{ACTIVE}}$) signal. The XMIT BUSY signal is used internally to inhibit the generation of $\overline{\text{R STROBE}}$. In addition, 4$\mu$s after the falling edge of the last XMIT BUSY signal, a $\overline{\text{R INH}}$ internal signal is generated which samples the fault signal resulting from the Wraparound Test. This $\overline{\text{R INH}}$ signal is also used to sample the FAULT signal resulting from the operation of the system as a whole. If a fault is detected, then the BCU FAIL signal will be activated. This output can be used as an interrupt to flag a system error, in which case $\overline{\text{RESET}}$ can be used as an interrupt acknowledge.

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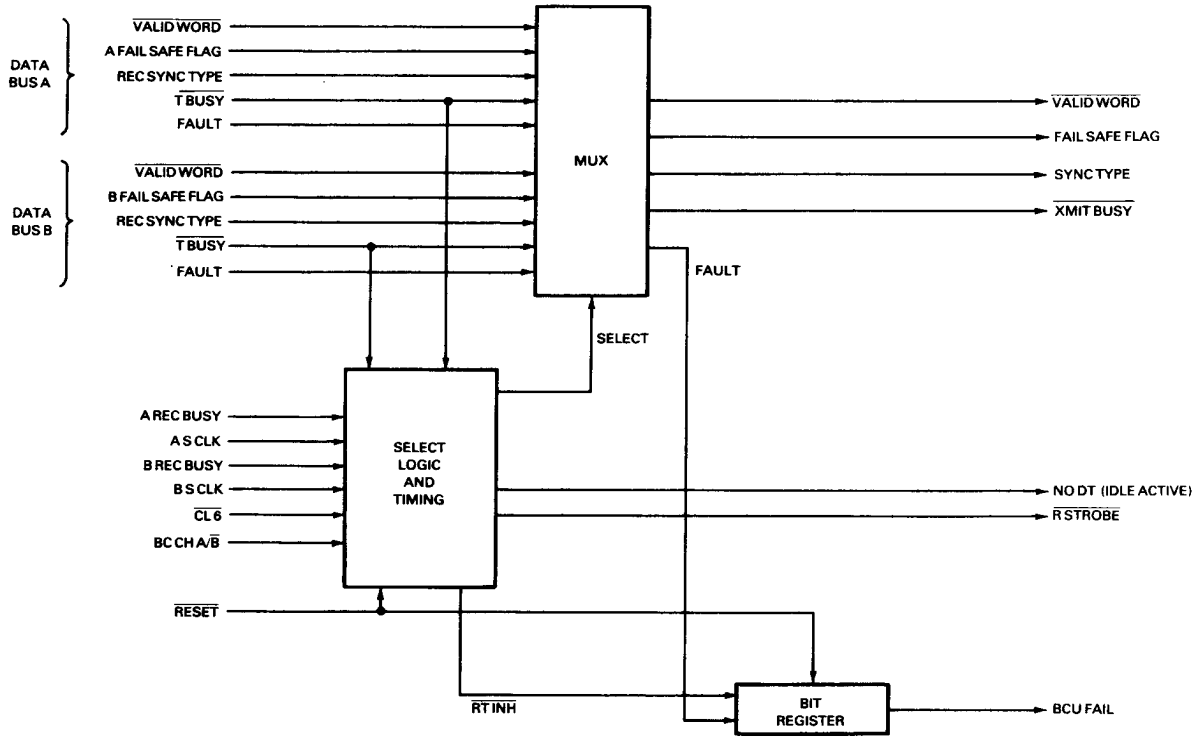

FIGURE 2. BUS-66111 PROTOCOL HYBRID BLOCK DIAGRAM

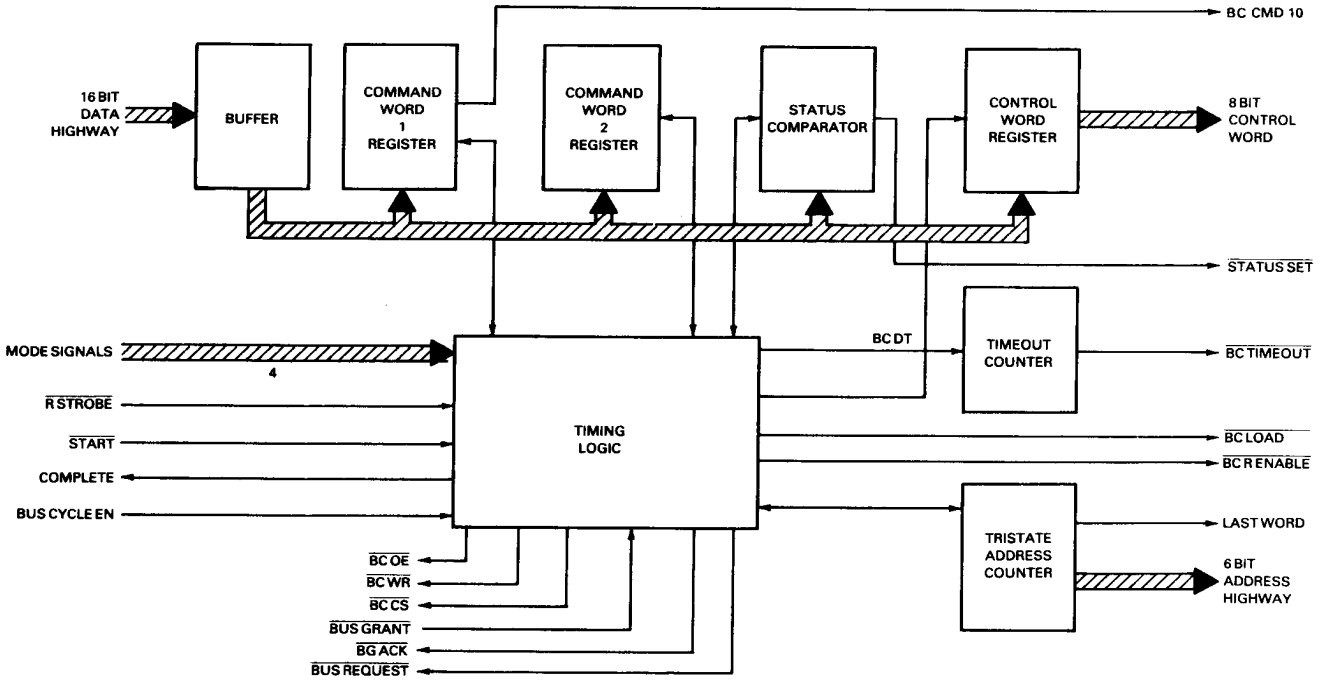

FIGURE 3. BUS-66106 BC PROTOCOL BLOCK DIAGRAM

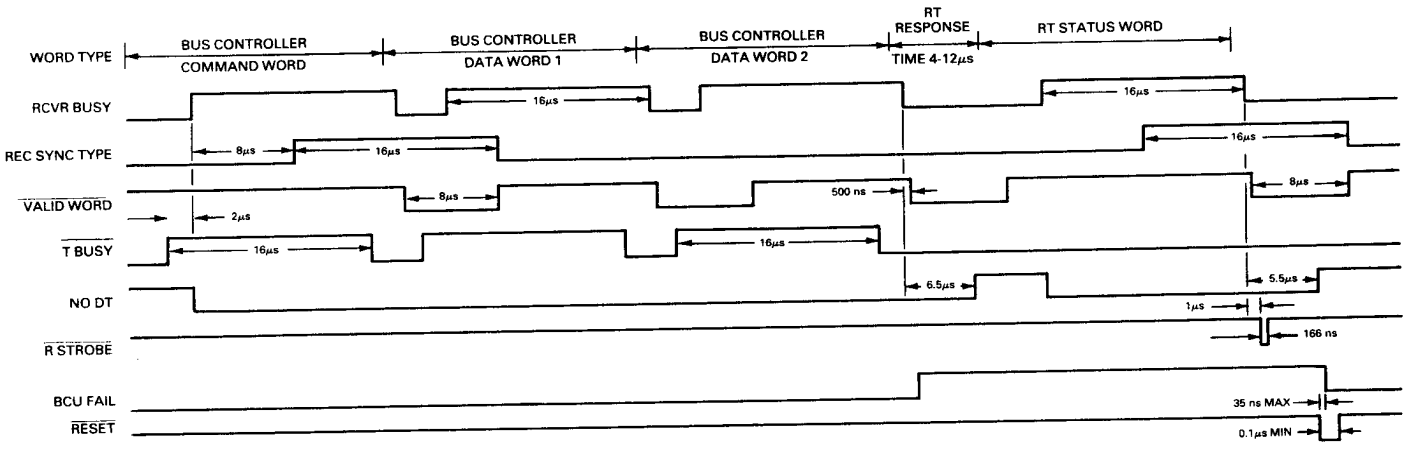

FIGURE 4. BUS-66111 TRANSMITTER MODE TIMING (2 DATA WORDS)

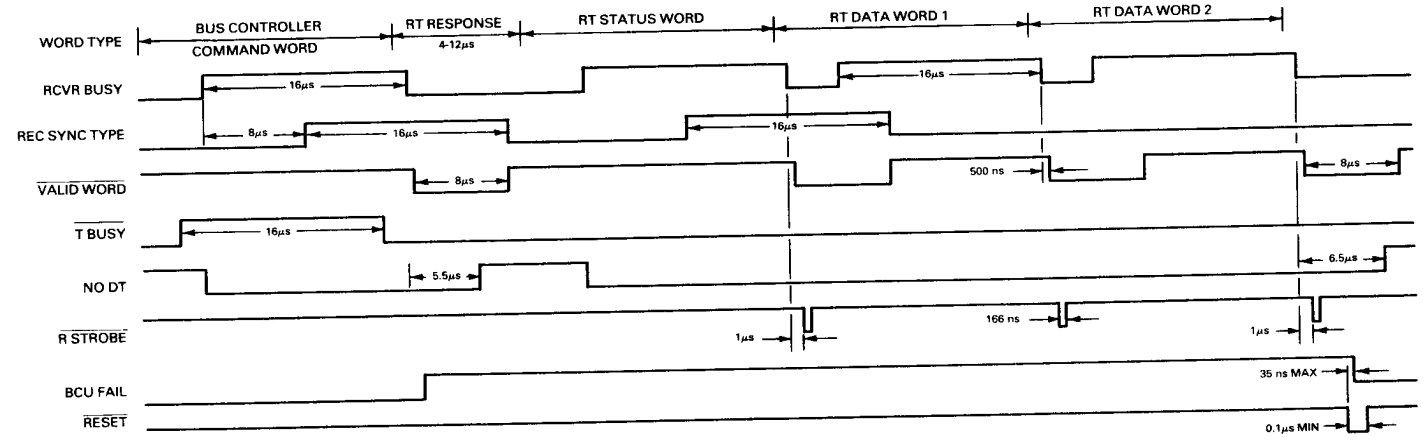

FIGURE 5. BUS-66111 RECEIVER MODE TIMING (2 DATA WORDS)

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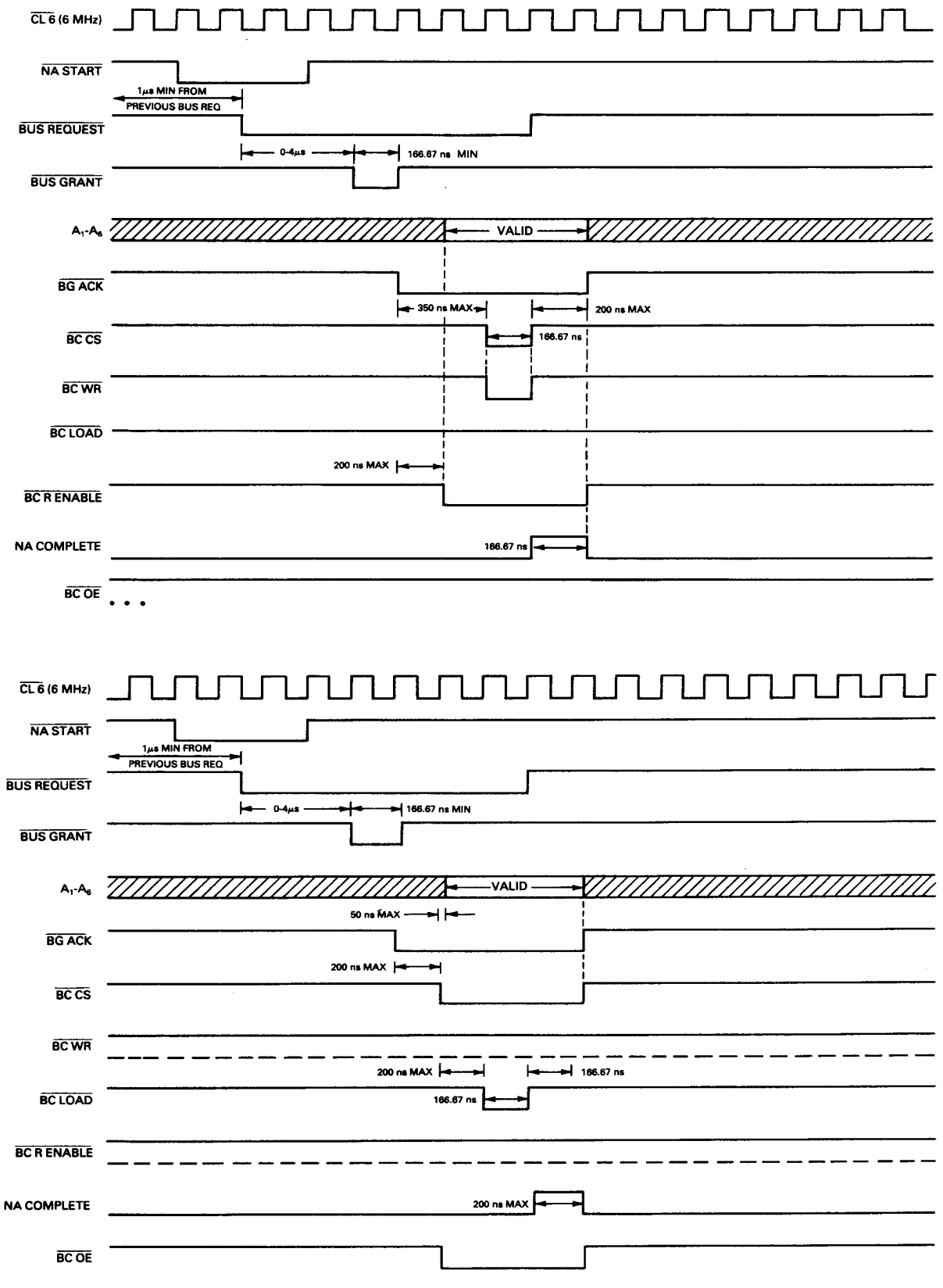

FIGURE 7. SUBSYSTEM MEMORY WRITING CYCLE

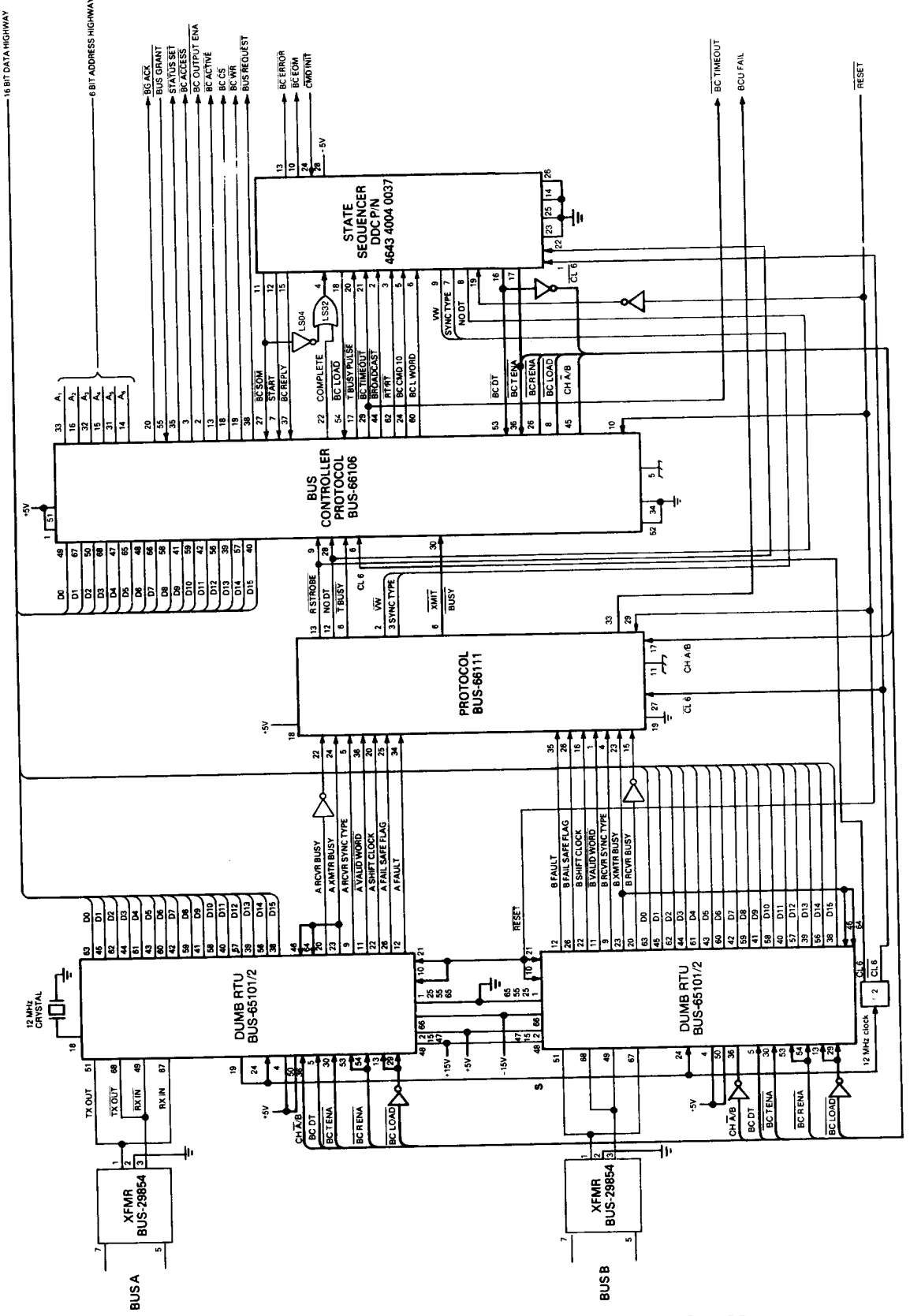

FIGURE 8. BUS CONTROLLER INTERCONNECT DIAGRAM

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BUS-66111 PIN FUNCTION AND LOADING TABLE

PIN NO.	NAME	I_{IH} (μA)	I_{IL} (mA)	I_{OH} (mA)	I_{OL} (mA)	DESCRIPTION
1	$\overline{\text{B VALID WORD}}$	20	−0.4			A LOW on this input indicates receipt of a valid word on Bus B.
2	$\overline{\text{VALID WORD}}$			−0.4	4.0	A LOW on this output indicates receipt of a valid word by the BCU.
3	SYNC TYPE			−0.4	4.0	A HIGH on this output indicates receipt of a Command or Status Word. A LOW indicates receipt of a Data Word.
4	B RCVR SYNC TYPE	20	−0.4			A HIGH on this input indicates receipt of a Command or Status word on Bus B. A LOW indicates receipt of a Data Word on Bus B.
5	A RCVR SYNC TYPE	20	−0.4			A HIGH on this input indicates receipt of a Command or Status Word on Bus A. A LOW indicates receipt of a Data Word on Bus A.
6	$\overline{\text{XMIT BUSY}}$			−0.4	4.0	A LOW on this output indicates that the BCU is transmitting.
7	NC					No connection.
8	NC					No connection.
9	NC					No connection.
10	NC					No connection.
11	CASE					Case connection.
12	NO DT			−0.4	4.0	A LOW on this IDLE/$\overline{\text{ACTIVE}}$ output indicates that the BCU is busy handling a message transfer.
13	$\overline{\text{R STROBE}}$			−0.4	4.0	This output goes LOW every time a valid Command or Data Word is received and is available for processing.
14	FAIL SAFE FLAG			−0.4	4.0	A HIGH on this output indicates that a 680μs fail-safe timeout occurred in one of the transmitters interfacing with the data bus.
15	B RCVR BUSY	60	−1.2			This input goes HIGH for nominally 16μs for each word being decoded on either Bus A or Bus B.
16	B SHIFT CLOCK	40	−0.8			Input for a TTL compatible 1 MHz decoder shift clock, which is synchronized with the Manchester coded data being received on Bus B.
17	BC CH$\overline{\text{A}}$/B	40	−0.8			A LOW on this input indicates selection of Channel A.
18	+5V DC					+5V power input.
19	GND					Logic and power return.
20	A SHIFT CLOCK	40	−0.8			Input for a TTL compatible 1 MHz decoder shift clock, which is synchronized with the Manchester coded data being received on Bus A.
21	NC					No connection.
22	A RCVR BUSY	60	−1.2			A HIGH on this input indicates that the BCU is receiving data on Bus A.
23	B XMIT BUSY	20	−0.4			A HIGH on this input indicates that the BCU is transmitting on Bus B.
24	A XMIT BUSY	20	−0.4			A HIGH on this input indicates that the BCU is transmitting on Bus A.
25	A FAIL-SAFE FLAG	40	−0.8			A HIGH on this input indicates that a 680μs timeout occurred on Bus A transmitter.
26	B FAIL-SAFE FLAG	40	−0.8			A HIGH on this input indicates that a 680μs timeout occurred on Bus B transmitter.
27	$\overline{\text{CL 6}}$	50	−2.0			Input for a TTL compatible 6 MHz system clock.
28	NC					No connection.
29	$\overline{\text{RESET}}$	20	−0.4			A LOW on this input (for 0.1μs min.) resets the fault detection and internal circuitry of the BUS-66111 Hybrid.
30	NC					No connection.
31	NC					No connection.
32	NC					No connection.
33	BCU FAIL			−0.4	4.0	A HIGH on this output indicates a fault condition occured during the normal BCU operation.
34	A FAULT	20	−0.4			A HIGH on this input indicates a fault during the loop back on Bus A. This signal sets the BCU Fail Register.
35	B FAULT	20	−0.4			A HIGH on this input indicates a fault during the loop back on Bus B. This signal sets the BCU Fail Register.
36	$\overline{\text{A VALID WORD}}$	20	−0.4			A LOW on this input indicates that the BCU received a valid word on Bus A.

NOTES: In the above table, the symbols are defined as follows:

I_{IH} = maximum input HIGH current with V_{in} = 2.5 volts.

I_{IL} = maximum input LOW current with V_{in} = 0.4 volts.

I_{OH} = maximum output HIGH current with V_{out} = 2.5 volts minimum.

I_{OL} = maximum output LOW current with V_{out} = 0.4 volts maximum.

BUS-66106 PIN FUNCTION AND LOADING TABLE

PIN NO.	NAME	I_{IH} (μA)	I_{IL} (mA)	I_{OH} (mA)	I_{OL} (mA)	DESCRIPTION
1	+5V DC					+5V power input.
2	$\overline{\text{BC OUTPUT ENABLE}}$			−0.4	4.0	A LOW on this output indicates that the Bus Controller is reading data from the subsystem.
3	$\overline{\text{BC ACCESS}}$			−0.36	3.6	A LOW on this output indicates that the Bus Controller is using the Data and Address Tri-State buses.
4	NC					No connection.
5	CASE					Case connection.
6	CL 6	20	−0.4			Input for a 6 MHz system clock, TTL compatible.
7	$\overline{\text{START}}$	20	−0.4			A LOW on this input initiates a word transfer by the hybrid.
8	$\overline{\text{BC LOAD}}$			−0.38	3.6	A LOW pulse on this output loads the data to be transmitted on the Encoder Registers.
9	$\overline{\text{R STROBE}}$	20	−0.4			A LOW pulse on this input starts a sequence to unload the data from the decoder register.
10	BUS CYCLE ENABLE	20	−0.4			A HIGH on this input from the subsystem will initiate a command/response sequence.
11	RECLOCKED CYCLE ENABLE			−0.38	3.6	This output is the Cycle Enable Signal synchronized with the 6 MHz clock.
12	BC NO DT			−0.4	0.4	This output is the NO DT input synchronized with the 6 MHz clock.
13	$\overline{\text{BC ACTIVE}}$			−0.4	4.0	A LOW on this output indicates that the device is processing a message.
14	A6			−1.2	12	MSB of 6 Bit Tri-State Address Bus.
15	A4			−1.2	12	Part of 6 Bit Tri-State Address Bus.
16	A2			−1.2	12	Part of 6 Bit Tri-State Address Bus.
17	$\overline{\text{T BUSY PULSE}}$			−0.4	4.0	A LOW level pulse that follows the trailing edge of $\overline{\text{T BUSY}}$.
18	$\overline{\text{BC CS}}$			−0.4	4.0	A LOW on this output selects a memory device.
19	$\overline{\text{BC WR}}$			−0.4	4.0	A LOW on this output transfers the data to the memory.
20	$\overline{\text{BG ACK}}$			−0.36	3.2	A LOW on this output handshake signal indicates that the device received the B GRANT signal.
21	NC					No connection.
22	COMPLETE			−0.4	4.0	A HIGH on this output indicates that the word transfer cycle is complete.
23	$\overline{\text{COMPLETE}}$			−0.36	3.2	This is the COMPLETE output inverted.
24	BC CMD 10			−0.36	3.2	This is the T/$\overline{\text{R}}$ bit of the Command Word transmitted.
25	NC					No connection.
26	$\overline{\text{BC R ENABLE}}$			−0.4	4.0	A LOW on this output enables the Decoder Register contents onto the internal 16 Bit Data Highway.
27	$\overline{\text{BC SOM}}$	20	−0.4			A LOW on this input resets the internal circuitry of the Hybrid.
28	NO DT	20	−0.4			A LOW on this IDLE/$\overline{\text{ACTIVE}}$ input indicates that the Data Bus Receiver is active.
29	$\overline{\text{BC TIMEOUT}}$			−0.4	4.0	A LOW on this output indicates that there was no reply from the RTU within 15μs.
30	$\overline{\text{T BUSY}}$	20	−0.4			Input to the negative edge triggered circuit which generatcs $\overline{\text{T BUSY PULSE}}$ output.
31	A5			−1.2	12	Part of 6 Bit Tri-State Address Bus.
32	A3			−1.2	12	Part of 6 Bit Tri-State Address Bus.
33	A1			−1.2	12	LSB of 6 Bit Tri-State Address Bus.
34	GND					Power and logic return.

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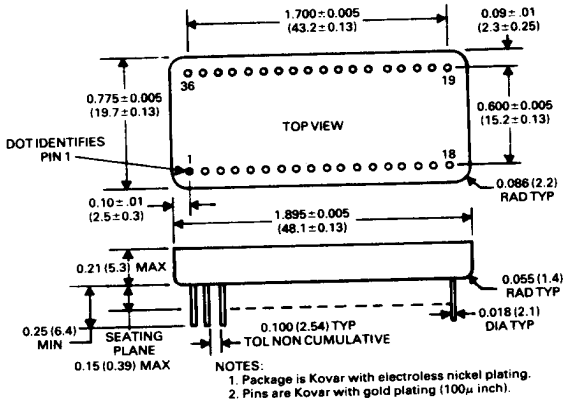
BUS-66106 PIN FUNCTION AND LOADING TABLE (CONTINUED)

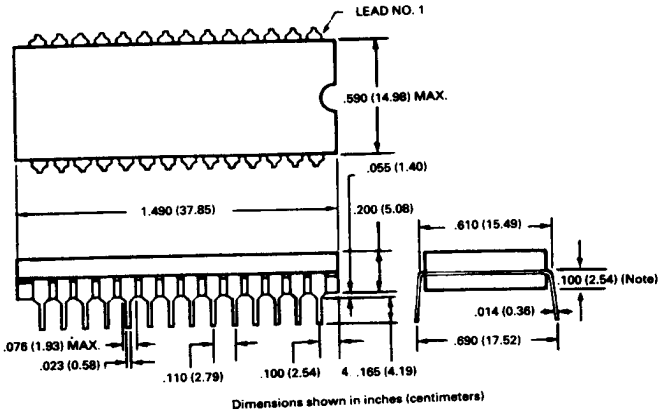
PIN NO.	NAME	I_{IH} (μA)	I_{IL} (mA)	I_{OH} (mA)	I_{OL} (mA)	DESCRIPTION
35	$\overline{\text{STAT SET}}$			−0.4	4.0	A LOW pulse on this output indicates a bit set or address mismatch in the Status Word received.
36	$\overline{\text{BC T ENABLE}}$	20	−0.4			This is one of a group of four Bus Controller mode code signals. A LOW on this input enables the transmit cycle.
37	$\overline{\text{BC REPLY}}$	−40	0.8			This is one of a group of four Bus Controller mode signals. A LOW on this input enables the reply cycle.
38	$\overline{\text{BUS REQUEST}}$			−0.38	3.6	A LOW on this handshake output signal indicates a request to access the Tri-State Data and Address Buses.
39	D 13	20	−0.2			Part of 16 Bit Tri-State Data input
40	D 15	20	−0.2			MSB of 16 Bit Tri-State Data input.
41	D 9	20	−0.2			Part of 16 Bit Tri-State Data input.
42	D 11	20	−0.2			Part of 16 Bit Tri-State Data input.
43	$\overline{\text{CTW3}}$			−0.4	4.0	Part of 8 Bit Control Word Register output.
44	$\overline{\text{CTW1}}$			−0.4	4.0	Part of 8 Bit Control Word Register. A LOW indicates a Broadcast Command.
45	$\overline{\text{CTW7}}$			−0.4	4.0	MSB of 8 Bit Control Word Register output. A LOW output selects MIL-STD-1553 Channel A.
46	$\overline{\text{CTW5}}$			−0.4	4.0	Part of 8 bit Control Word Register output.
47	D4	20	−0.2			Part of 16 bit Tri-State Data input.
48	D6	20	−0.2			Part of 16 bit Tri-State Data input.
49	D0	20	−0.2			LSB of 16 bit Tri-State Data input.
50	D2	20	−0.2			Part of 16 bit Tri-State Data input.
51	+5V					+5V Power supply.
52	GND					Power and logic return.
53	$\overline{\text{BC DT}}$	40	−0.8			This is one of a group of four Bus Controller mode signals. A LOW on this input indicates Data Word transfer on the Data Bus.
54	$\overline{\text{BC LOAD}}$	40	−0.8			This is one of a group of four Bus Controller mode signals. A LOW on this input indicates a Data Word to be loaded in the Encoder.
55	$\overline{\text{B GRANT}}$	20	−0.4			A LOW on this input indicates that the subsystem relinquished control of the Tri-State Buses.
56	D 12	20	−0.2			Part of 16 Bit Tri-State Data input.
57	D 14	20	−0.2			Part of 16 Bit Tri-State Data input.
58	D 8	20	−0.2			Part of 16 Bit Tri-State Data input.
59	D 10	20	−0.2			Part of 16 Bit Tri-State Data input.
60	BC L WORD			−0.4	4.0	A HIGH on this output indicates that the last Data Word has been transferred.
61	$\overline{\text{CTW2}}$			−0.4	4.0	Part of 8 Bit Control Word Register output. A LOW indicates a Mode Code Command.
62	$\overline{\text{CTW0}}$			−0.4	4.0	LSB of 8 Bit Control Word Register. A LOW indicates an RT to RT Command.
63	$\overline{\text{CTW6}}$			−0.4	4.0	Part of 8 Bit Control Word Register output.
64	$\overline{\text{CTW4}}$			−0.4	4.0	Part of 8 Bit Control Word Register output.
65	D 5	20	−0.2			Part of 16 Bit Tri-State Data input.
66	D 7	20	−0.2			Part of 16 Bit Tri-State Data input.
67	D 1	20	−0.2			Part of 16 Bit Tri-State Data input.
68	D 3	20	−0.2			Part of 16 Bit Tri-State Data input.

See notes following BUS-66111 Pin Function Table.

MECHANICAL OUTLINE BUS-66111

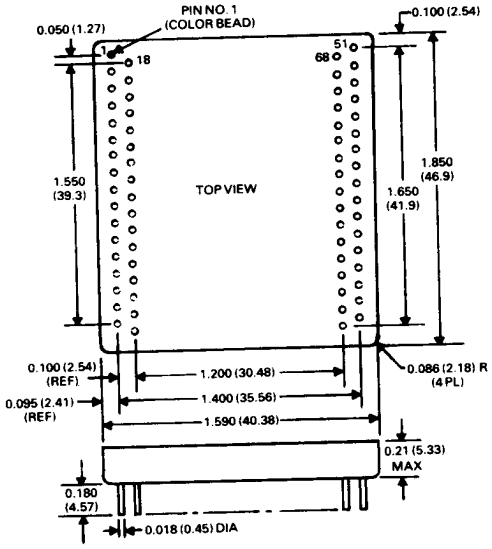


MECHANICAL OUTLINE #464340040037



MECHANICAL OUTLINE BUS 66106

Dimensions are in inches (millimeters)



ORDERING INFORMATION

BUS-66111-883B
BUS-66106-883B

Reliability Grade:

883B = Fully compliant with MIL-STD-883.
—B = Screened to MIL-STD-883 but without QCI testing.
Blank = Screened to MIL-STD-883 but without pre burn-in testing, burn-in, and QCI testing.

#464340040037 State Sequencer PLS

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