

LM6687

Ultra Fast Dual Voltage Comparators

General Description

The LM6687 is an ultra fast dual voltage comparator manufactured with an advanced high speed bipolar process that makes possible very short propagation delays (2.6 ns) with excellent matching characteristics. These comparators have differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output current capability is adequate for driving terminated 50Ω transmission lines. The low input offsets and short delays make these comparators especially suitable for high speed precision analog-to-digital processing.

Separate latch functions are provided to allow each comparator to be independently used in a sample and hold mode. The latch function inputs are designed to be driven from the complementary outputs of a standard ECL gate. If latch enable is HIGH and latch enable is LOW, the comparator functions normally. When latch enable is driven LOW

and latch enable is driven HIGH, the comparator outputs are locked in their existing logical states. Should the latch function not be used, latch enable must be connected to ground. The LM6687 is lead compatible with the AD96687 and SP9687.

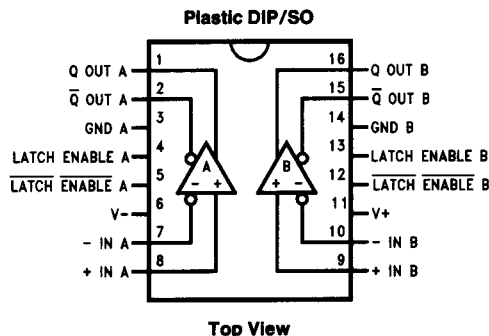
Features

- 2.6 ns Typical propagation delay at 10 mV overdrive
- Complementary ECL outputs
- 50Ω line driving capability
- 1.0 ns Latch set up time

Applications

- High-speed analog-to-digital processing
- High-speed window comparator

Connection Diagram



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Ordering Information

Temperature Range	Package	NSC Package Number
-30°C to +85°C		
LM6687IN	Molded DIP	N16A
LM6687IM	Surface Mount	M16A

Absolute Maximum Ratings (Note 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	–65°C to +150°C
Molded DIP	
Lead Temperature	
Molded DIP (Soldering, 10 sec.)	265°C
Internal Power Dissipation (Note 1)	
16L-Molded DIP	1.45W
16L-Surface Mount	0.95W
Positive Supply Voltage	+7.0V
Negative Supply Voltage	–7.0V
Junction Temperature	150°C

Input Voltage	±4.0V
Differential Input Voltage	±6.0V
Output Current	30 mA

Operating Ratings (Note 4)

Temperature Range	
Industrial	–30°C to +85°C
Positive Supply Voltage	+5.0V
Negative Supply Voltage	–5.2V
Minimum Operating Voltage (V+ to V–)	9.7V
Thermal Resistance (Note 5)	

LM6687**DC Electrical Characteristics** (Note 2)

Symbol	Parameter	Conditions	LM6687I			Units
			Typ	Min	Max	
V _{IO}	Input Offset Voltage	R _S ≤ 100Ω, T _A = 25°C	0.6	–1.9	+1.9	mV
		R _S ≤ 100Ω		–2.5	+2.5	
ΔV _{IO} /ΔT	Average Temperature Coefficient of Input Offset Voltage (Note 3)	R _S ≤ 100Ω	2.5			μV/°C
I _{IO}	Input Offset Current (Note 3)	25°C ≤ T _A ≤ T _A Max	0.1	–1.0	+1.0	μA
		T _A = T _A Min	0.1	–1.3	+1.3	
I _{IB}	Input Bias Current	25°C ≤ T _A ≤ T _A Max	3.0		9	μA
		T _A = T _A Min	4.0		11	
V _{CM}	Input Common Mode Range		+2.7	–3.3	+2.7	V
CMR	Common Mode Rejection	R _S ≤ 100Ω, (Note 6) –3.3 ≤ V _{CM} ≤ +2.7V	112	80		dB
PSRR	Power Supply Rejection Ratio	R _S ≤ 100Ω, ΔV _S = ±5% (Note 6)	80	70		dB
V _{OH}	Output Voltage HIGH	T _A = 25°C	–0.885	–0.960	–0.810	V
		T _A = T _A Min	–0.975	–1.060	–0.890	
		T _A = T _A Max	–0.795	–0.890	–0.700	
V _{OL}	Output Voltage LOW	T _A = 25°C	–1.750	–1.850	–1.650	V
		T _A = T _A Min	–1.783	–1.890	–1.675	
		T _A = T _A Max	–1.725	–1.825	–1.625	
I ⁺	Positive Supply Current		25		32	mA
I [–]	Negative Supply Current		30		38	mA
P _C	Power Consumption		340		420	mW

Switching Characteristics $V_{IN} = 100\text{ mV}$, $V_{OD} = 10\text{ mV}$ (Notes 2, 3)

Symbol	Parameter	Conditions	LM66871			Units
			Typ	Min	Max	
t_{PD+} , t_{PD-}	Propagation Delay (Note 3)	$T_A = 25^\circ\text{C}$	2.6		3.5	ns
t_S	Minimum Latch Set Up Time (Note 3)	$T_A = 25^\circ\text{C}$	0.5		1.0	ns

Note 1: Ratings apply to ambient temperature at 25°C .

Note 2: Unless otherwise specified $V^+ = +5.0\text{V}$, $V^- = -5.2\text{V}$, $R_L = 50\Omega$ to termination voltage $V_T = -2.0\text{V}$; all switching characteristics are for a 100 mV input step with 10 mV overdrive. The specifications given for V_{IO} , I_{IO} , I_{IB} , CMRR, PSRR, apply over the full V_{CM} range and for $\pm 5\%$ supply voltage tolerances. $T_A = T_J$.

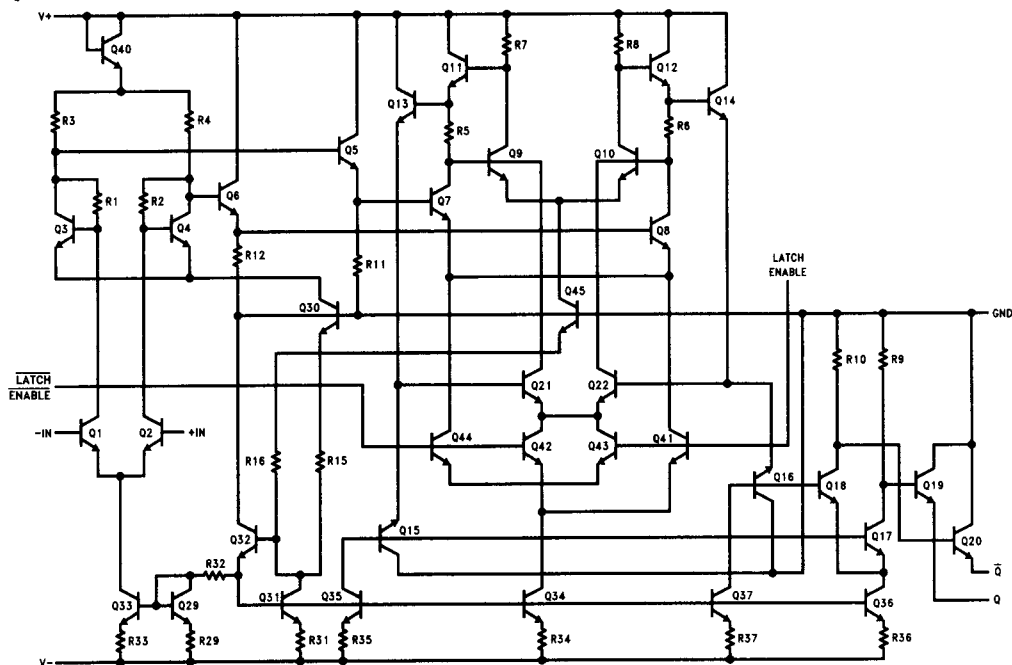
Note 3: Guaranteed, but not tested in production.

Note 4: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 5: The junction-to-ambient thermal resistance of the molded plastic DIP (N) is 86°C/W , the molded plastic SO (M) package is 132°C/W . All numbers apply for packages soldered directly into a PC board.

Note 6: Limit applies for 25°C only.

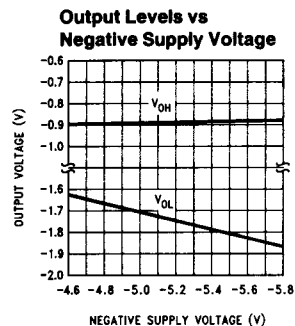
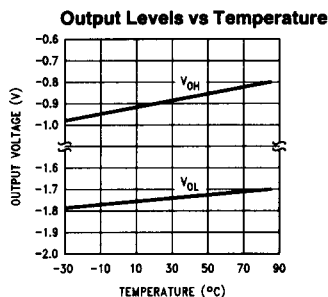
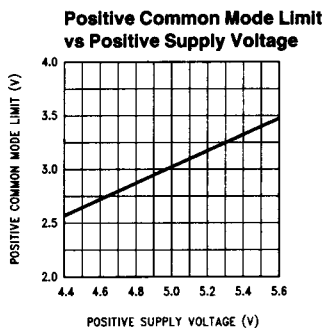
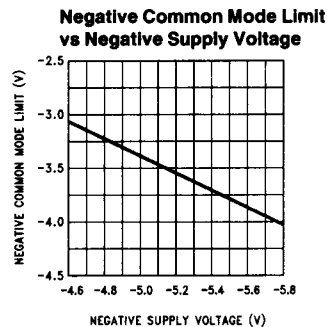
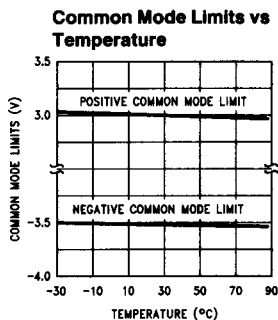
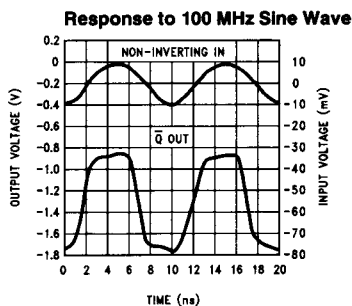
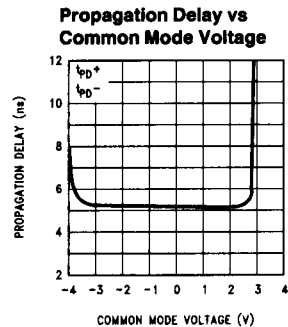
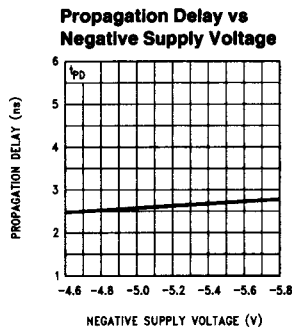
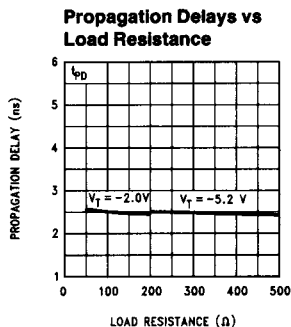
Equivalent Circuit (Each Comparator)



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Typical Performance Characteristics

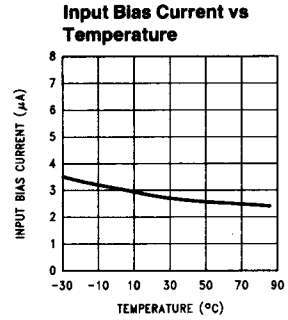
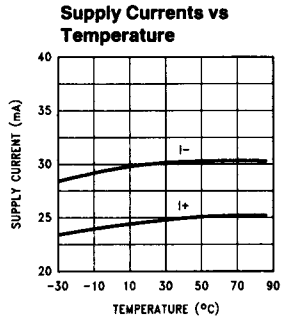
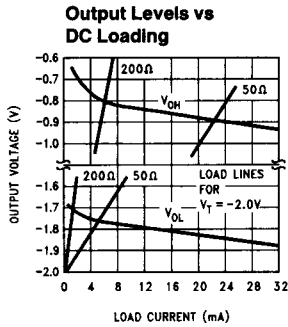
$T_A = 25^\circ\text{C}$, $V_+ = 5.0\text{V}$, $V_- = -5.2\text{V}$, $V_T = -2.0\text{V}$, $R_L = 50\Omega$ and switching characteristics are for $V_{IN} = 100\text{mV}$, $V_{OD} = 10\text{mV}$, unless otherwise specified



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Typical Performance Characteristics

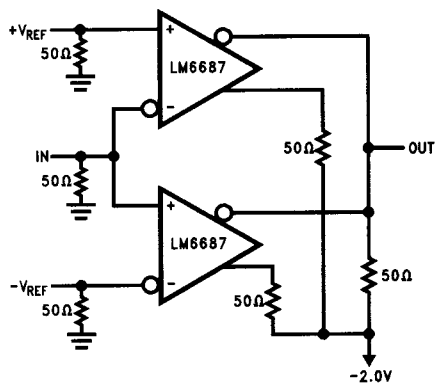
$T_A = 25^\circ\text{C}$, $V_+ = 5.0\text{V}$, $V_- = -5.2\text{V}$, $V_T = -2.0\text{V}$, $R_L = 50\Omega$ and switching characteristics are for $V_{IN} = 100\text{mV}$, $V_{OD} = 10\text{mV}$, unless otherwise specified (Continued)



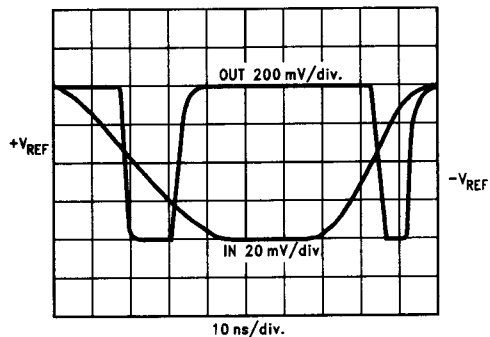
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Typical Applications $(T_A = 25^\circ\text{C})$

High Speed Window Detector

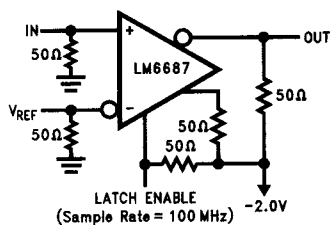


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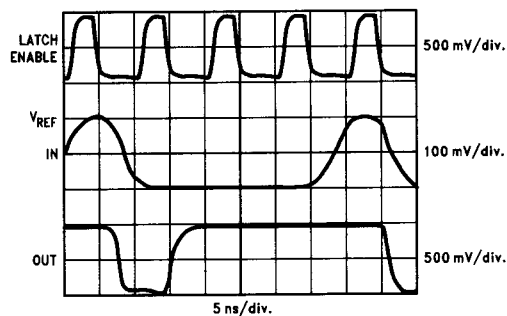


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High Speed Sampling

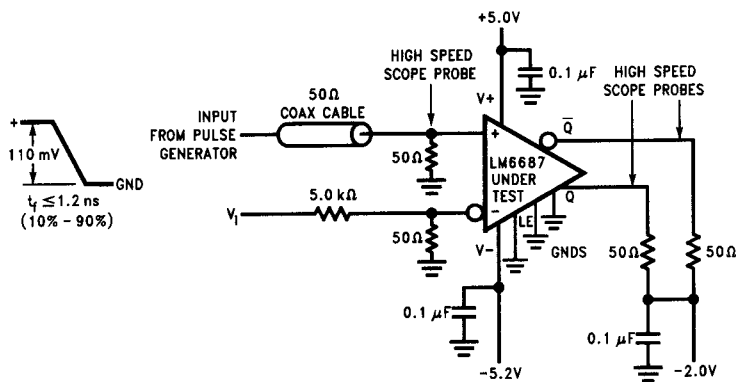


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Application Information



Propagation Delay Test Circuit

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Measurement Of Propagation Delay

Propagation delays $t_{PD} + (\bar{Q}$ output) and $t_{PD} - (Q$ output) are measured with input signal conditions of a 100 mV step with an overdrive of 10 mV (the overdrive is the voltage in excess of that needed to bring the output to the center of its dynamic range). Offset is compensated for by adjusting V_I until outputs are in the linear region while the Pulse Generator is disconnected. V_I is then increased in the positive direction so inverting input changes by 10 mV, i.e. the overdrive condition. Propagation delays are then measured with actual input pulse condition of +110 mV to 0V swing, with a $t_{PD} +$ or $t_{PD} -$ reading taken between the +10 mV level of the input pulse and the 50% point of the outputs.

Thermal Considerations

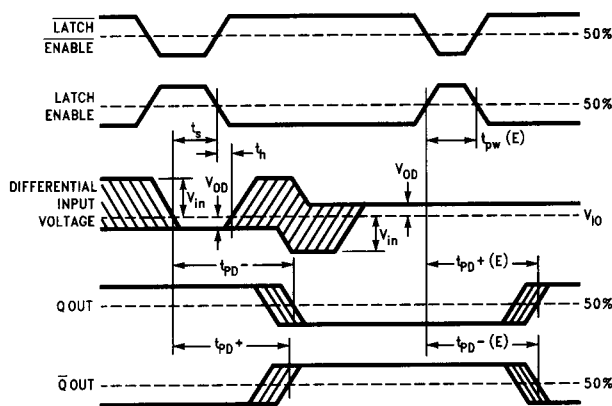
To achieve the high speed of the LM6687, a certain amount of power must be dissipated as heat. This increases the temperature of the die relative to the ambient temperature. In order to be compatible with ECL III and ECL 10,000, which normally use air flow as a means of package cooling, the device must have an air flow across the package of 500 linear feet per minute or greater. Thus, even though different ECL circuits on a printed circuit board may have different power dissipations, all will have the same input and output levels, etc. provided each sees the same air flow and air temperature. This eases design, since the only change in characteristics between devices is due to the increase in

ambient temperature of the air passing over the devices. If the LM6687 is operated without air flow, the change in electrical characteristics due to the increased die temperature must be taken into account.

Interconnection Techniques

All high speed ECL circuits require that special precautions be taken for optimum system performance. The LM6687 is particularly critical because it features very high gain (60 dB) at very high frequencies (100 MHz). A ground plane must be provided for a good, low inductance, ground current return path. The impedance at the inputs should be as low as possible and lead lengths as short as practical. It is preferable to solder the device directly to the printed circuit board instead of using a socket. Open wiring on the outputs should be limited to less than one inch, since severe ringing occurs beyond this length. For longer lengths, the printed circuit interconnections become microstrip transmission lines when backed up by a ground plane, with a characteristic impedance of 50 to 150Ω. Reflections will occur unless the line is terminated in its characteristic impedance. The termination resistors normally go to -2.0V, but a Thevenin equivalent to V_{-} can be used at some increase in power. Best results are usually obtained with the terminating resistor at the end of the driven line. The lower impedance lines are more suitable for driving capacitive loads. The supply voltages should be decoupled with RF capacitors connected to the ground plane as close to the device supply leads as possible.

Timing Diagram



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Note: The setup and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal changes occurring before t_s will be detected and held; those occurring after t_h will not be detected. Changes between t_s and t_h may or may not be detected.

Key to Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

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Definition of Terms

V_{IO}	Input Offset Voltage —That voltage which must be applied between the two input terminals through two equal resistances to obtain zero voltage between the two outputs.
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage —The ratio of the change in input offset voltage over the operating temperature range to the temperature range.
I_{IO}	Input Offset Current —The difference between the currents into the two input terminals when there is zero voltage between the two outputs.
I_{IB}	Input Bias Current —The average of the two input currents.
R_i	Input Resistance —The resistance looking into either input terminal with the other grounded.
C_i	Input Capacitance —The capacitance looking into either input terminal with other grounded.
V_{CM}	Common Mode Voltage Range —The range of voltages on the input terminals for which the offset and propagation delay specifications apply.
CMR	Common Mode Rejection —The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.
PSRR	Power Supply Rejection Ratio —The ratio of the change in input offset voltage to the change in power supply voltages producing it.
V_{OH}	Output Voltage HIGH —The logic HIGH output voltage with an external pull-down resistor returned to a negative supply.
V_{OL}	Output Voltage LOW —The logic LOW output voltage with an external pull-down resistor returned to a negative supply.
I_+	Positive Supply Current —The current required from the positive supply to operate the comparator.
I_-	Negative Supply Current —The current required from the negative supply to operate the comparator.
P_c	Power Consumption —The power dissipated by the comparator with both outputs terminated in 50Ω to $-2.0V$.

Switching Terms (see Timing Diagram)

t_{PD+}	Input to Output HIGH Delay —The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.
t_{PD-}	Input to Output LOW Delay —The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.
$t_{PD+(E)}$	Latch Enable to Output HIGH Delay —The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.
$t_{PD-(E)}$	Latch Enable to Output LOW Delay —The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to the 50% point of an output HIGH to LOW transition.
t_S	Minimum Setup Time —The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.
t_H	Minimum Hold Time —The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.
$t_{pw(E)}$	Minimum Latch Enable Pulse Width —The minimum time that the Latch Enable signal must be HIGH in order to acquire and hold an input signal change.

Other Symbols

T_A	Ambient temperature
R_S	Input source resistance
V_{CC}	Supply voltages
V_+	Positive supply voltage
V_-	Negative supply voltage
V_T	Output load terminating voltage
R_L	Output load resistance
V_{IN}	Input pulse amplitude
V_{OD}	Input overdrive
f	Frequency