

DATA SHEET

BUT12; BUT12A Silicon diffused power transistors

Product specification
Supersedes data of February 1996
File under Discrete Semiconductors, SC06

1997 Aug 13

Philips
Semiconductors



PHILIPS

Silicon diffused power transistors

BUT12; BUT12A

DESCRIPTION

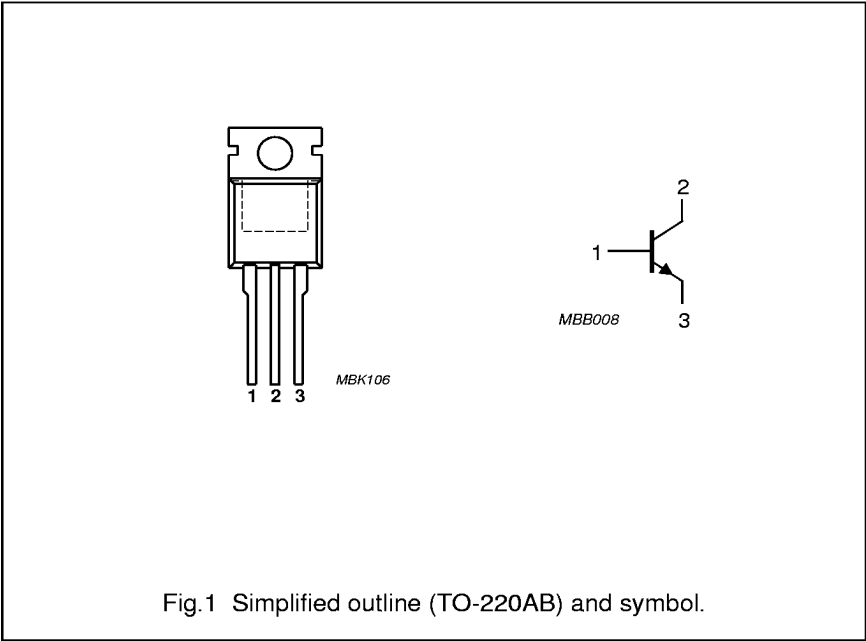
High-voltage, high-speed, glass-passivated NPN power transistor in a TO-220AB package.

APPLICATIONS

- Converters
- Inverters
- Switching regulators
- Motor control systems.

PINNING

PIN	DESCRIPTION
1	base
2	collector; connected to mounting base
3	emitter



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{CESM}	collector-emitter peak voltage BUT12 BUT12A	$V_{BE} = 0$	850 1000	V V
V_{CEO}	collector-emitter voltage BUT12 BUT12A	open base	400 450	V V
V_{CEsat}	collector-emitter saturation voltage	see Fig.8	1.5	V
I_{Csat}	collector saturation current BUT12 BUT12A		6 5	A A
I_C	collector current (DC)	see Figs 3 and 4	8	A
I_{CM}	collector current (peak value)	see Fig. 4	20	A
P_{tot}	total power dissipation	$T_{mb} \leq 25\text{ }^{\circ}\text{C}$; see Fig.2	125	W
t_f	fall time	resistive load; see Figs 12 and 13	0.8	μs

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-mb}$	thermal resistance from junction to mounting base	1	K/W

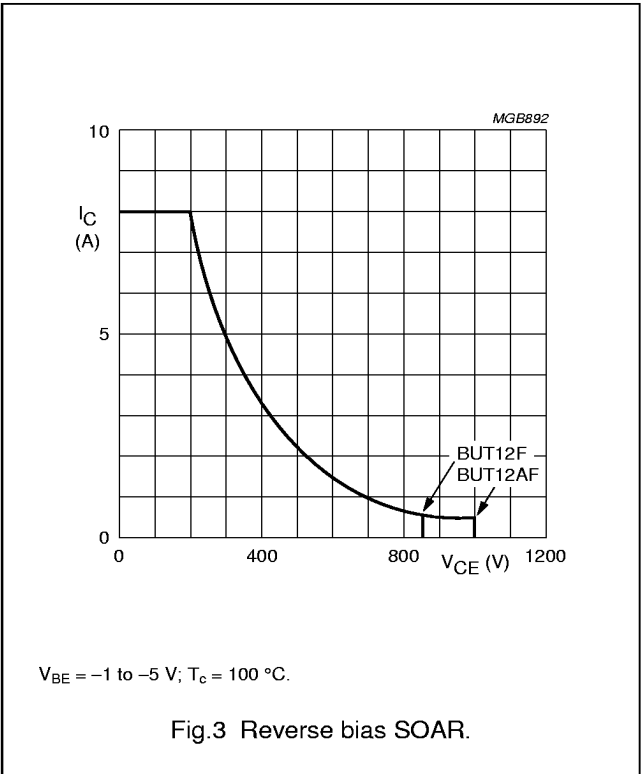
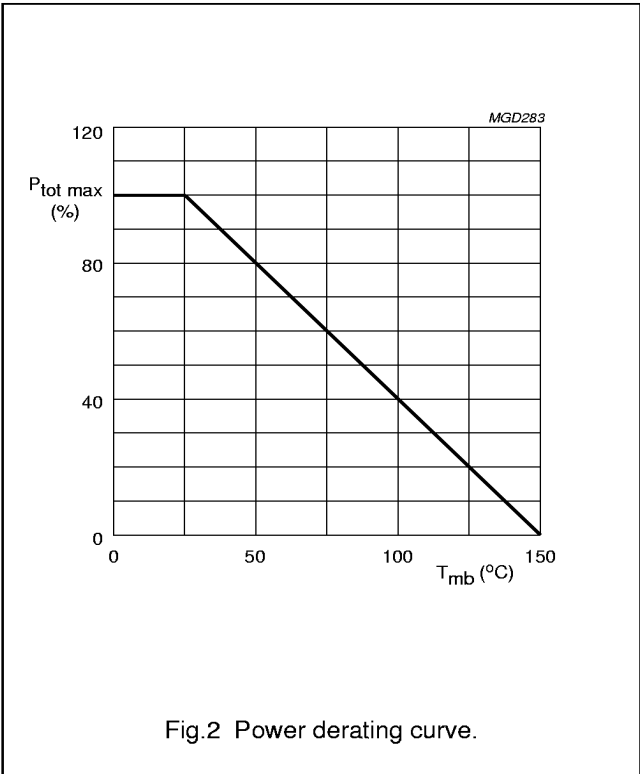
Silicon diffused power transistors

BUT12; BUT12A

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CESM}	collector-emitter peak voltage	$V_{BE} = 0$	—	850	V
	BUT12			1000	V
V_{CEO}	collector-emitter voltage	open base	—	400	V
	BUT12A			450	V
I_{Csat}	collector saturation current		—	6	A
	BUT12A			5	A
I_C	collector current (DC)	see Figs 3 and 4	—	8	A
I_{CM}	collector current (peak value)	see Fig. 4	—	20	A
I_B	base current (DC)		—	4	A
I_{BM}	base current (peak value)		—	6	A
P_{tot}	total power dissipation	$T_{mb} \leq 25\text{ }^{\circ}\text{C}$; see Fig.2	—	125	W
T_{stg}	storage temperature		−65	+150	$^{\circ}\text{C}$
T_j	junction temperature		—	150	$^{\circ}\text{C}$



Silicon diffused power transistors

BUT12; BUT12A

CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

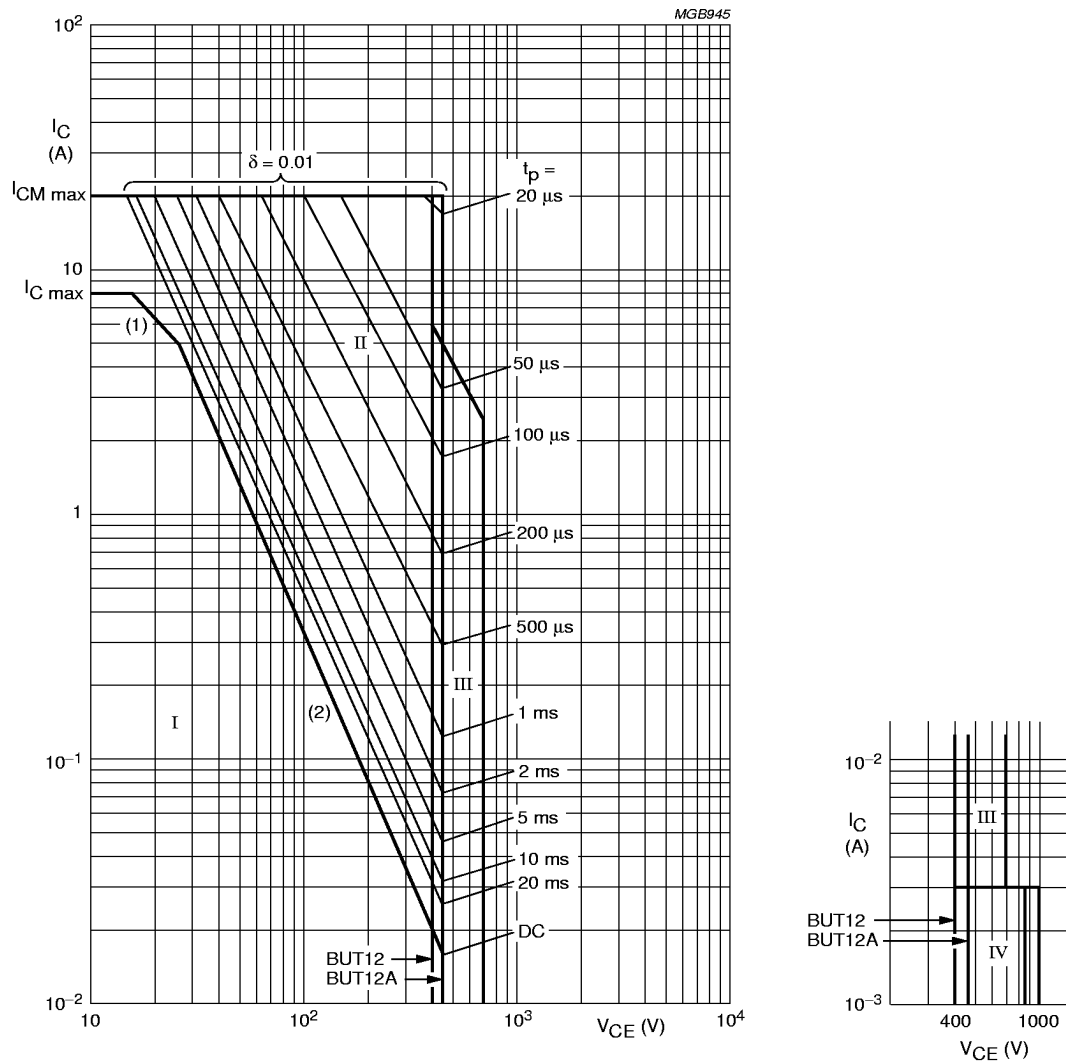
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CEOsust}$	collector-emitter sustaining voltage BUT12 BUT12A	$I_C = 100\text{ mA}$; $I_{Boff} = 0$; $L = 25\text{ mH}$; see Figs 6 and 7	400	—	—	V
			450	—	—	V
V_{CEsat}	collector-emitter saturation voltage BUT12 BUT12A	$I_C = 6\text{ A}$; $I_B = 1.2\text{ A}$; see Figs 8 and 10	—	—	1.5	V
		$I_C = 5\text{ A}$; $I_B = 1\text{ A}$; see Figs 8 and 10	—	—	1.5	V
V_{BEsat}	base-emitter saturation voltage BUT12 BUT12A	$I_C = 6\text{ A}$; $I_B = 1.2\text{ A}$; see Fig.8	—	—	1.5	V
		$I_C = 5\text{ A}$; $I_B = 1\text{ A}$; see Fig.8	—	—	1.5	V
I_{CES}	collector-emitter cut-off current	$V_{CE} = V_{CESmax}$; $V_{BE} = 0$; note 1	—	—	1	mA
		$V_{CE} = V_{CESmax}$; $V_{BE} = 0$; $T_j = 125\text{ }^{\circ}\text{C}$; note 1	—	—	3	mA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 9\text{ V}$; $I_C = 0$	—	—	10	mA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}$; $I_C = 10\text{ mA}$; see Fig.11	10	18	35	
		$V_{CE} = 5\text{ V}$; $I_C = 1\text{ A}$; see Fig.11	10	20	35	
Switching times resistive load (see Figs 12 and 13)						
t_{on}	turn-on time BUT12 BUT12A	$I_{Con} = 6\text{ A}$; $I_{Bon} = -I_{Boff} = 1.2\text{ A}$	—	—	1	μs
		$I_{Con} = 5\text{ A}$; $I_{Bon} = -I_{Boff} = 1\text{ A}$	—	—	1	μs
t_s	storage time BUT12 BUT12A	$I_{Con} = 6\text{ A}$; $I_{Bon} = -I_{Boff} = 1.2\text{ A}$	—	—	4	μs
		$I_{Con} = 5\text{ A}$; $I_{Bon} = -I_{Boff} = 1\text{ A}$	—	—	4	μs
t_f	fall time BUT12 BUT12A	$I_{Con} = 6\text{ A}$; $I_{Bon} = -I_{Boff} = 1.2\text{ A}$	—	—	0.8	μs
		$I_{Con} = 5\text{ A}$; $I_{Bon} = -I_{Boff} = 1\text{ A}$	—	—	0.8	μs
Switching times inductive load (see Figs 14 and 15)						
t_s	storage time BUT12 BUT12A	$I_{Con} = 6\text{ A}$; $I_{Bon} = 1.2\text{ A}$; $V_{CL} = 250\text{ V}$; $T_c = 100\text{ }^{\circ}\text{C}$	—	1.9	2.5	μs
		$I_{Con} = 5\text{ A}$; $I_{Bon} = 1\text{ A}$; $V_{CL} = 300\text{ V}$; $T_c = 100\text{ }^{\circ}\text{C}$	—	1.9	2.5	μs
t_f	fall time BUT12 BUT12A	$I_{Con} = 6\text{ A}$; $I_{Bon} = 1.2\text{ A}$; $V_{CL} = 250\text{ V}$; $T_c = 100\text{ }^{\circ}\text{C}$	—	200	300	ns
		$I_{Con} = 5\text{ A}$; $I_{Bon} = 1\text{ A}$; $V_{CL} = 300\text{ V}$; $T_c = 100\text{ }^{\circ}\text{C}$	—	200	300	ns

Note

1. Measured with a half-sinewave voltage (curve tracer).

Silicon diffused power transistors

BUT12; BUT12A



$T_{mb} < 25\ ^\circ\text{C}$.

I - Region of permissible DC operation.

II - Permissible extension for repetitive pulse operation.

(1) $P_{tot\ max}$ and $P_{tot\ peak\ max}$ lines.

(2) Second breakdown limits.

Fig.4 Forward bias SOAR.

Silicon diffused power transistors

BUT12; BUT12A

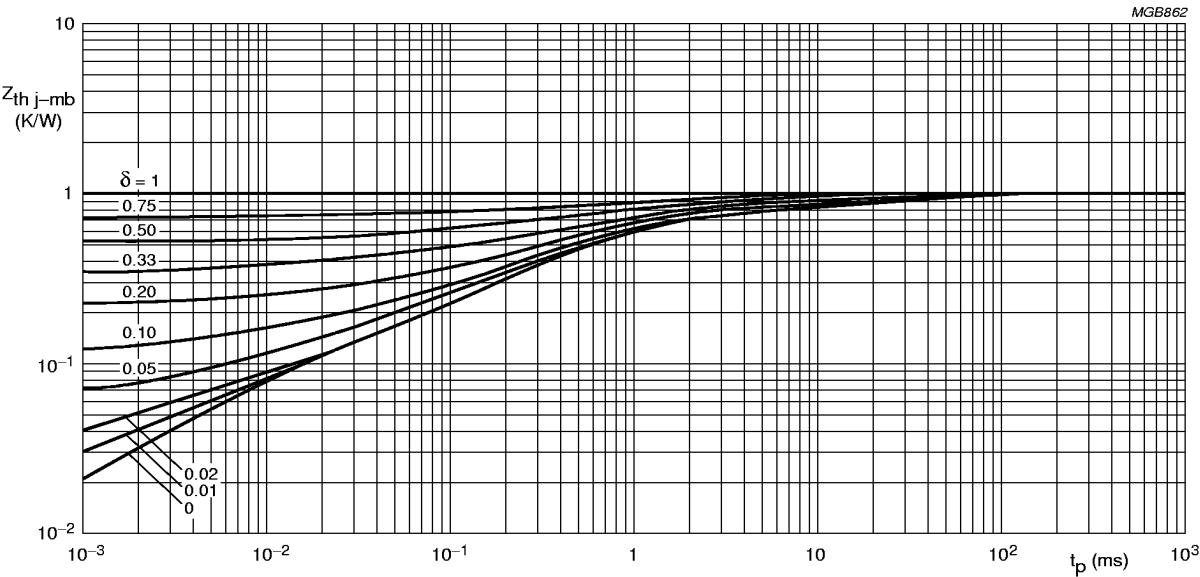


Fig.5 Transient thermal impedance.

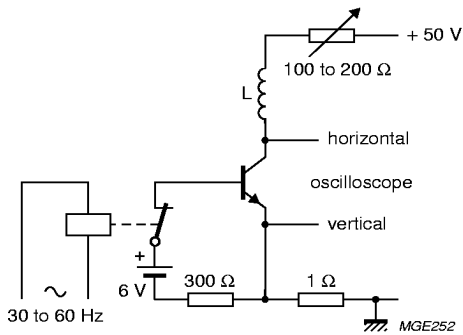


Fig.6 Test circuit for collector-emitter sustaining voltage.

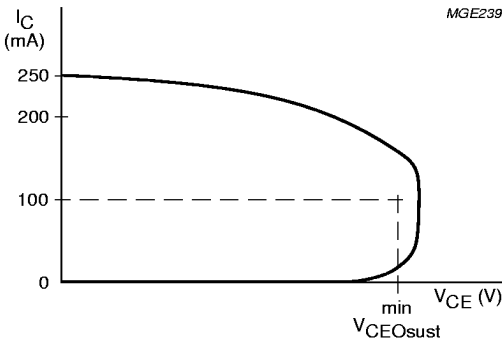
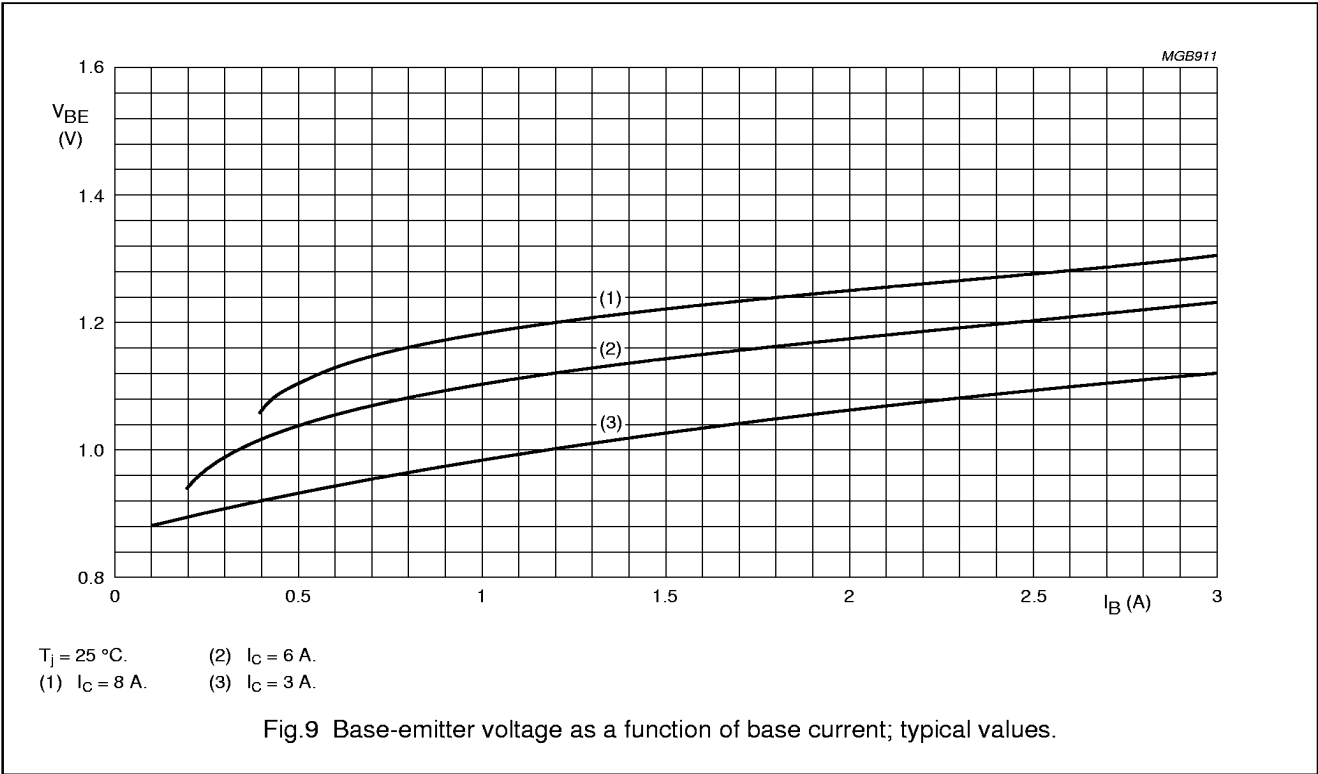
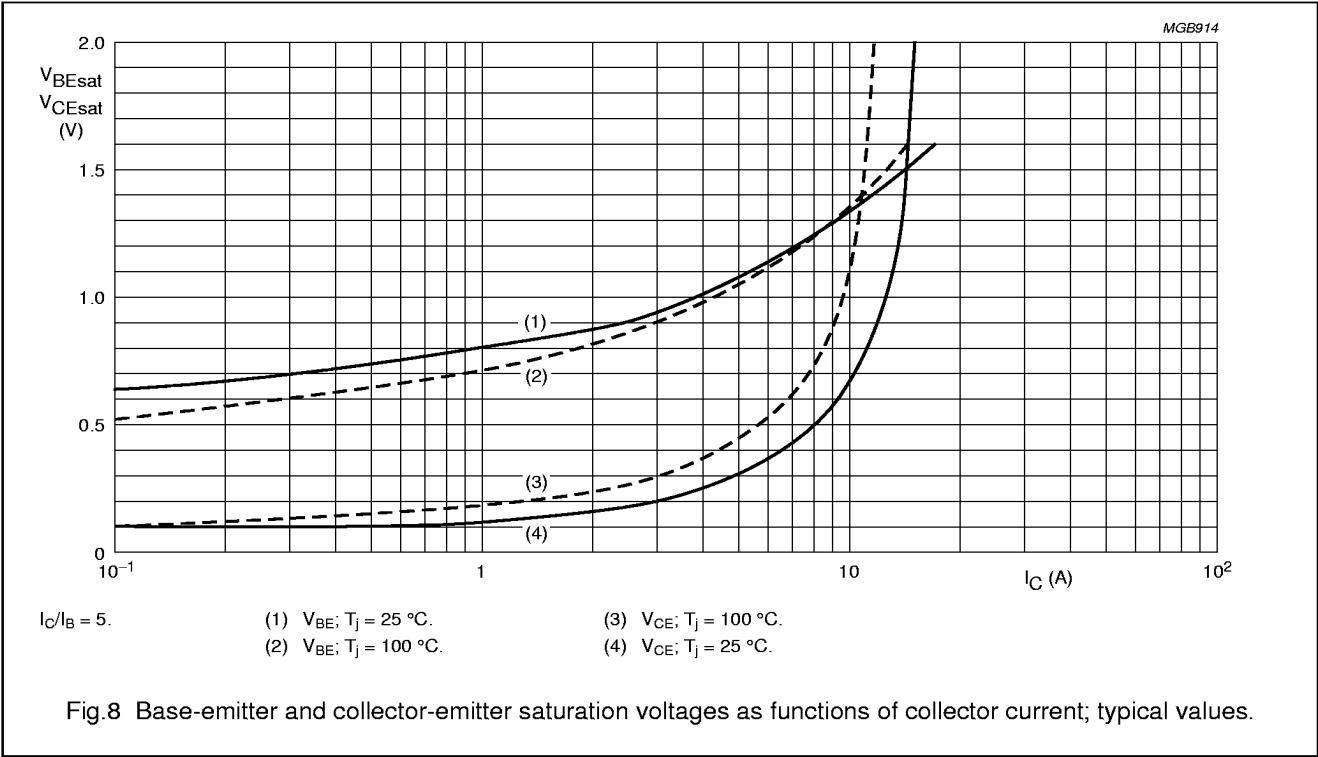


Fig.7 Oscilloscope display for collector-emitter sustaining voltage.

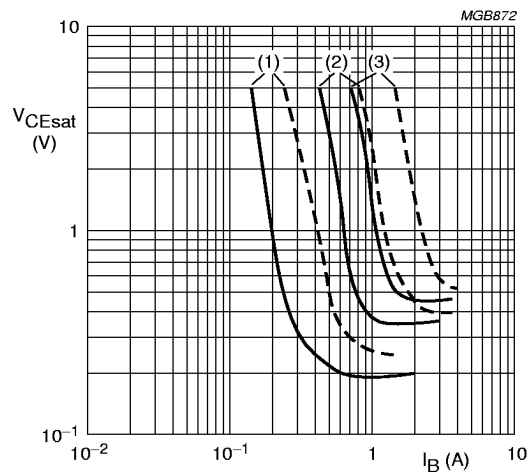
Silicon diffused power transistors

BUT12; BUT12A



Silicon diffused power transistors

BUT12; BUT12A



(1) $I_C = 3$ A.
(2) $I_C = 6$ A.
(3) $I_C = 8$ A.
 $T_J = 25$ °C; solid line: typical values; dotted line: maximum values.

Fig.10 Collector-emitter saturation voltage as a function of base current.

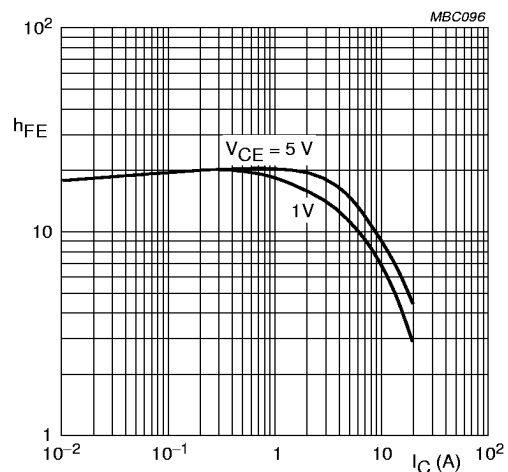
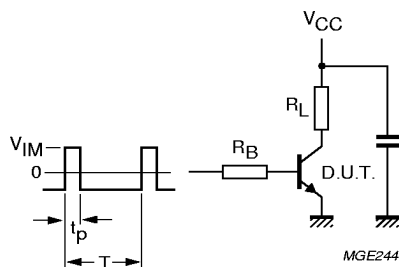
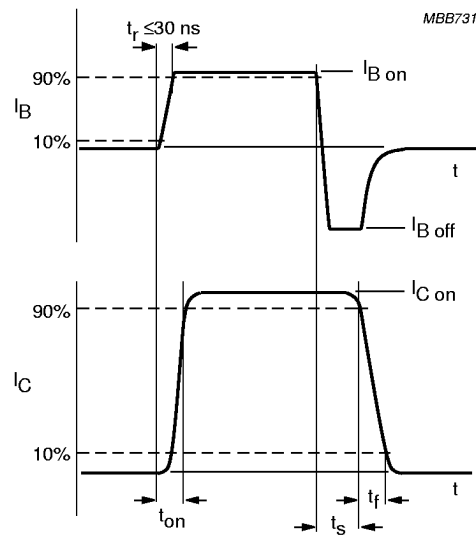


Fig.11 DC current gain; typical values.



$V_{CC} = 250$ V; $t_p = 20$ μ s; $V_{IM} = -6$ to $+8$ V; $t_p/T = 0.01$.
The values of R_B and R_L are selected in accordance with I_{Con} and I_{Bon} requirements.

Fig.12 Test circuit resistive load.

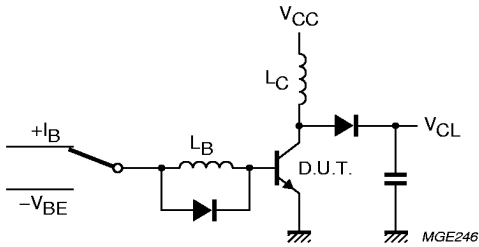


$t_r \leq 20$ ns.

Fig.13 Switching time waveforms with resistive load.

Silicon diffused power transistors

BUT12; BUT12A



V_{CL} = up to 1000 V; V_{CC} = 30 V; V_{BE} = -1 to -5 V; L_B = 1 μ H; L_C = 200 μ H.

Fig.14 Test circuit inductive load and reverse bias SOAR.

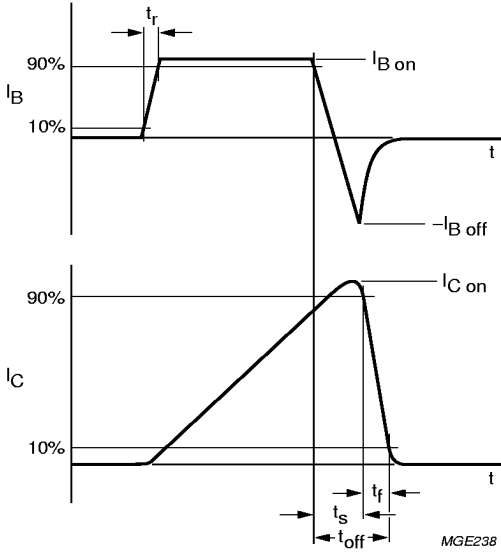


Fig.15 Switching time waveforms with inductive load.

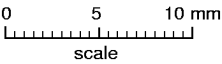
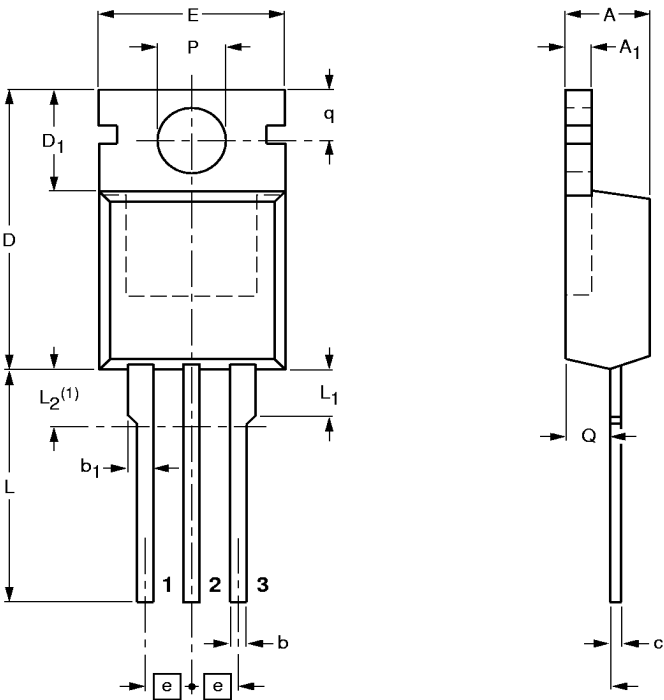
Silicon diffused power transistors

BUT12; BUT12A

PACKAGE OUTLINE

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220

SOT78



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁	c	D	D ₁	E	e	L	L ₁	L ₂ ⁽¹⁾ max.	P	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

Note

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		TO-220				97-06-11