

# Negative Output Flyback Pulse Width Modulator

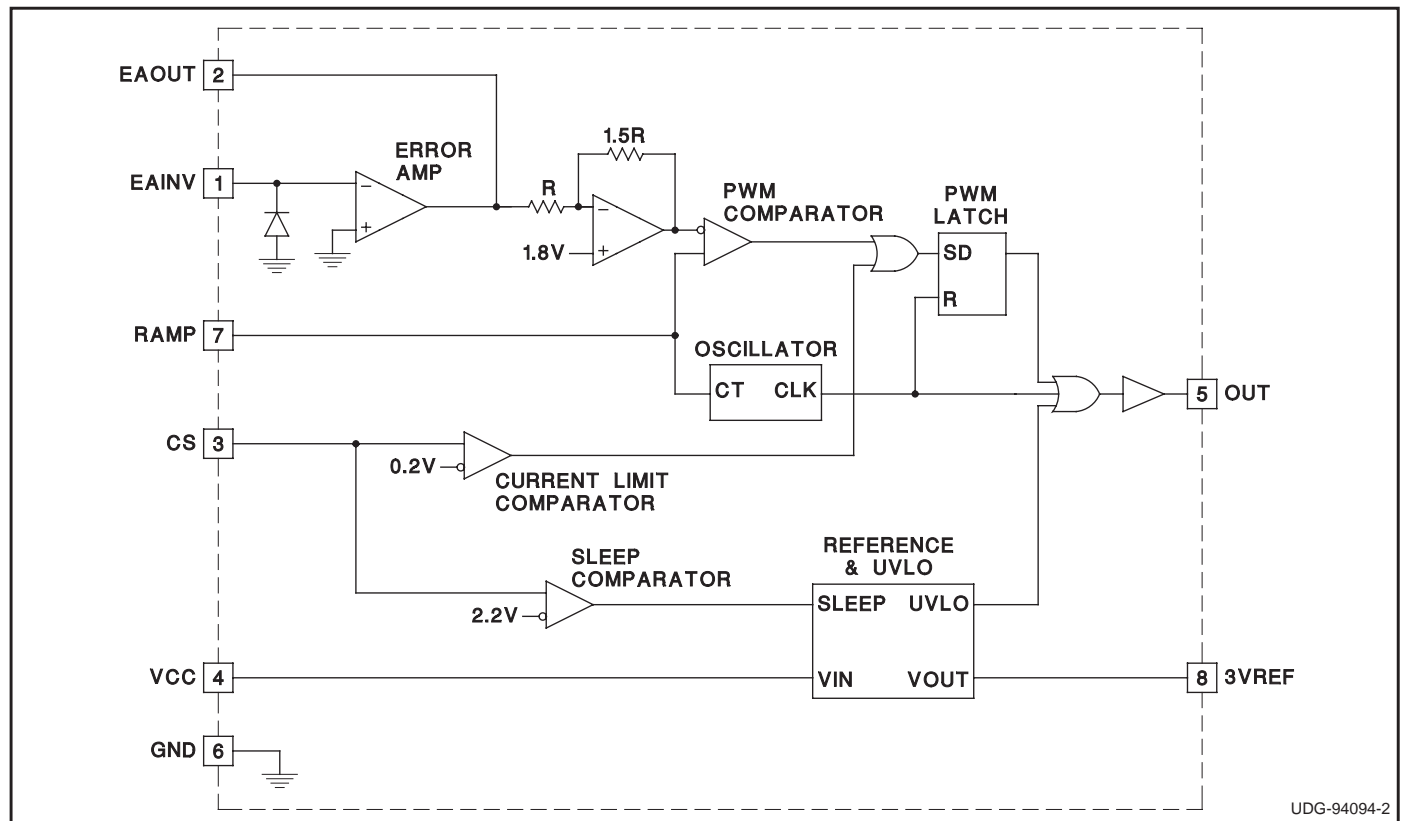
## FEATURES

- Simple Single Inductor Flyback PWM for Negative Voltage Generation
- Drives External PMOS Switch
- Contains UVLO Circuit
- Includes Pulse-by-Pulse Current Limit
- Low 50 $\mu$ A Sleep Mode Current

## DESCRIPTION

The UC3572 is a negative output flyback pulse width modulator which converts a positive input voltage to a regulated negative output voltage. The chip is optimized for use in a single inductor negative flyback switching converter employing an external PMOS switch. The block diagram consists of a precision reference, an error amplifier configured for voltage mode operation, an oscillator, a PWM comparator with latching logic, and a 0.5A peak gate driver. The UC3572 includes an undervoltage lockout circuit to insure sufficient input supply voltage is present before any switching activity can occur, and a pulse-by-pulse current limit. Output current can be sensed and limited to a user determined maximum value. The UVLO circuit turns the chip off when the input voltage is below the UVLO threshold. In addition, a sleep comparator interfaces to the UVLO circuit to turn the chip off. This reduces the supply current to only 50 $\mu$ A, making the UC3572 ideal for battery powered applications.

## BLOCK DIAGRAM



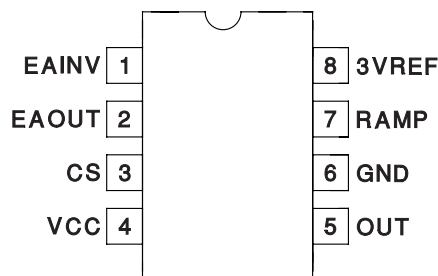
## ABSOLUTE MAXIMUM RATINGS

VCC	35V
EAINV	-0.6V to VCC
IEAOUT	25mA
RAMP	-0.3V to 4V
CS	-0.3V to VCC
Iout	-0.7A to 0.7A
I3VREF	-15mA
Storage Temperature	-65°C to +150°C
Junction Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

## CONNECTION DIAGRAM

DIL-8, SOIC-8 (TOP VIEW)  
D, N or J Packages



## ORDERING INFORMATION

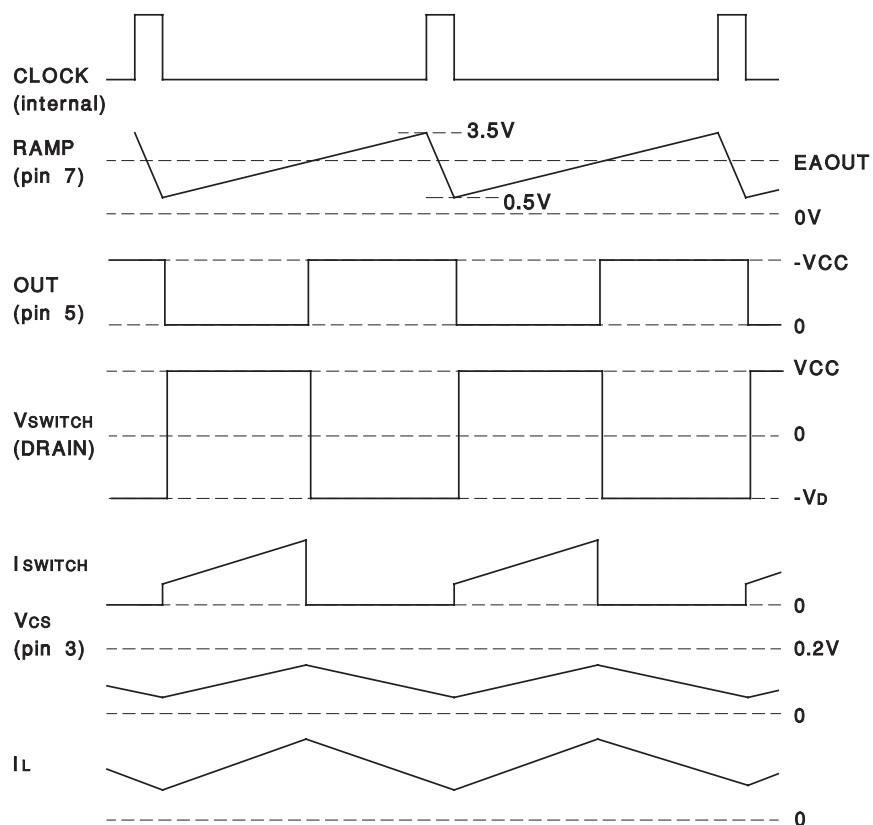
	TEMPERATURE RANGE	PACKAGE
UC1572	-55°C to +125°C	J
UC2572	-40°C to +85°C	D, N or J
UC3572	0°C to +70°C	D or N

**ELECTRICAL CHARACTERISTICS:** Unless otherwise specified, VCC = 5V, CT = 680pF, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Reference Section</b>					
3VREF		2.94	3	3.06	V
Line Regulation	VCC = 4.75 to 30V		1	10	mV
Load Regulation	I3VREF = 0V to -5mA		1	10	mV
<b>Oscillator Section</b>					
Frequency	VCC = 5V to 30V	85	100	115	kHz
<b>Error Amp Section</b>					
EAINV	EAOUT = 2V	-10	0	10	mV
	IEANV = -1mA		-0.2	-0.9	V
IEAINV	EAOUT = 2V		-0.2	-1.0	μA
AVOL	EAOUT = 0.5V to 3V	65	90		dB
EAOUT High	EAINV = -100mV	3.6	4	4.4	V
EAOUT Low	EAINV = 100mV		0.1	0.2	V
IEAOUT	EAINV = -100mV, EAOUT = 2V	-350	-500		μA
	EAINV = 100mV, EAOUT = 2V	7	20		mA
Unity Gain Bandwidth	TJ = 25°C, F = 10kHz	0.6	1		MHz
<b>Current Sense Comparator Section</b>					
Threshold		0.195	0.215	0.235	V
Input Bias Current	CS = 0		-0.4	-1	μA
CS Propagation Delay			300		nS
<b>Gate Drive Output Section</b>					
OUT High Saturation	IOUT = 0		0	0.3	V
	IOUT = -10mA		0.7	1.5	V
	IOUT = -100mA		1.5	2.5	V
OUT Low Saturation	IOUT = 10mA		0.1	0.4	V
	IOUT = 100mA		1.5	2.2	V
Rise Time	TJ = 25°C, CLOAD = 1nF + 3.3 Ohms		30	80	nS

**ELECTRICAL CHARACTERISTICS:** Unless otherwise specified, VCC = 5V, CT = 680pF, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Fall Time	TJ = 25°C, CLOAD = 1nF + 3.3 Ohms		30	80	nS
<b>Pulse Width Modulator Section</b>					
Maximum Duty Cycle	EAINV = +100mV, VCC = 5V to 30V		92	96	%
Minimum Duty Cycle	EAINV = -100mV, VCC = 5V to 30V			0	%
Modulator Gain	EAOUT = 1.5V to 2.5V	45	55	65	%/V
<b>Undervoltage Lockout Section</b>					
Start Threshold		3.5	4.2	4.5	V
Hysteresis		100	200	300	mV
<b>Sleep Mode Section</b>					
Threshold		1.8	2.2	2.6	V
<b>Supply Current Section</b>					
IVCC	VCC = 5V, 30V		9	12	mA
	VCC = 30, CS = 3V		50	150	μA



UDG-94095

**Figure 1. Typical waveforms.**

## PIN DESCRIPTIONS

**3VREF:** Precision 3V reference. Bypass with 100nF capacitor to GND.

**CS:** Current limit sense pin. Connect to a ground referenced current sense resistor in series with the flyback inductor. OUT will be held high (PMOS switch off) if CS exceeds 0.2V.

**EAINV:** Inverting input to error amplifier. Summing junction for 3VREF and VOUT sense. The non-inverting input of the error amplifier is internally connected to GND. This pin will source a maximum of 1mA.

**EAOUT:** Output of error amplifier. Use EAOUT and EAINV for loop compensation components.

**GND:** Circuit Ground.

**OUT:** Gate drive for external PMOS switch connected between VCC and the flyback inductor. OUT drives the gate of the PMOS switch between VCC and GND.

**RAMP:** Oscillator and ramp for pulse width modulator. Frequency is set by a capacitor to GND by the equation

$$F = \frac{1}{15k \cdot C_{RAMP}}$$

Recommended operating frequency range is 10kHz to 200kHz.

**VCC:** Input voltage supply to chip. Range is 4.75 to 30V. Bypass with a 1μF capacitor.

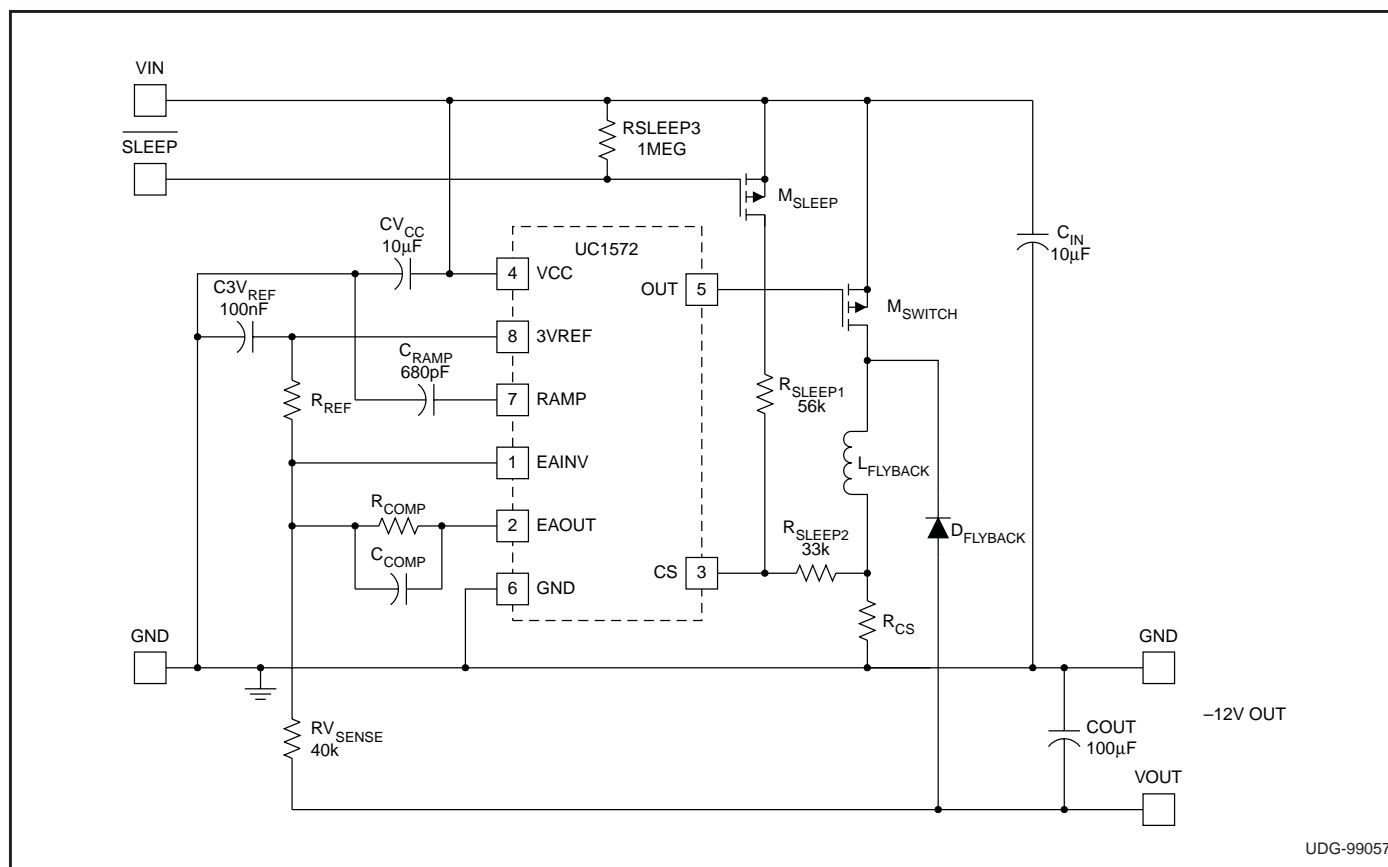


Figure 2. Typical application: +5V to -12V flyback converter.

## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.