

# Buck Pulse Width Modulator Stepdown Voltage Regulator

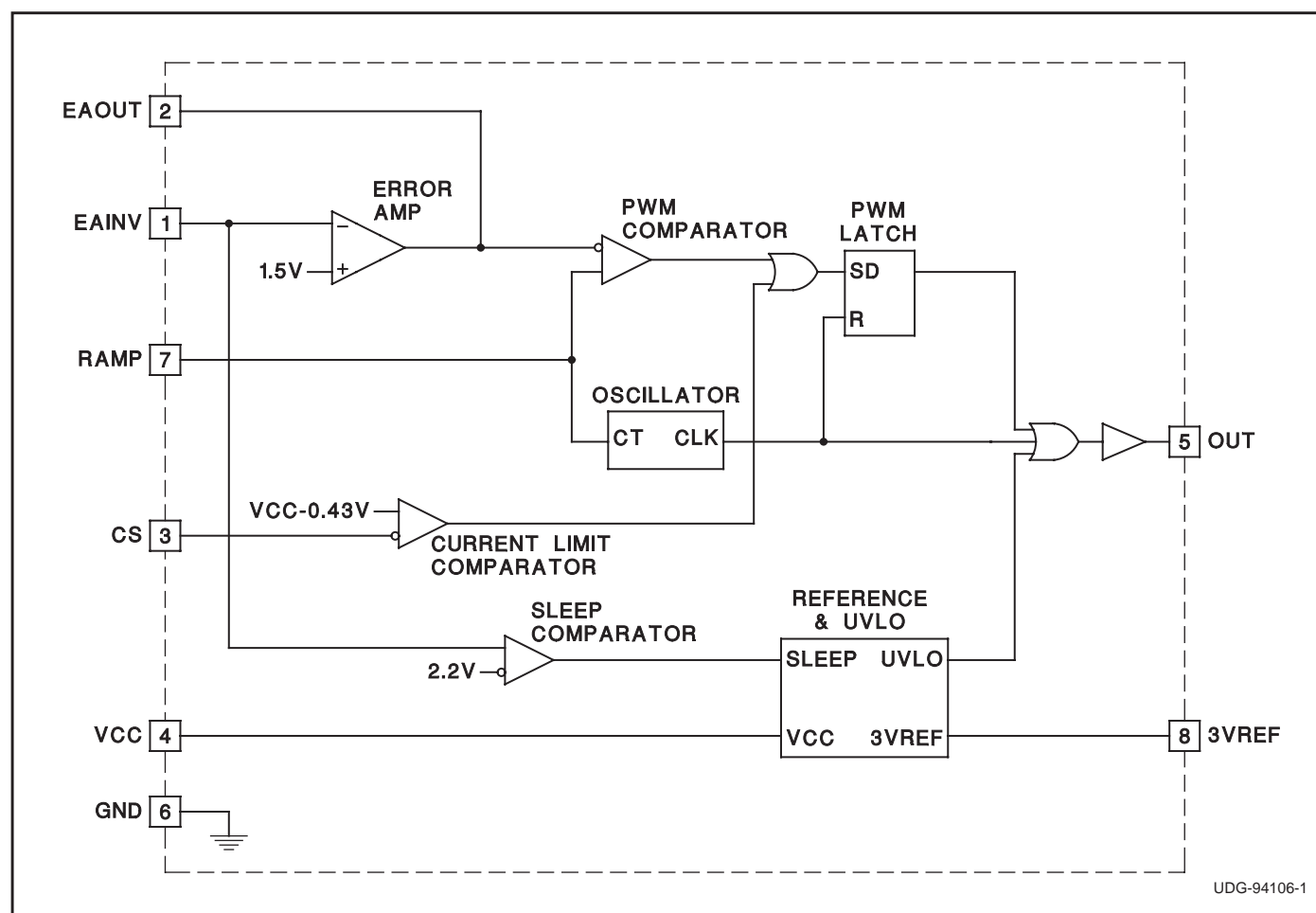
## FEATURES

- Simple Single Inductor Buck PWM Stepdown Voltage Regulation
- Drives External PMOS Switch
- Contains UVLO Circuit
- Includes Pulse-by-Pulse Current Limit
- Low 50 $\mu$ A Sleep Mode Current

## DESCRIPTION

The UC3573 is a Buck pulse width modulator which steps down and regulates a positive input voltage. The chip is optimized for use in a single inductor buck switching converter employing an external PMOS switch. The block diagram consists of a precision reference, an error amplifier configured for voltage mode operation, an oscillator, a PWM comparator with latching logic, and a 0.5A peak gate driver. The UC3573 includes an undervoltage lockout circuit to insure sufficient input supply voltage is present before any switching activity can occur, and a pulse-by-pulse current limit. Input current can be sensed and limited to a user determined maximum value. In addition, a sleep comparator interfaces to the UVLO circuit which turns the chip off when the input voltage is below the UVLO threshold. This reduces the supply current to only 50 $\mu$ A, making the UC3573 ideal for battery powered applications.

## BLOCK DIAGRAM



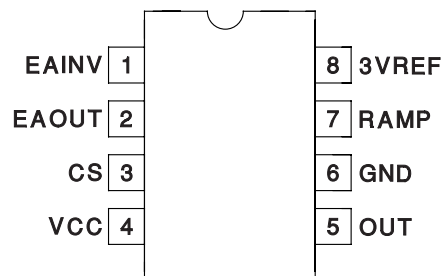
## ABSOLUTE MAXIMUM RATINGS

VCC	35V
EAINV	−0.6V to VCC
I <sub>EAOUT</sub>	25mA
RAMP	−0.3V to 4V
CS	−0.3V to VCC
I <sub>OUT</sub>	−0.7A to 0.7A
I <sub>3VREF</sub>	−15mA
Storage Temperature	−65°C to +150°C
Junction Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

## CONNECTION DIAGRAMS

**DIL-8, SOIC-8 (TOP VIEW)  
J or N, D Packages**



**ELECTRICAL CHARACTERISTICS:** Unless otherwise specified, these parameters apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for the UC1573,  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  for the UC2573, and  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC3573,  $V_{CC} = 5\text{V}$ ,  $C_T = 680\text{pF}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Reference Section</b>					
3VREF		2.94	3	3.06	V
Line Regulation	$V_{CC} = 4.75$ to $30\text{V}$		1	10	mV
Load Regulation	$I_{3VREF} = 0$ to $-5\text{mA}$		1	10	mV
<b>Oscillator Section</b>					
Frequency	$V_{CC} = 5\text{V}$ , $30\text{V}$	85	100	115	kHz
<b>Error Amp Section</b>					
EAINV	EAOUT = $2\text{V}$	1.45	1.5	1.55	V
I <sub>EAINV</sub>	EAOUT = $2\text{V}$		−0.2	−1	μA
AVOL	EAOUT = $0.5\text{V}$ to $3\text{V}$	65	90		dB
EAOUT High	EAINV = $1.4\text{V}$	3.6	4	4.4	V
EAOUT Low	EAINV = $1.6\text{V}$		0.1	0.2	V
I <sub>EAOUT</sub>	EAINV = $1.4\text{V}$ , EAOUT = $2\text{V}$	−350	−500		μA
	EAINV = $1.6\text{V}$ , EAOUT = $2\text{V}$	7	20		mA
Unity Gain Bandwidth	$T_J = 25^\circ\text{C}$ , $F = 10\text{kHz}$	0.6	1		MHz
<b>Current Sense Comparator Section</b>					
Threshold (referred to VCC)		−0.39	−0.43	−0.47	V
Input Bias Current	CS = VCC		150	800	nA
CS Propagation Delay			400		ns
<b>Gate Drive Output Section</b>					
OUT High Saturation	I <sub>OUT</sub> = 0		0	0.3	V
	I <sub>OUT</sub> = $-10\text{mA}$		0.7	1.5	V
	I <sub>OUT</sub> = $-100\text{mA}$		1.5	2.5	V
OUT Low Saturation	I <sub>OUT</sub> = $10\text{mA}$		0.1	0.4	V
	I <sub>OUT</sub> = $100\text{mA}$		1.5	2.2	V
Rise Time	$T_J = 25^\circ\text{C}$ , $C_{LOAD} = 1\text{nF} + 3.3\text{ Ohms}$		30	80	ns
Fall Time	$T_J = 25^\circ\text{C}$ , $C_{LOAD} = 1\text{nF} + 3.3\text{ Ohms}$		30	80	ns
<b>Pulse Width Modulator Section</b>					
Maximum Duty Cycle	EAINV = $1.4\text{V}$		92	96	%
Minimum Duty Cycle	EAINV = $1.6\text{V}$			0	%
Modulator Gain	EAOUT = $1.5\text{V}$ to $2.5\text{V}$	25	35	45	%/V
<b>Undervoltage Lockout Section</b>					
Start Threshold		3.5	4.2	4.5	V
Hysteresis		100	200	300	mV

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Sleep Mode Section</b>					
Threshold		1.8	2.2	2.6	V
<b>Supply Current Section</b>					
$I_{VCC}$	$V_{CC} = 30\text{V}$		9	12	mA
$I_{VCC}$	$V_{CC} = 30\text{V}$ , $EAINV = 3\text{V}$		50	150	$\mu\text{A}$

## PIN DESCRIPTIONS

**3VREF:** Precision 3V reference. Bypass with 100nF capacitor.

**CS:** Peak current limit sense pin. Senses the current across a current sense resistor placed between  $V_{CC}$  and source of the PMOS Buck switch. OUT will be held high (PMOS buck switch off) if  $V_{CC} - CS$  exceeds 0.4V.

**EAINV:** Inverting input to error amplifier. VOUT sense feedback connected to this pin. The non-inverting input of the error amplifier is internally connected to:

$$\frac{3V_{REF}}{2} \text{ Volts.}$$

Connecting the EAINV pin to an external voltage greater than 2.6V commands the chip to go into a low current sleep mode.

**EAOUT:** Output of error amplifier. Use EAOUT and EAINV for loop compensation components.

**GND:** Circuit Ground.

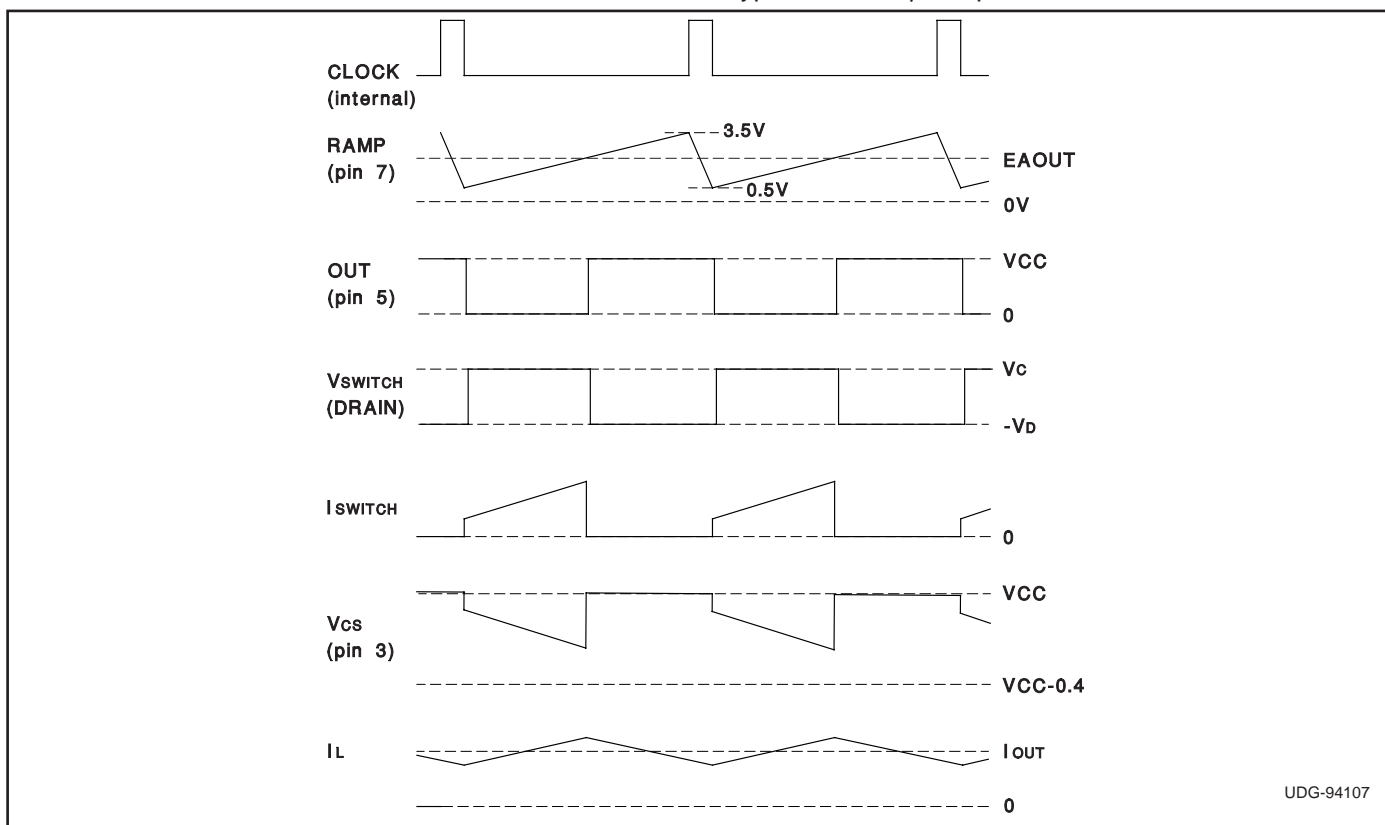
**OUT:** Gate drive for external PMOS switch connected between  $V_{CC}$  and the flyback inductor. OUT drives the gate of the PMOS switch between  $V_{CC}$  and GND.

**RAMP:** Oscillator and ramp for pulse width modulator. Frequency is set by a capacitor to GND by the equation

$$F = \frac{1}{15k \cdot C_{RAMP}}$$

Recommended operating frequency range is 10kHz to 200kHz.

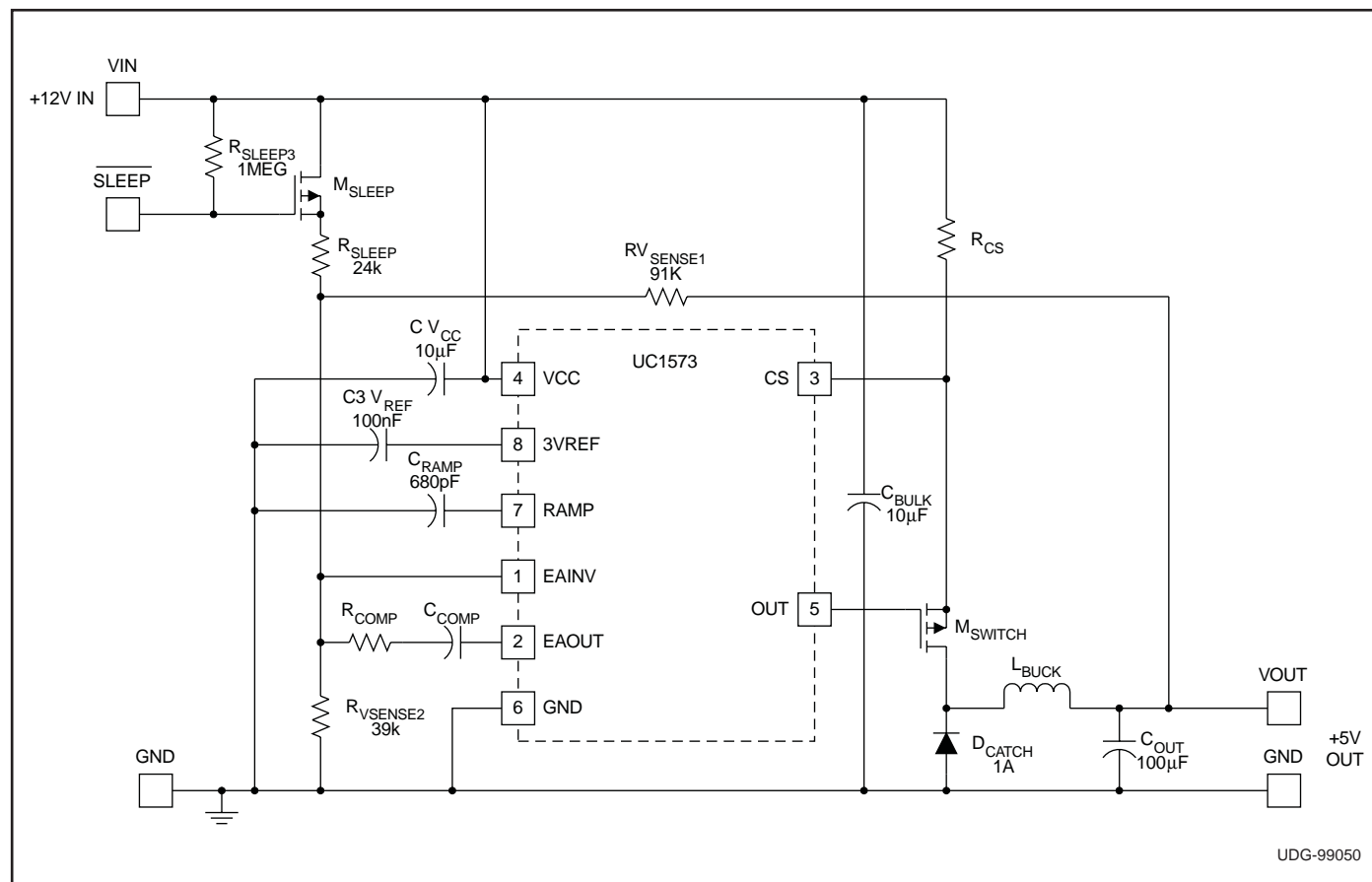
**VCC:** Input voltage supply to chip. Range is 4.75V to 30V. Bypass with a 1 $\mu\text{F}$  capacitor.



UDG-94107

**Typical Waveforms.**

# TYPICAL APPLICATION: 12V TO 5V BUCK CONVERTER



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