

UC1846, UC1847, UC2846 UC2847, UC3846, UC3847 CURRENT-MODE PWM CONTROLLERS

D3045, APRIL 1988—REVISED OCTOBER 1988

- Automatic Feed-Forward Compensation
- Programmable Pulse-by-Pulse Current Limiting
- Automatic Symmetry Correction in Push-Pull Configuration
- Enhanced Load Response Characteristics
- Parallel Operation Capability for Modular Power Systems
- Differential Current-Sense Amplifier with Wide Common-Mode Range
- Double-Pulse Suppression
- 200-mA Totem-Pole Outputs
- $\pm 1\%$ Bandgap Reference
- Under-Voltage Lockout
- Soft-Start Capability
- Shutdown Terminal
- 500-kHz Operation

description

This family of control ICs provides all of the necessary features to implement fixed frequency, current-mode control schemes while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier-to-design control loop. Topological advantages include inherent pulse-by-pulse current-limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel "power modules" while maintaining equal current sharing.

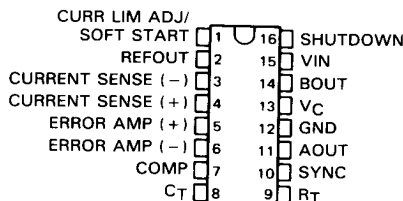
Protection circuitry includes built-in under-voltage lockout and programmable current limiting in addition to soft-start capability. A shutdown function is also available that can initiate either a complete shutdown with automatic restart, or latch the supply off.

Other features include fully-latched operation, double-pulse suppression, deadtime adjustment capability, and a $\pm 1\%$ trimmed bandgap reference.

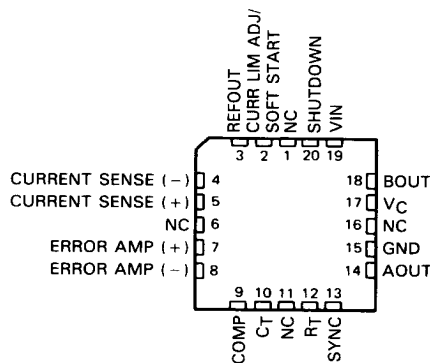
In the off state, the UC1846 outputs are low and the UC1847 outputs are high.

The UC1846 and UC1847 are characterized for operation over the full military temperature range of -55°C to 125°C , the UC2846 and UC2847 are characterized for operation from -25°C to 85°C , and the UC3846 and UC3847 are characterized for operation from 0°C to 70°C .

UC1846, UC1847 . . . J PACKAGE
UC2846, UC2847, UC3846, UC3847 . . . N PACKAGE
(TOP VIEW)



UC2846, UC2847, UC3846, UC3847 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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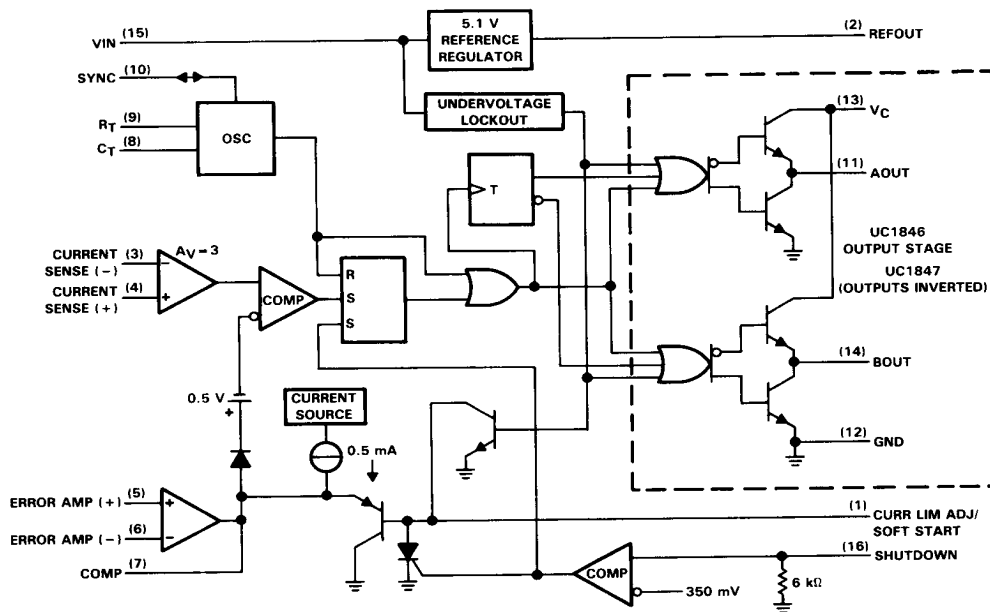
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CURRENT-MODE PWM CONTROLLERS

functional block diagram

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Data Sheets



**UC1846, UC1847, UC2846
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CURRENT-MODE PWM CONTROLLERS**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{IN} (see Note 1)	40 V
Collector supply voltage, V_C	40 V
Output current, source or sink, I_O	500 mA
Analog input voltage (CURRENT SENSE (-), CURRENT SENSE (+), ERROR AMP (+), ERROR AMP (-), or SHUTDOWN)	-0.3 V to V_{IN}
Reference output current	-30 mA
SYNC output current	-5 mA
Error amplifier output current	-5 mA
Soft-start sink current	50 mA
Oscillator charging current	5 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range: UC1846, UC1847	-55°C to 125°C
UC2846, UC2847	-25°C to 85°C
UC3846, UC3847	0°C to 70°C
Storage temperature range	-65°C to 150°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$	$T_A = 85^\circ\text{C}$	$T_A = 125^\circ\text{C}$
	POWER RATING		POWER RATING	POWER RATING	POWER RATING
FN	1400 mW	11.2 mW/°C	896 mW	728 mW	280 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	

**UC1846, UC1847, UC2846
UC2847, UC3846, UC3847
CURRENT-MODE PWM CONTROLLERS**

recommended operating conditions

	UC1846, UC1847		UC2846, UC2847		UC3846, UC3847		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
High-level input voltage, V_{IH} (Oscillator Section)	3.9		3.9		3.9		V
Low-level input voltage, V_{IL} (Oscillator Section)		2.5		2.5		2.5	V
Supply voltage operating range, V_{IN}	8	40	8	40	8	40	V
Operating free-air temperature, T_A	-55	125	-25	85	0	70	°C

electrical characteristics over operating free-air temperature range, $V_{IN} = 15$ V, $R_T = 10$ k Ω , $C_T = 4.7$ nF (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS	UC1846, UC1847 UC2846, UC2847			UC3846, UC3847			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_O Output voltage	$I_O = 1$ mA, $T_A = 25^\circ\text{C}$	5.05	5.1	5.1	5	5.1	5.2	V
Line regulation	$V_{IN}(\text{pin } 15) = 8$ V to 40 V		5	20		5	20	mV
Load regulation	$I_{IL} = 1$ mA to 10 mA		3	15		3	15	mV
α_{VO} Temperature coefficient of output voltage			0.4			0.4		mV/°C
Total output variation		5		5.2	4.95		5.25	V
Output noise voltage	$f = 1$ kHz to 10 kHz, $T_A = 25^\circ\text{C}$			100			100	μV
Output voltage long-term drift	$t = 1000$ hours, $T_A = 25^\circ\text{C}$		5			5		mV
I_{OS} Short-circuit output current (REFOUT)	$V_{REF} = 0$	-10	-45		-10	-45		mA

oscillator section

PARAMETER	TEST CONDITIONS	UC1846, UC1847 UC2846, UC2847			UC3846, UC3847			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Initial accuracy	$T_A = 25^\circ\text{C}$	39	43	47	39	43	47	kHz
Frequency change with voltage	$V_{IN}(\text{pin } 15) = 8$ V to 40 V		-1%	$\pm 2\%$		-1%	$\pm 2\%$	
Frequency change with temperature			-1%			-1%		
V_T Threshold voltage (SYNC)		2.5		3.9	2.5		3.9	V
V_{OH} High-level output voltage (SYNC)		3.9			3.9			V
V_{OL} Low-level output voltage (SYNC)				2.5			2.5	V
I_i Input current (SYNC)	Sync voltage = 5.25 V, C_T at 0 V		1.3	1.5		1.3	1.5	mA

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electrical characteristics over operating free-air temperature range, $V_{IN} = 15\text{ V}$, $R_T = 10\text{ k}\Omega$, $C_T = 4.7\text{ nF}$ (unless otherwise noted) (continued)

error amplifier section

PARAMETER	TEST CONDITIONS	UC1846, UC1847 UC2846, UC2847			UC3846, UC3847			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage			0.5	5		0.5	5	mV
I_{IO} Input offset current			40	250		40	250	nA
I_{IB} Input bias current			-0.6	-1		-0.6	-1	μA
V_{OH} High-level output voltage	$R_L(\text{COMP}) = 15\text{ k}\Omega$	4.3	4.6		4.3	4.6		V
I_{OH} High-level output current	$V_{ID} = 15\text{ mV to } 5\text{ V}$, COMP at 2.5 V	-0.4	-0.5		-0.4	-0.5		mA
V_{OL} Low-level output voltage	$R_L(\text{COMP}) = 15\text{ k}\Omega$		0.7	1		0.7	1	V
I_{OL} Low-level output current	$V_{ID} = -15\text{ mV to } -5\text{ V}$, COMP at 1.2 V	2	6		2	6		mA
V_{ICR} Common-mode input voltage range	$V_{IN} = 8\text{ V to } 40\text{ V}$	0 to $V_{IN}-2$			0 to $V_{IN}-2$			V
A_{VD} Open-loop voltage amplification	$\Delta V_O = 1.2\text{ V to } 3\text{ V}$, $V_{IC} = 2\text{ V}$	80	105		80	105		dB
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to } 38\text{ V}$, $V_{IN} = 40\text{ V}$	75	100		75	100		dB
kSVR Supply-voltage rejection ratio	$V_{IN} = 8\text{ V to } 40\text{ V}$	80	105		80	105		dB

current-sense amplifier section

PARAMETER	TEST CONDITIONS	UC1846, UC1847 UC2846, UC2847			UC3846, UC3847			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	CURR LIM ADJ/SOFT START at 0.5 V, COMP open, See Note 3		5	25		5	25	mV
I_{IO} Input offset current			0.08	1		0.08	1	μA
I_{IB} Input bias current			-2.5	-10		-2.5	-10	μA
A_V Voltage amplification	CURRENT SENSE (-) at 0 V, CURR LIM ADJ/SOFT START open, See Notes 2 and 3	2.5	2.75	3	2.5	2.75	3	V
V_{ICR} Common-mode input voltage range		0 to $V_{IN}-3$			0 to $V_{IN}-3$			V
Maximum usable differential input signal	CURR LIM ADJ/SOFT START open, $R_L(\text{COMP}) = 15\text{ k}\Omega$, See Note 2	1.1	1.3		1.1	1.2		V
CMRR Common-mode rejection ratio	$V_{IC} = 1\text{ V to } 12\text{ V}$	60	83		60	83		dB
kSVR Supply-voltage rejection ratio	$V_{IN} = 8\text{ V to } 40\text{ V}$	60	84		60	84		dB
t_d Input-to-output delay time	$T_A = 25^\circ\text{C}$		200	600		200	600	ns

NOTES: 2. This parameter is measured at the trip point of the latch with ERROR AMP (+) at V_{REF} , ERROR AMP (-) at 0 V.
3. Amplifier gain is defined as:

$$A_V = \frac{\Delta V_{PIN\ 7}}{\Delta V_{PIN\ 4}}$$

Where:

$$\Delta V_{PIN\ 4} = 0\text{ V to } 1.0\text{ V}$$

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electrical characteristics over operating free-air temperature range, $V_{IN} = 15\text{ V}$, $R_T = 10\text{ k}\Omega$, $C_T = 4.7\text{ nF}$ (unless otherwise noted) (continued)

current limit adjustment section

PARAMETER	TEST CONDITIONS	UC1846, UC1847 UC2846, UC2847			UC3846, UC3847			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	CURRENT SENSE (–) at 0 V, CURRENT SENSE (+) at 0 V, COMP open, See Note 3	0.45	0.5	0.55	0.45	0.5	0.55	V
I_{IB} Input bias current	ERROR AMP (+) at V_{REF} , ERROR AMP (–) at 0 V		–10	–30		–10	–30	μA

shutdown terminal section

PARAMETER	TEST CONDITIONS	UC1846, UC1847 UC2846, UC2847			UC3846, UC3847			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_T Differential-input threshold voltage		250	350	400	250	350	400	mV
V_I Input voltage range		0 to V_{IN}			0 to V_{IN}			V
Minimum latching current (CURR LIM ADJ/SOFT START)	See Note 4	0.8	1.5	3	0.8	1.5	3	mA
Output delay	$T_A = 25^\circ\text{C}$		300	600		300	600	ns

output section

PARAMETER	TEST CONDITIONS	UC1846, UC1847 UC2846, UC2847			UC3846, UC3847			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)CE}$ Collector-emitter breakdown voltage		40			40			V
I_{CEX} Collector-emitter off-state current	$V_{CE} = 40\text{ V}$, See Note 5			200			200	μA
V_{OH} High-level output voltage (AOUT and BOUT)	$I_{OH} = -20\text{ mA}$	13	13.5		13	13.5		V
	$I_{OH} = -100\text{ mA}$	12	13.5		12	13.5		
V_{OL} Low-level output voltage (AOUT and BOUT)	$I_{OL} = 20\text{ mA}$		0.1	0.4		0.1	0.4	V
	$I_{OL} = 100\text{ mA}$		0.4	2.1		0.4	2.1	
t_r Rise time (AOUT and BOUT)	$C_L = 1\text{ nF}$, $T_A = 25^\circ\text{C}$		50	300		50	300	ns
t_f Fall time (AOUT and BOUT)			50	300		50	300	ns

under-voltage lockout section

PARAMETER	TEST CONDITIONS	UC1846, UC1847 UC2846, UC2847			UC3846, UC3847			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Startup threshold			7.7	8		7.7	8	V
Threshold hysteresis			0.75			0.75		V

- NOTES: 3. This parameter is measured at the trip point of the latch with ERROR AMP (+) at V_{REF} and ERROR AMP (–) at 0 V.
4. This is the lowest current into Pin 1 that will latch the circuit in the shutdown state.
5. This applies for UC1846, UC2846, and UC3846 only (due to polarity of outputs).

UC1846, UC1847, UC2846
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electrical characteristics over operating free-air temperature range, $V_{IN} = 15\text{ V}$, $R_T = 10\text{ k}\Omega$,
 $C_T = 4.7\text{ nF}$ (unless otherwise noted) (continued)
total device

PARAMETER	TEST CONDITIONS	UC1846, UC1847 UC2846, UC2847			UC3846, UC3847			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply current			17	21		17	21	mA

TYPICAL CHARACTERISTICS

ERROR AMPLIFIER AMPLIFICATION AND PHASE
VS
FREQUENCY

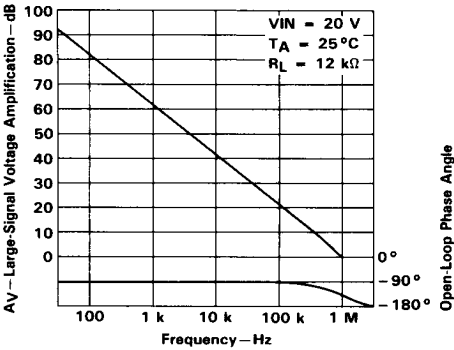


FIGURE 1

ERROR AMPLIFIER LARGE-SIGNAL DC AMPLIFICATION
VS
LOAD RESISTANCE

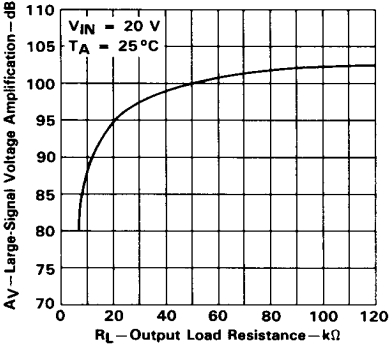


FIGURE 2



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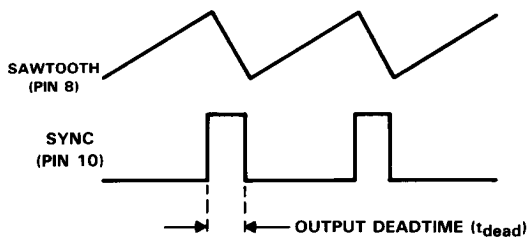
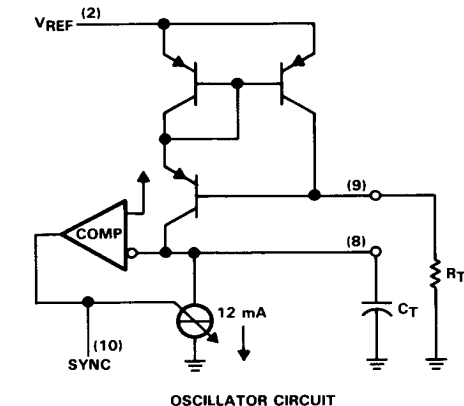
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TYPICAL APPLICATION DATA

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OSCILLATOR WAVEFORMS

NOTE: Oscillator frequency is approximated by the formula: $f_T = \frac{2.2}{R_T C_T}$

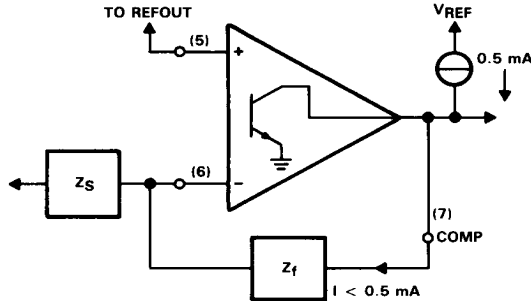
Output deadtime is determined by the size of the external capacitor, C_T , according to the following formula:

$$t_{dead} = 145 C_T \left(\frac{12}{12 - \frac{3.6}{R_T (k\Omega)}} \right)$$

For large values of R_T , $t_{dead} \approx 145 C_T$

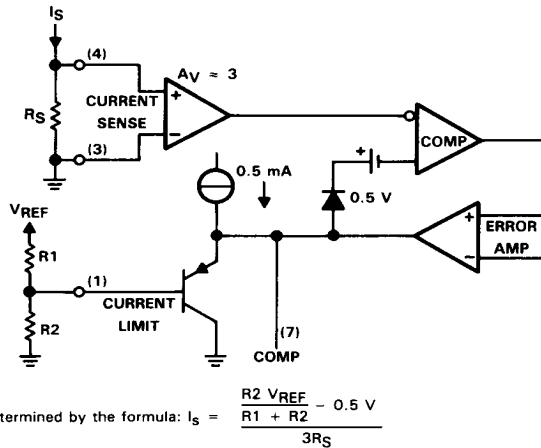
FIGURE 3. OSCILLATOR CIRCUIT

TYPICAL APPLICATION DATA



NOTE: Error Amplifier can source up to 0.5 mA.

FIGURE 4. ERROR AMPLIFIER OUTPUT CONFIGURATION



NOTE: Peak Current (I_s) is determined by the formula: $I_s = \frac{R_2 V_{REF} - 0.5 V}{3R_s}$

FIGURE 5. PULSE-BY-PULSE CURRENT LIMITING

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The schematic diagram illustrates the current limit and shutdown circuitry. It is divided into two main sections by a vertical dashed line.

Current Limit Section:

- A current source I_{SOURCE} is connected to a diode.
- The diode's cathode is connected to a node labeled "CURRENT LIMIT".
- The diode's anode is connected to a 0.5 V reference voltage.
- A comparator (COMP) is connected to the "CURRENT LIMIT" node and the 0.5 V reference. Its output is labeled "E/A".
- The "CURRENT LIMIT" node is also connected to a node labeled (1).

Shutdown Section:

- A shutdown pin (16) is connected to a node labeled "SHUTDOWN".
- The "SHUTDOWN" node is connected to a 350 mV reference voltage.
- A comparator (COMP) is connected to the "SHUTDOWN" node and the 350 mV reference. Its output is connected to a node labeled "S".

Other Components:

- A reference voltage V_{REF} is connected to a resistor $R1$ and a capacitor C .
- The other end of $R1$ is connected to a node labeled I_{SS} .
- The other end of C is connected to a node labeled $R2$.
- The other end of $R2$ is connected to a node labeled (1).

The timing diagram illustrates the behavior of the MAX4223E under two different load conditions. The signals shown are:

- CURRENT LIMIT (PIN 1):** The current limit voltage. It is 0V when the device is in shutdown. When the device is turned on, it ramps up to a peak value and then settles at a steady-state value. A dashed line indicates a 0.5V reference level.
- SHUTDOWN (PIN 16):** The shutdown control signal. It is ON (high) when the device is operating and OFF (low) when the device is in shutdown. A pulse to ON turns the device on, and a pulse to OFF turns it off.
- PWM:** The pulse-width modulation signal. It is a square wave that controls the output current.

The diagram is divided into two sections based on the load current:

- Left Section:** $\frac{V_{REF}}{R1} < 0.8 \text{ mA}$. In this case, the current limit voltage (PIN 1) ramps up to a peak and then settles at a steady-state value that is above the 0.5V reference line.
- Right Section:** $\frac{V_{REF}}{R1} > 3 \text{ mA (LATCHED OFF)}$. In this case, the current limit voltage (PIN 1) ramps up to a peak and then settles at a steady-state value that is below the 0.5V reference line, indicating the device has latched off.

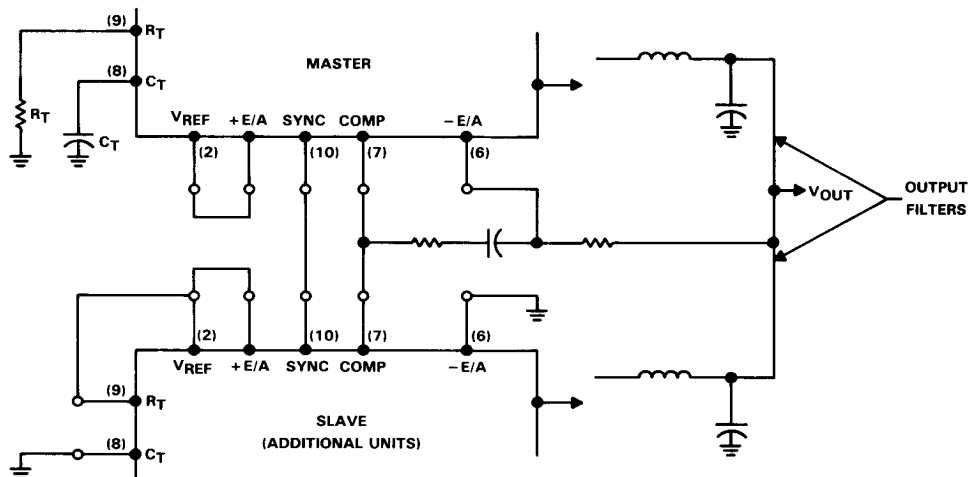
NOTE: If $\frac{V_{REF}}{R1} > 3 \text{ mA}$, the device will latch off until power is cycled.

SHUTDOWN WITHOUT AUTO-RESTART (LATCHED)

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TYPICAL APPLICATION DATA



NOTE: Slaving allows parallel operation of two or more units with equal current sharing.

FIGURE 7. PARALLEL OPERATION