INTEGRATED CIRCUITS

UNITRODE

UC1861/64/65
UC2861/64/65
UC3861/64/65

Resonant-Mode Power Supply Controllers

PRELIMINARY

FEATURES

- Controls Zero Current Switched (ZCS) or Zero Voltage Switched (ZVS) quasi-resonant converters
- Zero-crossing terminated one-shot timer
- Precision 1%, soft-started 5V reference
- Programmable restart delay following fault
- Voltage-Controlled Oscillator (VCO) with programmable minimum and maximum frequencies from 10 kHz to 1 MHz
- Low start-up current (150 µA typ.)
- Dual 1 Amp peak FET drivers
- UVLO option for off-line or DC/DC applications

Device	UVLO	Outputs	'Fixed'
1861	16/10	Alternating	Off Time
1864	9/7	Parallel	On Time
1865	16/10	Alternating	Off Time

Other variations of this series can be

DESCRIPTION

The UC1861/64/65 family of ICs is optimized for the control of Zero Current Switched and Zero Voltage Switched quasi-resonant converters. Differences between members of this device family result from the various combinations of UVLO thresholds and output options. Additionally, the one-shot pulse steering logic is configured to program either on-time for ZCS systems (UC1865), or off-time for ZVS applications (UC1861/64).

The primary control blocks implemented include an error amplifier to compensate the overall system loop and to drive a voltage controlled oscillator (VCO), featuring programmable minimum and maximum frequencies. Triggered by the VCO, the one-shot generates pulses of a programmed maximum width, which can be modulated by the Zero Detection comparator. This circuit facilitates "true" zero current or voltage switching over various line, load, and temperature changes, and is also able to accommodate the resonant components' initial tolerances.

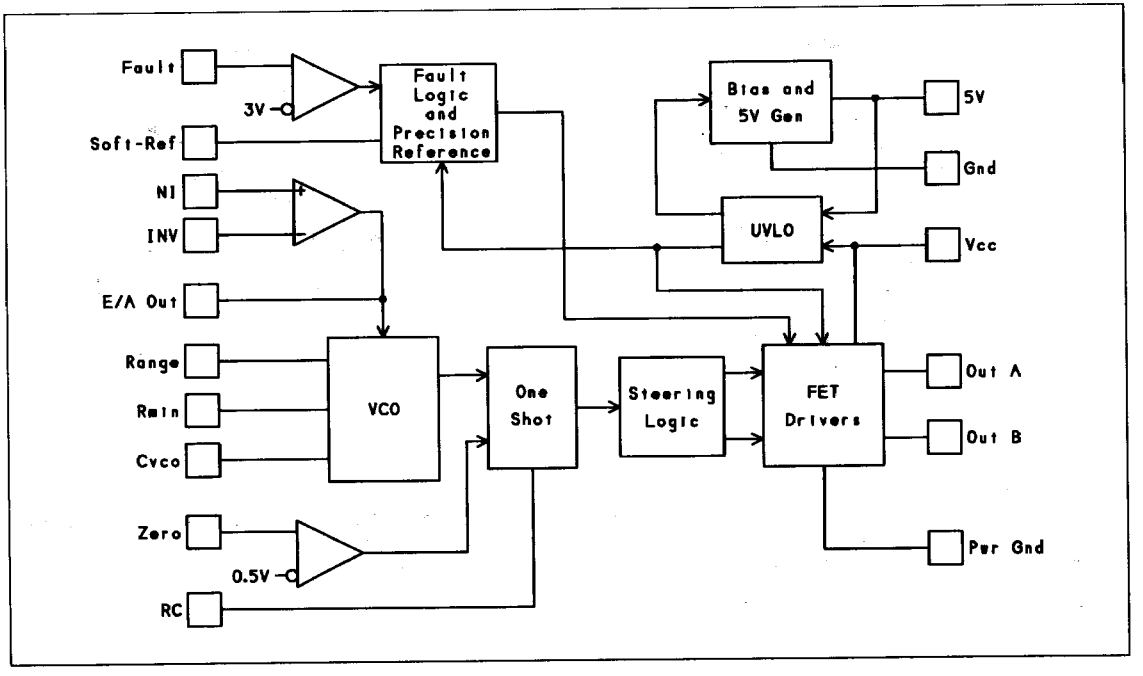
Under-Voltage Lockout is incorporated to facilitate safe starts upon power-up. The supply current during the under-voltage lockout period is typically less than 150 uA, and the outputs are actively forced to the low state. UVLO thresholds for the UC1861 and UC 1865 are 16V (ON) and 10V (OFF), whereas the UC1864 thresholds are 8V (ON) and 7V (OFF). After Vcc exceeds the UVLO threshold, a 5V generator is enabled which provides bias for the internal circuits and up to 10mA for external usage.

A Fault comparator serves to detect fault conditions and set a latch while forcing the output drivers low. The Soft-Ref pin serves three functions: providing soft start, restart delay, and the internal system reference.

Each device features dual 1 Amp peak totem pole output drivers for direct interface to power MOSFETS. The outputs are programmed to alternate in the UC1861/65 devices. The UC1864 outputs operate in unison alllowing 2 Amp peak current.

Options other than the three outlined in this data sheet can be obtained from this family of control IC's. Consult the factory for further information.

BLOCK DIAGRAM



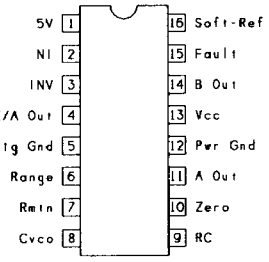
ABSOLUTE MAXIMUM RATINGS

Vcc 22V
Output Current, Source or Sink (Pins 11 & 14) DC 0.5A
Pulse (0.5μs) 1.5A
Power Ground Volage . . . . . ±0.2V
Inputs (Pins 2, 3, 10, & 13) . . . . . –0.4 to 7V
Error Amp Output Current . . . . . ±2mA
Power Dissipation at $T_A \leq 50^oC$ (N & Q package) 1W
Derate 10mW/^{o}C for $T_A > 50^oC$
Power Dissipation at $T_A \leq 70^oC$ (J package) 1W
Derate 12.5mW/^{o}C for $T_A > 70^oC$
Power Dissipation at $T_A \leq 80^oC$ (L package) 1W
Derate 14.3mW/^{o}C for $T_A > 80^oC$.
Junction Temperature (Operating) . . . . . 150^{o}C
Lead Temperature (Soldering, 10 seconds) . . . . . 300^{o}C

Note: All voltages are with respect to signal ground and all currents are positive into the specified terminal. Pin numbers refer to the J and N packages.

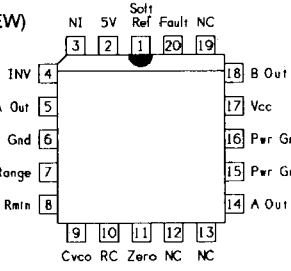
CONNNECTION DIAGRAM

J or N PACKAGE (TOP VIEW)



Q or L PACKAGE

(TOP VIEW)



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ELECTRICAL CHARACTERISTICS

Unless otherwise stated, all specifications apply for $-55^oC \leq T_A \leq 125^oC$ for the UC18xx, $-25^oC \leq T_A \leq 85^oC$ for the UC28xx, and $0^oC \leq T_A \leq 70^oC$ for the UC38xx, VCC=12V, Cvco=1nF, Range=7.5K, Rmin=91K, C=200pF, R=4.3K, and Csr=0.1μF. $T_A = T_j$

PARAMETER	TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNITS
5 VOLT GENERATOR					
Output Voltage	12V≤Vcc≤20V, –10mA≤Io≤0mA	4.8	5.0	5.2	V
Short Circuit Current	Vo=0V	–150		–15	mA
SOFT-REFERENCE					
Restart Delay Current	V=2V	10	20	35	μA
Soft Start Current	V=2V	–650	–500	–350	μA
Reference Voltage	T_J=25°C, Io=0	4.95	5.00	5.05	V
Reference Voltage	12V≤Vcc≤20V, –200μA≤Io≤200μA	4.85		5.15	V
Line Regulation	12V≤Vcc≤20V		2	20	mV
Load Regulation	–200μA≤Io≤200μA		8	25	mV
ERROR AMPLIFIER (Note 3)					
Input Offset Voltage	Vcm=5V, Vo=2V, Io=0	–10		10	mV
Input Bias Current	Vcm=0V	–2.0	–0.3		μA
Voltage Gain	Vcm=5V, 0.5V≤Vo≤3.7V, Io=0	70	100		dB
Power Supply Rejection Ratio	Vcm=5V, Vo=2V, 12V≤Vcc≤20V	70	100		dB
Common Mode Rejection Ratio	0V≤Vcm≤6V, Vo=2V	70	100		dB
Vout Low	Vid=–100mV, Io=200μA		0.05	0.20	V
Vout High	Vid=100mV, Io=–200μA	4.0	4.3		V
Unity Gain Bandwidth		0.7	1.0		MHz

PARAMETER	TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNITS
VOLTAGE CONTROLLED OSCILLATOR					
Maximum Frequency	Vid (Error Amp)=100mV, TJ=25oC	450	500	550	kHz
Maximum Frequency	Vid (Error Amp)=100mV	425		575	kHz
Minimum Frequency	Vid (Error Amp)=−100mV, TJ=25oC	45	50	55	kHz
Minimum Frequency	Vid (Error Amp)=−100mV	42		58	kHz
ONE SHOT					
Zero Comparator Vth		0.45	0.50	0.55	V
Propogation Delay	(Note 4)		100	200	ns
Maximum Pulse Width	Vzero=1V	900	1000	1100	ns
Maximum to Minimum Pulse Width Ratio	Vzero=0V	5	6	7	
OUTPUT STAGE					
Rise and Fall Time	Cload=1nF (Note 4)		30	60	ns
Output Low Saturation	Io=20mA		0.2	0.4	V
Output Low Saturation	Io=200mA		0.5	2.2	V
Output High Saturation	Io=−20mA, down from Vcc		1.5	2.0	V
Output High Saturation	Io=−200mA, down from Vcc		1.7	2.5	V
UVLO Low Saturation	Io=20mA		0.8	1.5	V
FAULT COMPARATOR					
Fault Comparator Vth		2.85	3.00	3.15	V
Delay to Output	(Note 4) (Note 5)		100	200	ns
UVLO					
Vcc Turn-on Threshold	UCxx61, UCxx65	15	16	17	V
Vcc Turn-on Threshold	UCxx64	7.2	8.0	8.8	V
Vcc Turn-off Threshold	UCxx61, UCxx65	9	10	11	V
Vcc Turn-off Threshold	UCxx64	6.2	7.0	7.8	V
Icc Start	Vcc=Vcc(on)−0.3V		150	300	µA
Icc Run	Vid=100mV		20	30	mA

Note 1: Currents are defined as positive into the pin
Note 2: Pulse measurement techniques are used to insure that $T_J=T_A$
Note 3: Vid=V(NI)-V(INV)
Note 4: This parameter is not 100% tested in production but guaranteed by design.
Note 5: Vi= 0 to 4V, tr(Vi)≤ 10ns tpd=t(Vo=6V)-t(Vi=3V)

UVLO & 5V GENERATOR (See Figure 1)

When power is applied to the chip and Vcc is less than the upper UVLO threshold, Icc will be less than 300µA, the 5V generator will be off, and the outputs will be actively held low.

When Vcc exceeds the upper UVLO threshold, the 5V generator turns on. Until the 5V pin exceeds 4.9V, the outputs will still remain low.

The 5V pin should be bypassed to signal ground with a 0.1uF capacitor. The capacitor should have low equivalent series resistance and inductance.

FAULT AND SOFT-REFERENCE (See Figure 1)

The Soft-Ref pin serves three functions: System reference, restart delay, and soft-start. Designed to source or sink 200uA, this pin should be used as the input reference for the error amplifier circuit. This pin requires a bypass capacitor of at least 0.1µF. This yields a minimum soft-start time of 1ms.

Under-Voltage Lockout sets both the fault and restart delay latches. This holds the outputs low and discharges the Soft-Ref pin. After UVLO, the fault latch is reset by the low voltage on the Soft-Ref pin. The reset fault latch resets the delay latch and Soft-Ref charges via the 0.5mA current source.

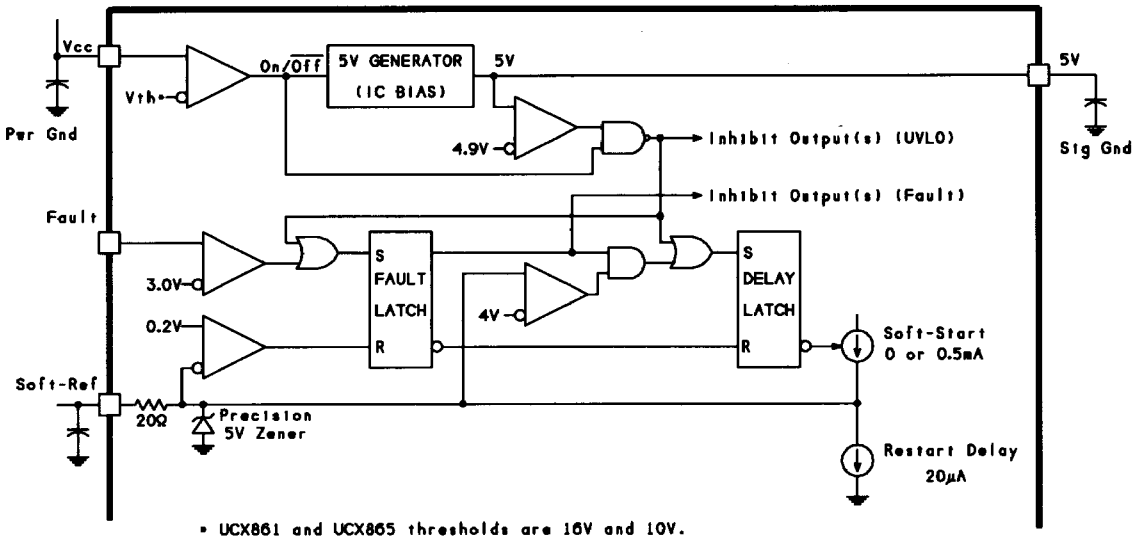
The fault pin is input to a high speed comparator with a threshold of 3V. In the event of a detected fault, the fault latch is set and the outputs are driven low. If Soft-Ref is above 4V, the delay latch is set. Restart delay is timed as Soft-Ref is discharged by 20µA. When Soft-Ref is fully discharged, the fault latch is reset if the fault input signal is low. The Fault pin can be used as a system shutdown pin.

If a fault is detected during soft-start, the fault latch is set and the outputs are driven low. The delay latch will remain reset until Soft-Ref charges to 4V. This sets the delay latch, and restart delay is timed. Note that restart delay for a single fault event is longer than for recurring faults since Soft-Ref must be discharged from 5V instead of 4V.

The restart delay to soft-start time ratio is 24:1 for a fault occurring during normal operation and 19:1 for faults occurring during soft-start. Shorter ratios can be programmed down to a limit of approximately 3:1 by the addition of a 20K or larger resistor from Soft-Ref to ground.

A 100K resistor from Soft-Ref to 5V will have the effect of permanent shut down after a fault since the internal 20µA current source can't pull Soft-Ref low. This feature can be used to require recycling Vcc after a fault. Care must be taken to insure Soft-Ref is indeed low at start up, or the fault latch will never be reset.

UVLO, 5V, Fault, and Soft-Ref



* UCX861 and UCX865 thresholds are 16V and 10V.
UCX864 thresholds are 8V and 7V.

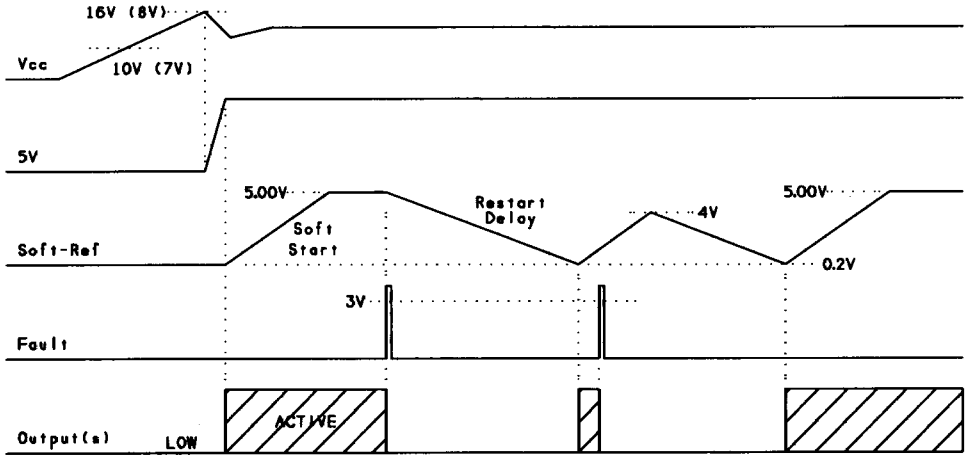


Figure 1

Error Amp, Voltage Controlled Oscillator, and One Shot

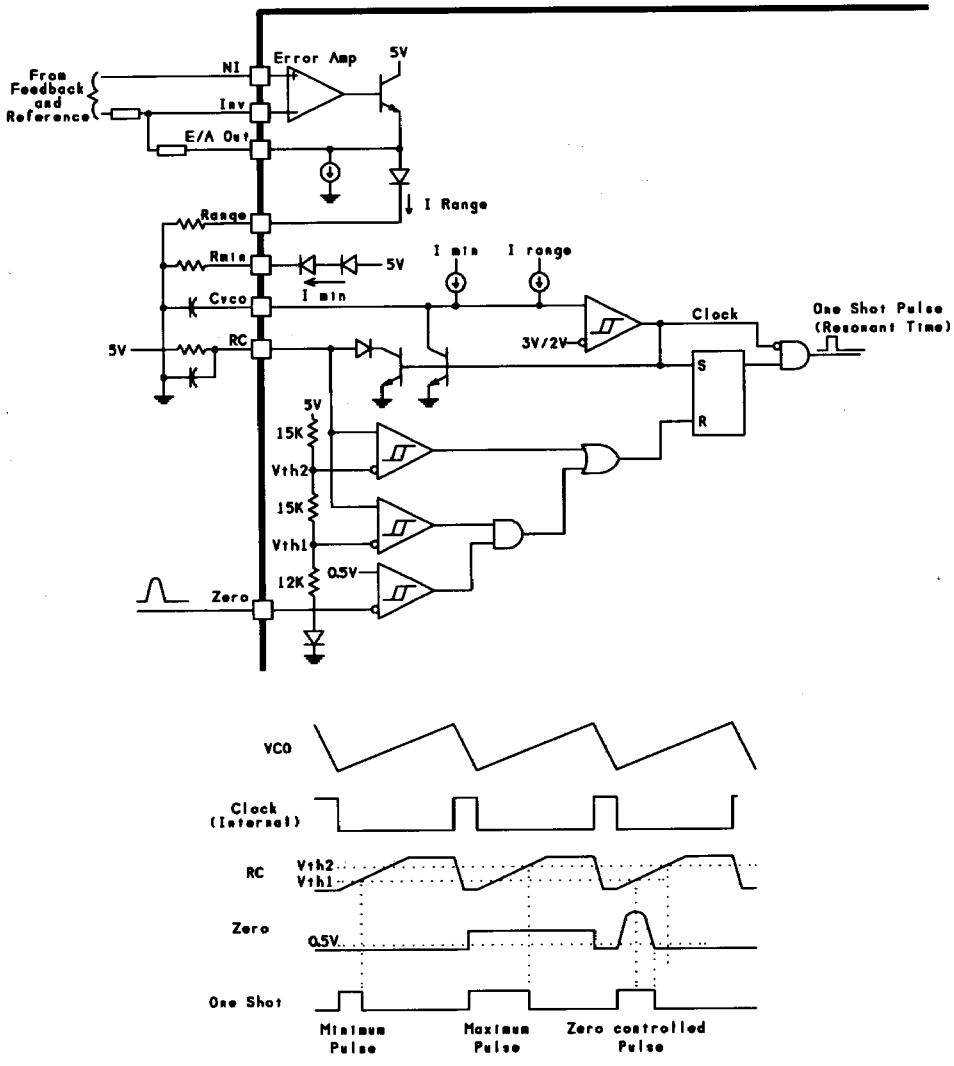


Figure 2

Minimum oscillator frequency is set by Rmin and Cvco. The minimum frequency is approximately given by the equation:

$$Fmin = \frac{4.5}{Rmin * Cvco}$$

Maximum oscillator frequency is set by Rmin, Range & Cvco. The maximum frequency is approximately given by the equation:

$$Fmax = \frac{3.6}{(Rmin||Range) * Cvco}$$

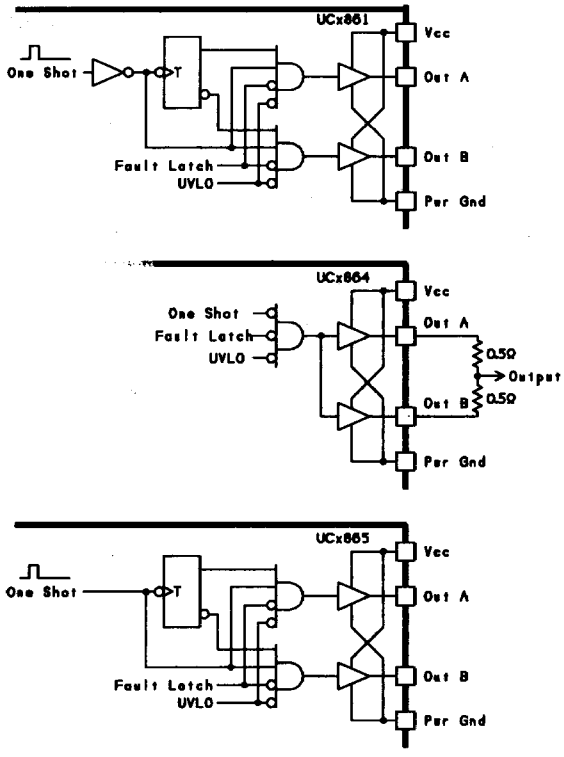
The Error Amplifier directly controls the oscillator frequency. E/A output low corresponds to minimum frequency and output high corresponds to maximum frequency. At the end of each oscillator cycle, the RC pin is discharged to one diode drop above ground. At the beginning of the oscillator cycle, V(RC) is less than Vth1 and so the output of the zero detect comparator is ignored. After V(RC) exceeds Vth1, the one shot pulse will be terminated as soon as the zero pin falls below 0.5V or V(RC) exceeds Vth2. The minimum one shot pulse width is approximately given by the equation:

$$Tpw(min) = 0.2 * R * C.$$

The maximum pulse width is approximately given by:

$$Tpw(max) = 1.2 * R * C.$$

Steering Logic



The steering logic is configured on the UC1861 to result in dual non-overlapping square waves at outputs A & B. This is suited to drive dual switch ZVS systems.

The steering logic is configured on the UC1864 to result in inverted pulse trains occurring identically at both output pins. This is suited to drive single switch ZVS systems. Both outputs are available to drive the same MOSFET gate. It is advisable to join the pins with 0.5 ohm resistors.

The steering logic is configured on the UC1865 to result in alternating pulse trains at outputs A & B. This is suited to drive dual switch ZCS systems.

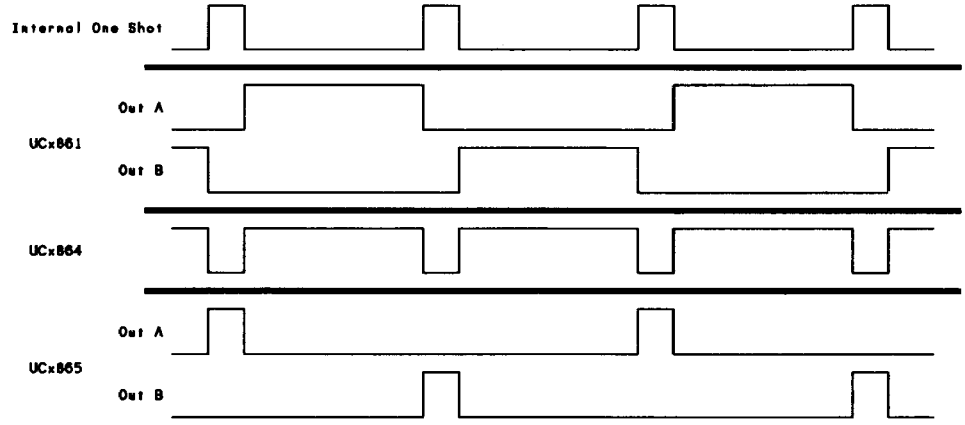


Figure 3

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