High Efficiency, Synchronous, Step-down (Buck) Controllers

FEATURES

- Operation to 36V Input Voltage
- Fixed Frequency Average Current Mode Control
- 2V to 3.5V Output Voltage when Combined with UC3910 Precision Reference/DAC
- Drives External N-Channel MOSFETs for Highest Efficiency
- Sleep Mode Current <75µA
- Complementary 1 Amp Outputs with Regulated Gate Drive Voltage
- LDO (Low Drop Out) Virtual 100% Duty Cycle Operation
- Non-Overlapping Gate Drives

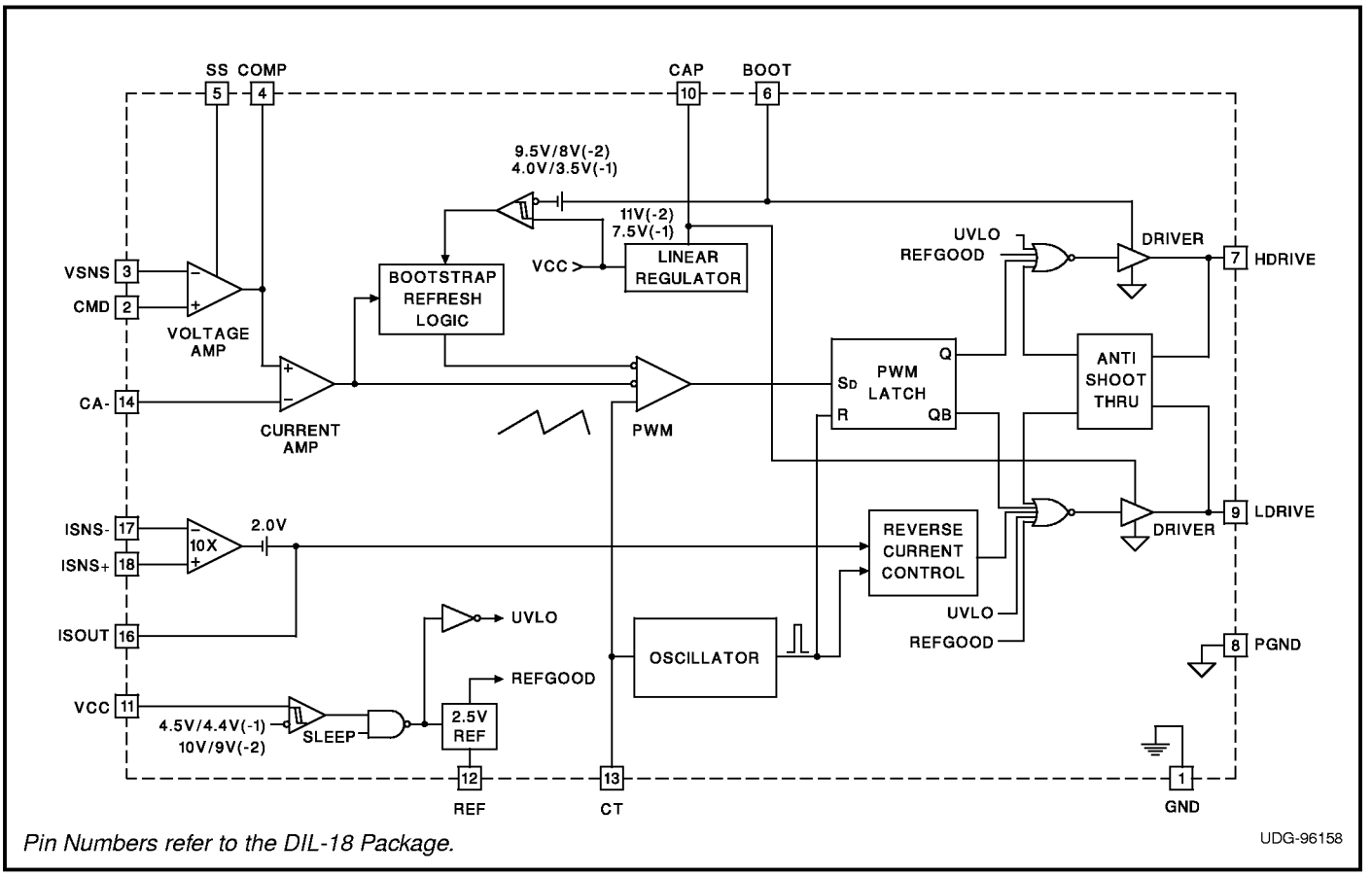
DESCRIPTION

The UC3870 family of synchronous step-down (Buck) regulators provides high efficiency power conversion from an input voltage range of 4.5 to 36 volts. The UC3870 is tailored for battery powered applications such as laptop computers, consumer products, communications systems, and aerospace which demand high performance and long battery life. The synchronous regulator replaces the catch diode in the standard buck regulator with a low Rds(on) N-channel MOSFET switch allowing for significant efficiency improvements. The high side N-channel MOSFET switch is driven out of phase from the low side N-channel MOSFET switch by an on-chip bootstrap circuit which requires only a single external capacitor to develop the regulated gate drive. Fixed frequency, average current mode control provides the regulator with inherent slope compensation, tight regulation of the output voltage, and superior load and line transient response. Switching frequencies up to 300kHz are possible.

The UC3870-1,-2 is designed to interface directly with precision references like the UC3910. When combined with the UC3910, output voltages between 2V to 3.5V in 100mV increments and ± 1% accuracy are attainable. This makes the UC3870-1,-2 ideal for powering high performance microprocessors like the Intel Pentium® Pro and others.

(continued)

BLOCK DIAGRAM



Pin Numbers refer to the DIL-18 Package.

DESCRIPTION (continued)

A low power sleep mode can be invoked through the SS pin. Quiescent supply current in sleep mode is typically less than 50µA. Two UVLO options are available. The UC3870-1 is designed for logic level MOSFETs and has UVLO turn-on and turn-off thresholds of 4.5V and 4.4V respectively. The UC3870-2 is designed for standard power MOSFETs and has UVLO turn-on and turn-off thresholds of 10V and 9V respectively. A precision 2.5V reference can supply 20mA to external circuitry. An error amplifier with soft start, high bandwidth current amplifier, and a synchronizable oscillator are additional features.

Available packages include 18-pin plastic and ceramic DIP (N, J), 18-pin SOIC (DW), and 20-pin plastic and ceramic leadless chip carriers (Q, L).

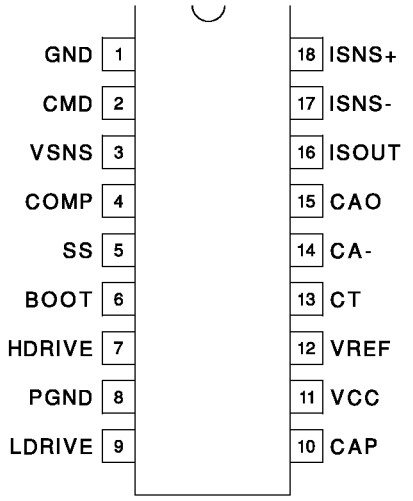
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC) 36V
Boost Voltage (BOOT) 50V
OUTPUT Drivers (HDRIVE, LDRIVE) Currents
(continuous) . . . . . ±0.25A
(peak) . . . . . ±1A
VREF Current . . . . . internally limited
Inputs (VSNS, SS, COMP, CT) . . . . . –0.3 to 10V
Inputs (CMD) . . . . . –0.3 to 7.5V
Inputs (ISNS+, ISNS-) . . . . . –0.3 to20V
Outputs (CAO) . . . . . –0.3 to10V
Soft start Sinking Current 1.5mA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

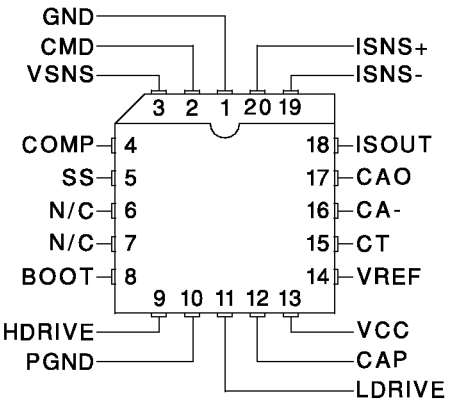
All currents are positive into, negative out of the specified terminal. All voltages are referenced to GND. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

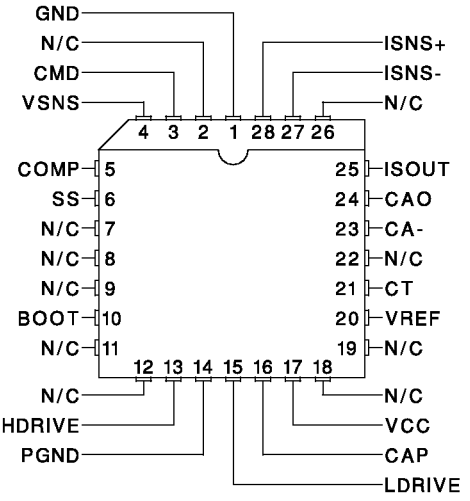
DIL-18 (TOP VIEW)
J or N, DW Packages



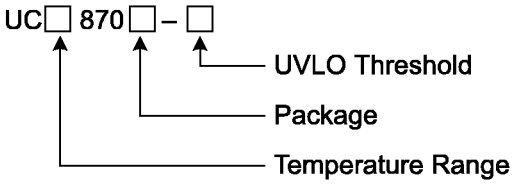
PLCC-20 (TOP VIEW)
J or N, DW Packages



PLCC-20 (TOP VIEW)
J or N, DW Packages



ORDERING INFORMATION



UVLO Turn On/Off Threshold	Package	Temperature Range
1: 4.5V/4.4V	J: Ceramic DIL-18	1: –55°C to +125°C
2: 10V/9V	N: Plastic DIL-18	2: –40°C to +85°C
	DW: SOIC-18	3: 0°C to +70°C

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1870X; –25°C to +85°C for UC2870X; 0°C to +70°C for UC3870X; VCC = 12V, C = 680pF, C_{CAP} = 1µF; C_{BOOT} = 0.1µF, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall Section					
Supply Current, Sleep	SOFTSTART=0V; T_A = 25°C		30	75	µA
Supply Current, Operating			8.5	12	mA
VCC Turn-on Threshold	UCX870-2		10	10.5	V
	UCX870-1		4.5	4.8	V
VCC Turn-off Threshold	UCX870-2	8.5	9		V
	UCX870-1	4.1	4.4		V
Voltage Amplifier Section					
Input Voltage Offset	T_A = 25°C	–30	0	30	mV
VSNS Bias Current		–500	25	500	nA
Transconductance	I_{COMP} = +10µA to –10µA; UC3870 -1, -2; UC2870 -1, -2;	400	675	1000	µMho
	I_{COMP} = +5µA to –5µA; UC1870 -1, -2	250	675	1250	µMho
V_{OUT} High		2.9	3.1	3.25	V
V_{OUT} Low			0.15	1	V
Output Source Current	V_{OUT} = 1V; UC3870 -1, -2; UC2870 -1, -2;	10	35		µA
	V_{OUT} = 1V; UC1870 -1, -2	5	35		µA
Current Amplifier Section					
Input Offset Voltage	V_{COMP} = 2.5V	–6	0	6	mV
Input Bias Current(sense)	V_{CM} = 2.5V	–500		500	nA
Open Loop Gain	V_{CM} = 2.5V, V_{OUT} = 1V to 3.5V	80	110		dB
V_{OUT} High	R_{CAOUT} = 100k to GND, T_A = 25°C	3.6	3.7		V
V_{OUT} Low	R_{CAOUT} = 100k to VREF, T_A = 25°C		0.7	0.86	V
Output Source Current	V_{OUT} = 0V, T_A = 25°C	80	100	120	µA
Common Mode REJ Ratio	V_{CM} = 2V to 3V	70	90		dB
Gain Bandwidth Product	F_{IN} = 100kHz, 10mV p-p	2	3.5		MHz
Reference Section					
Output Voltage	I_{REF} = 0mA, T_A = 25°C	2.462	2.5	2.538	V
	I_{REF} = 0mA	2.437	2.5	2.563	V
Load Regulation	I_{REF} = 0mA to 5mA		2	±15	mV
Line Regulation	VCC = 12V to 24V		2	±15	mV
Short Circuit Current	VREF = 0V	10	20	25	mA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1870X; –25°C to +85°C for UC2870X; 0°C to +70°C for UC3870X; VCC = 12V, C_T = 680pF, C_{CAP} = 1µF; C_{BOOT} = 0.1µF, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section					
Initial Accuracy	T_A = 25°C	85	100	115	kHz
Voltage Stability	VCC = 12V to 18V		1	1.5	%
Total Variation	Line, Temperature	80		120	kHz
Ramp Amplitude (p-p)	T_A = 25°C	2.48	2.7	2.85	V
Ramp Valley Voltage	T_A = 25°C	0.86	0.95		V
Sleep/Soft Start/Bootstrap Section					
Sleep Threshold	Measured on SS, T_A = 25°C	0.25	0.6	0.8	V
SS Charge Current	V_{SS} = 2.5V	4	6	10	µA
SS Discharge Current	V_{SS} = 2.5V	0.5	0.8		mA
Bootstrap Regulation Voltage	UCX870-2, Low Driver ON	9.5	10.2	12.5	V
	UCX870-1, Low Driver ON	6	7.5	9	V
Bootstrap Refresh Voltage	UCX870-2, $V_{CAOUT} > V_{CTpeak}$	7	8	9	V
	UCX870-1, $V_{CAOUT} > V_{CTpeak}$	2.7	3.5	4	V
High Side Driver Output Section					
Output High Voltage	I_{OUT} = –50mA, BOOT = 23V	21	22.2		V
Output Low Voltage	I_{OUT} = 50mA		1	2.2	V
	I_{OUT} = 10mA		300	500	mV
Output Low (UVLO)	I_{OUT} = 50mA, VCC = 0V		0.9	1.5	V
Output Rise Time	C_{OUT} = 1nF		40	160	ns
Output Fall Time	C_{OUT} = 1nF		30	100	ns
Low Side Driver Output Section					
Output High Voltage	I_{OUT} = –50mA, V_{CAP} = 11V	8.8	9.5		V
Output Low Voltage	I_{OUT} = 50mA		1	2.2	V
	I_{OUT} = 10mA		300	500	mA
Output Low (UVLO)	I_{OUT} = 50mA, VCC = 0V		0.9	1.5	V
Output RISE/FALL Time	C_{LOAD} = 1nF		40	160	ns
Output FALL Time	C_{OUT} = 1nF		30	100	ns
X10 Amplifier Section					
Gain	$V_{ISNS} \pm V_{ISNS}$ = 20mV to 80mV	9.2	10	10.4	V/V
Slew Rate Rising	T_A = 25°C	1	1.4		V/µs
Slew Rate Falling	T_A = 25°C	2	3.5		V/µs
Input Resistance	T_A = 25°C	60	100	165	kΩ

PIN DESCRIPTIONS

BOOT: This pin provides the high side rail for the HDRIVE output. An external capacitor (Cbst) is connected between this pin and the drain of the external low side MOSFET. When the low side MOSFET is conducting Cbst is charged to 11V (UC3870-2), 7.5V (UC3870-1), via an external diode tied to CAP. When the low side MOSFET turns off and the high side MOSFET turns on, the Cbst bootstraps itself up with the source of high side MOSFET, ultimately providing a 10V Vgs for the upper MOSFET. Since this 10V is referenced to the source of the high side N-channel MOSFET, the actual voltage on BOOT and HDRIVE is approximately 10V above VCC while the high side MOSFET is conducting. The voltage on BOOT is continuously monitored during low input voltage conditions when the duty cycle equals approximately 100% to insure that a sufficient gate drive level is being supplied by the UC3870. If the voltage on BOOT falls below 8V (UC3870-2) or 3.5V (UC3870-1), the IC forces the low side driver to cycle itself on for the few cycles required to replenish Cbst. In this way, virtual 100% duty cycle operation is provided.

CA-: This is the inverting input to the current amplifier. Connect a series resistor and capacitor between this pin and CAO to set the current loop compensation. An input resistor between this pin and ISOUT provides the inductor current sense signal to the amplifier and also sets the high frequency gain of the amplifier. The common mode operating range for this input is between GND and 4V. The normal range during operation is between 2V and 3V.

CAO: This is the output of the wide bandwidth current amplifier and one of the inputs to the PWM duty cycle comparator. The output signal generated by this amplifier commands the PWM to force the correct duty cycle to maintain output voltage in regulation. The output can swing from 0.1V to 4V.

CAP: A capacitor is normally connected between this pin and GND providing bypass for the internal 11V (UC3870-2) and 7.5V (UC3870-1) regulator. Charge is transferred from this capacitor to Cbst via an external diode when the low side MOSFET is conducting. If VCC ≤ 10V logic level MOSFETs are generally specified. CAP should then be shorted to VCC in conjuncton with a low VF Schottky to BOOT to maximize the gate drive amplitude. This technique provides adequate gate drive signal amplitudes with VCC as low as 4.5V. For high input voltage applications, a simple external shunt zener regulator circuit can be connected to CAP, thereby offloading power dissipation requirements from the IC to an external transistor.

COMP: This is the output of the voltage amplifier. It provides the current command signal to the current amplifier. The voltage is clamped to approximately 3.2V.

CMD: This is the non-inverting input of the voltage error amplifier. The voltage applied to CMD sets the output voltage of the power converter. The 2V to 3.5V input common mode range allows for direct interfacing to the UC3910 DAC/precision reference.

CT: A capacitor from CT to GND sets the PWM oscillator frequency according to the following equation:

$$F = \frac{1}{14250 \bullet CT}.$$

Use a high quality ceramic capacitor with low ESL and ESR for best results. A minimum CT value of 220pF insures good accuracy and less susceptibility to circuit layout parasitics. The oscillator and PWM are designed to provide practical operation to 300kHZ.

GND: All voltages are measured with respect to this pin. All bypass capacitors and timing components except those listed under the PGND pin description should be connected to this pin. Component leads should be as short and direct as possible.

HDRIVE, LDRIVE: The outputs of the PWM are totem pole MOSFET gate drivers on the HDRIVE and LDRIVE pins. The outputs can sink approximately 1A and source 500mA. This characteristic optimizes the switching transitions by providing a controlled dV/dT at turn-on and a lower impedance at turn-off. These are complementary outputs with a typical deadtime of 200ns. Internal circuitry prevents the possibility of simultaneous conduction of the output MOSFETs (shoot through). HDRIVE is the high side bootstrapped output. Its upper power supply rail is the BOOT pin which means that its output will fly approximately 10V above VCC when the upper side of the totem pole output is conducting. The power supply rail for LDRIVE is CAP. As a result the Vgs of both gates are regulated to approximately 10V if VCC is >11V. A series resistor between these pins and the MOSFET gates of at least 10 ohms can be used to control ringing. Additionally, a low VF Schottky diode should be connected between these pins and GND to prevent substrate conduction and possible erratic operation.

ISNS–: This is the inverting input to the X10 instrumentation amplifier. The common mode input range for this pin extends from GND to VCC. A low value resistor in series with the output inductor is connected between this pin and ISNS+ to develop the current sense signal.

PIN DESCRIPTIONS (continued)

ISNS+: This is the non-inverting input to the X10 instrumentation amplifier. The common mode input range for this pin extends from GND to VCC.

ISOUT: This is the output of the X10 instrumentation amplifier. The output voltage on this pin is level shifted 2V above GND, such that if a 100mV differential input is applied across ISNS+ and ISNS–, the output will be 3V.

PGND: This is the high current ground for the IC. The MOSFET driver transistors are referenced to this ground. For best performance an external star ground connection should be made between this pin, the source of the low side MOSFET, the capacitor on CAP, the anodes of any external Schottky clamp diodes and the output filter capacitor. As with all high frequency layouts, a ground plane and short leads are highly recommended.

SS: A capacitor from this pin to GND in conjunction with an internal 10μA current source provides a soft start function for the IC. The voltage level on SS clamps the output of the voltage amplifier through an internal buffer, thus providing a controlled startup. The SS time is approximately:

$$\frac{C_{SS} \bullet \left(\frac{V_O}{V_{IN}}\right) \bullet 3V}{10\mu A}$$

Once the device has completed its soft start cycle, a low power sleep mode can be invoked by pulling SS below 0.5V typically. In sleep mode, all of the device functions are disabled except for those which are required to bring the device out of sleep mode when SS is released. Typical sleep mode supply current is less than 50mA.

VCC: Positive supply rail for the IC. Bypass this pin to GND with a 1mF low ESL/ESR ceramic capacitor. The maximum voltage for VCC is 36V. The turn on voltage level on VCC is 4.5V with 100mV of hysteresis for the UC3870-1 and 10V with 1V of hysteresis for the UC3870-2.

VREF: V_{REF} is the output of the precision reference. The output is capable of supplying 20mA to peripheral circuitry and is internally short circuit current limited. VREF is disabled and low whenever VCC is below the UVLO threshold, and when SS is pulled below 0.5V. A VREF "good" comparator senses VREF and disables the PWM stage until VREF has attained approximately 90% of its nominal value. Bypass VREF to GND with a 0.1mF ceramic capacitor for best performance.

VSNS: This pin is the inverting input of the voltage amplifier and serves as the output voltage feedback point for the synchronous regulator. It senses the output voltage through a voltage divider which produces a nominal 2V.

APPLICATIONS INFORMATION

The UC3870 employs a fixed frequency average current mode control buck topology to convert a higher battery voltage down to a tightly regulated output voltage. Special design techniques allow this bipolar IC to deliver exceptional performance while consuming approximately 6mA of supply current over an input voltage range of 4.5 to 35 volts. Fixed frequency operation allows synchronization to an existing system clock, and easier filtering. Average current mode control provides inherent slope compensation and accurate short circuit current limiting.

The output inductor current is sensed by an external low value shunt resistor (R_{SENSE}). This signal at full load current should be no larger than 100mV in order to minimize sensing losses. The differential voltage across Rsense is amplified by the internal X10 instrumentation amplifier. The common mode input range for this amplifier extends from GND to VCC in order to maintain accurate current sensing under normal conditions as well as abnormal conditions such as output short circuit and low drop out (LDO) modes. The output of the X10 instrumentation amplifier is applied to the inverting input of the current amplifier through an external resistor. The converter's output voltage feedback is applied to the VSNS pin through an external voltage divider. The difference between the voltage at VSNS and the voltage at the non-inverting input is amplified by the voltage amplifier and applied to the non-inverting input of the current amplifier. This instantaneous reference level forms the current command input for the average current control loop. The average current amplifier develops the duty cycle command signal by integrating the current feedback signal with respect to the instantaneous current command input. This output is compared to the fixed high amplitude oscillator ramp waveform at the inputs of the PWM comparator to develop duty cycle information for the PWM drive. The large amplitude oscillator ramp provides both high noise margin and built-in slope compensation in average current mode control methodology. The fixed frequency oscillator is programmed with a single ex-

APPLICATION INFORMATION (continued)

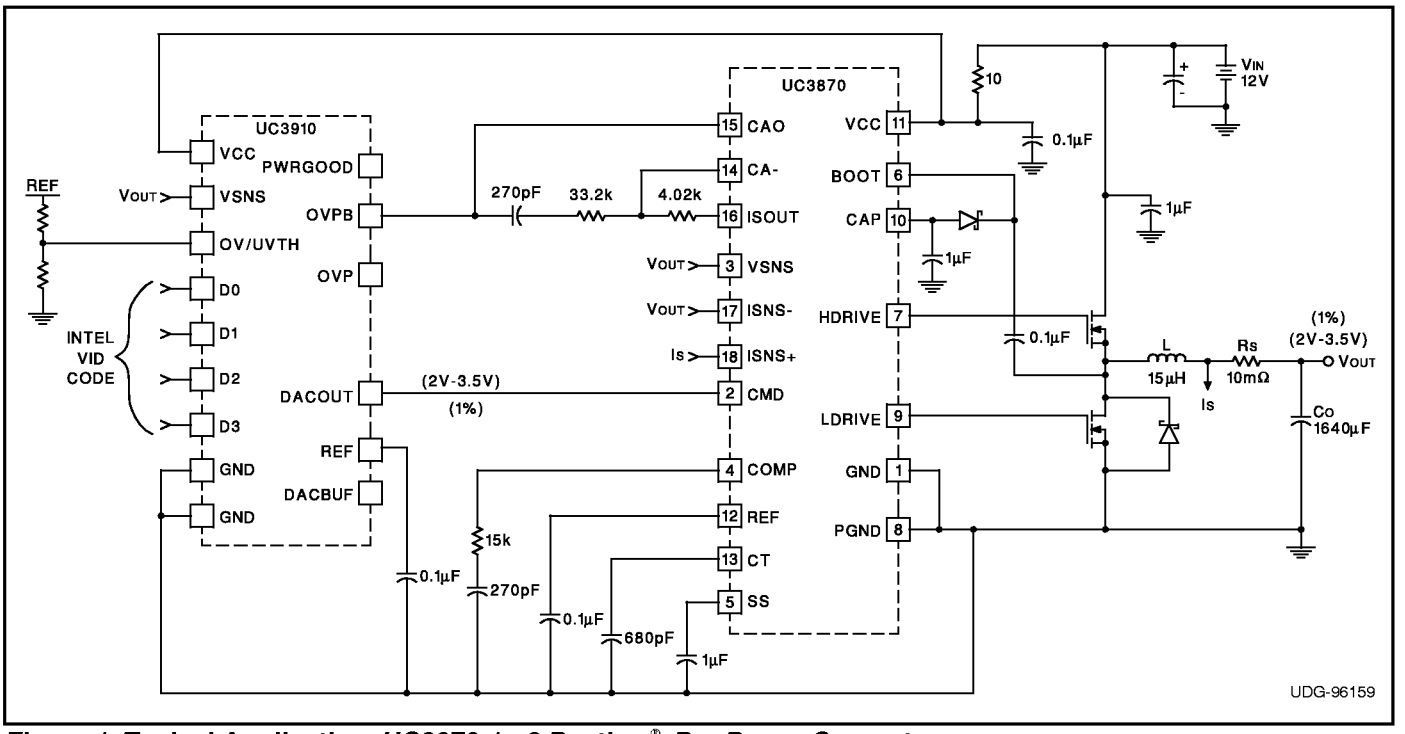


Figure 1. Typical Application: UC3870-1, -2 Pentium® Pro Power Converter

ternal capacitor connected between CT and GND, and is capable of switching frequencies up to 300kHz. The UC3870 can be synchronized to an external clock by capacitively coupling the signal to the junction of the capacitor at CT and a low value resistor tied to GND. Refer to Application Note U-111.

The PWM drive signal is applied to the complementary output driver stages. Since the high side switch is an N–channel MOSFET, a means for driving its gate above VCC is required. This is accomplished via the internal 11V (UC3870-2)/7.5V (UC3870-1) regulator and an external capacitor (C_{BST}). C_{BST} is charged through an external diode to VCC or CAP when the low side MOSFET is on. The charging level on C_{BST} is internally regulated to 11V or 7.5V minus an external diode drop by the UC3870 as long as VCC is above 11V. When the low side MOSFET turns off, C_{BST} is applied across the gate to the source of the upper MOSFET allowing it to begin turn-on. As the upper MOSFET turns on, it lifts or bootstraps the low end of C_{BST}, along with its source. Shortly thereafter, the source voltage level is reduced by RDS(on) · I_{LOAD} below VCC. When VCC < 10V, V_{GS} for the high side MOSFET is approximately equal to VCC. If VCC < 8V, logic level MOSFETs are recommended. In these applications, CAP should be shorted to VCC and an external Schottky diode is connected between CAP/VCC and BOOT. For low battery applications, a synchronous regulator must be capable of LDO or 100% duty cycle operation. The UC3870 includes circuitry to insure that this mode of operation is possible even though it uses a bootstrapped drive technique for the high side MOSFET. During commanded 100% duty cycle operation, the UC3870 monitors the V_{GS} drive signal applied to the high side MOSFET, and automatically provides complementary pulses to refresh the bootstrap capacitor when this voltage falls below a set threshold. In this way, near 100% duty cycle operation is possible, with effective duty cycle dependent only upon the value of C_{BST}.

High efficiency is obtained primarily by the low side MOSFET which replaces the Schottky diode in the standard buck configuration. Its low $R_{DS(ON)}$ produces a much lower voltage drop than a low VF Schottky diode. As output voltages get lower, these improvements become more evident.

Another efficiency consideration is the the possibility of reverse current in the output inductor. For a non-synchronous regulator this isn't a problem since the diode will block reverse current, allowing discontinuous inductor current operation at light loads. Since the synchronous regulator replaces the diode with a switch, reverse current can and will flow if the low side switch is on when the inductor is depleted. The UC3870 includes circuitry to prevent reverse current from flowing in the in-

APPLICATION INFOMATION (continued)

ductor by disabling the low side gate drive signal during discontinuous mode operation. This increases efficiency by eliminating unnecessary I^2R losses in the MOSFET and the inductor.

Soft start is recommended for Buck converters to reduce stress on the power components during startup, and to reduce overshoot of the output voltage. This improves reliability. The UC3870 includes a user programmable soft start pin to implement this feature. An internal 10mA current source charges the external soft start capacitor which provides a clamp at the output of the voltage amplifier. An ultra low power sleep mode is also invoked from the SS pin. A voltage level below 0.5V on this pin reduces total standby current to less than 50mA. Short circuit protection is inherent to the average current mode technique with proper compensation of the current amplifier. To prevent operation of the MOSFETs with an inadequete drive signal, an undervoltage lockout circuit suppresses the output drivers until the input supply voltage is sufficiently high enough for proper operation. The UC3870-1 is intended for applications with logic level MOSFETs and its VCC turn-on and turn-off thresholds are 4.5V/4.4V respectively. The UC3870-2 is intended for applications with standard MOSFETs and has UVLO turn-on and turn-off thresholds of 10V and 9V respectively. The precision 2.5V reference can provide 10mA to power external circuitry. The reference output is disabled during UVLO and sleep modes.

TYPICAL PERFORMANCE INFORMATION

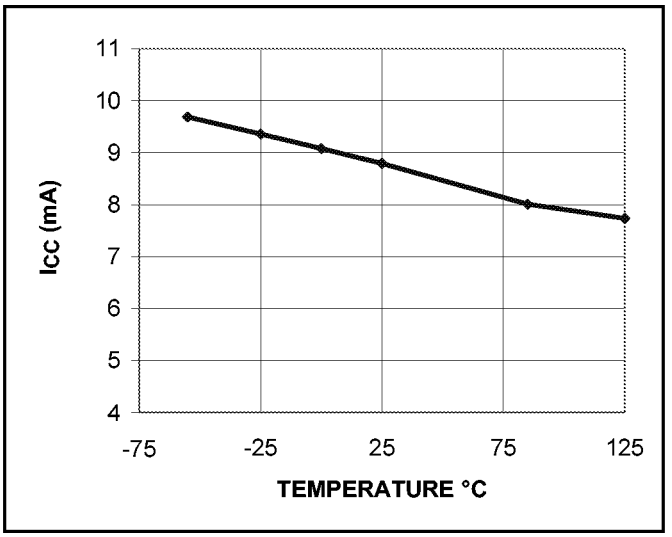


Figure 1. Supply Current

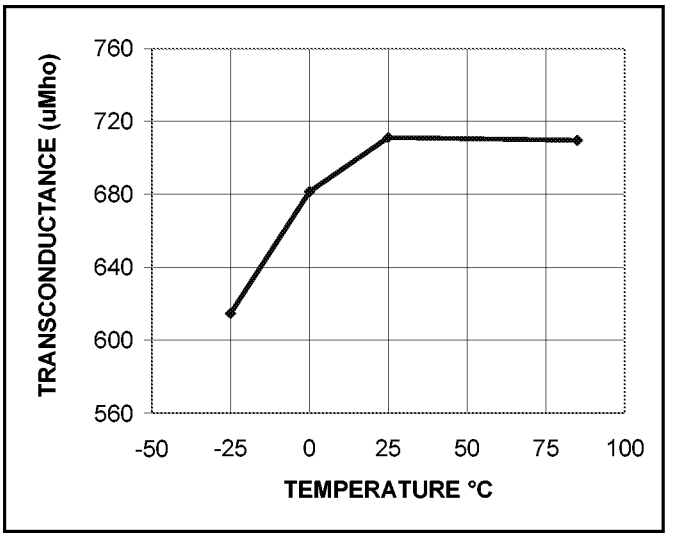


Figure 2. Volt Amp GM (I_{OUT} = ± 10μA)

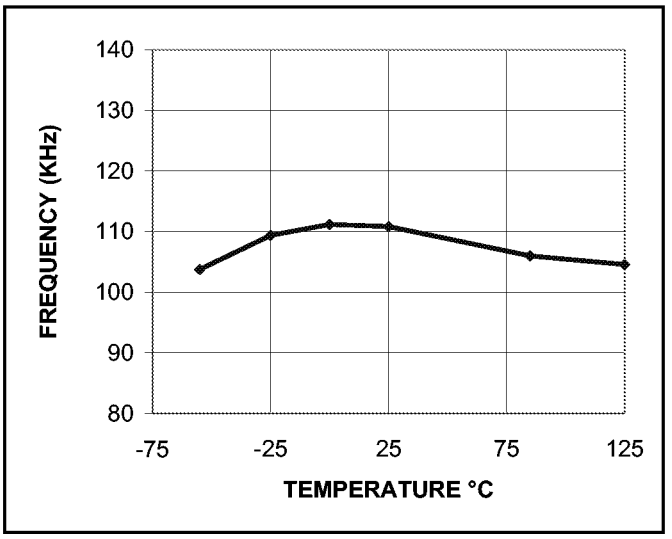


Figure 3. Oscillator Frequency vs. Temperature (CT = 680pF)

TYPICAL PERFORMANCE INFO (continued)

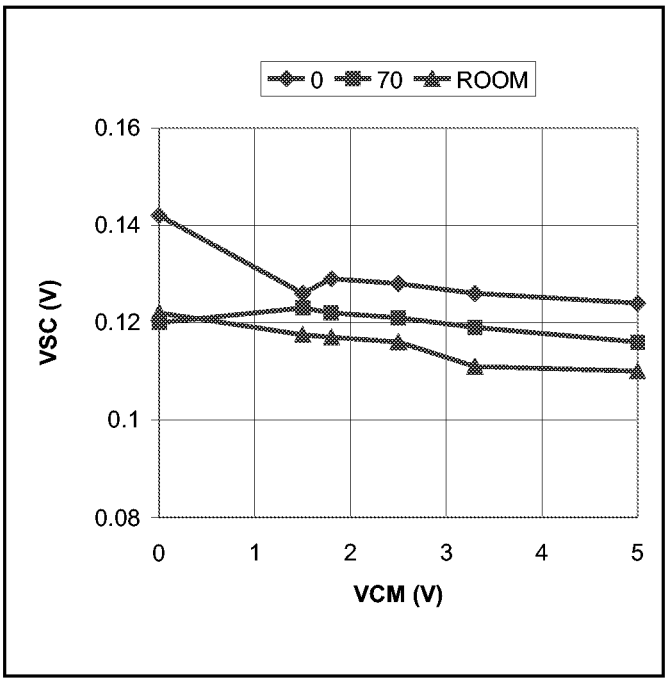


Figure 4. Short Circuit Limit Voltage Reflected to Input of Current Amp vs. Current Amp Common Mode Voltage

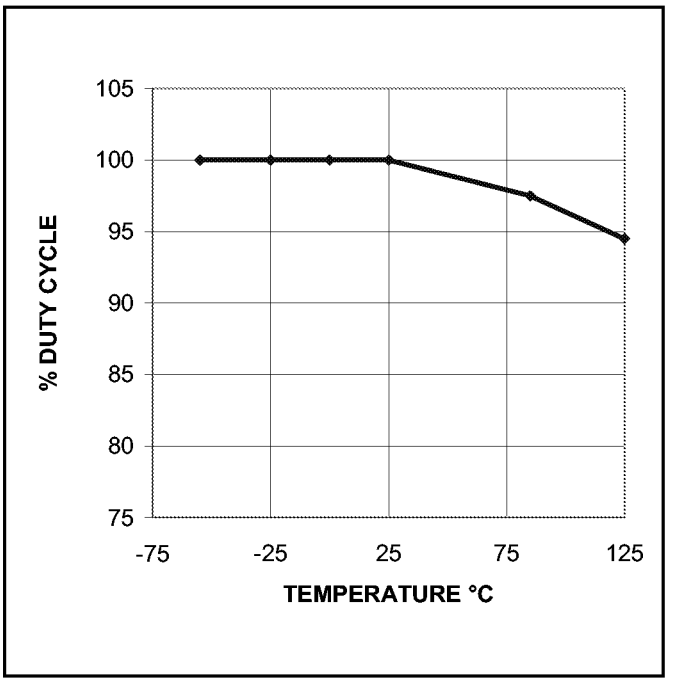


Figure 5. High Drive Maximum Duty Cycle (UC1870-1,-2)

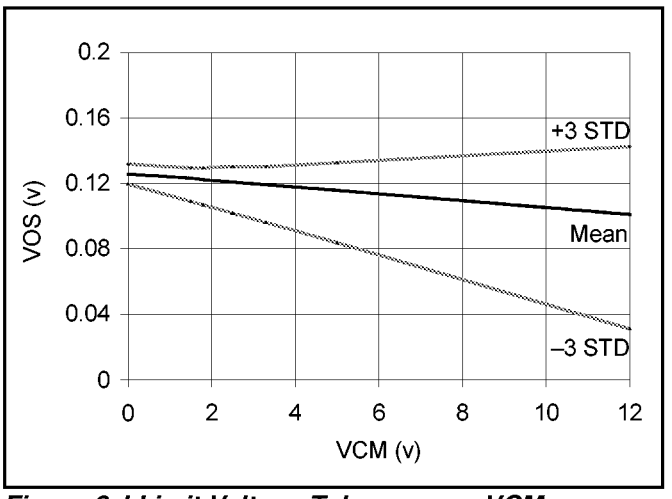


Figure 6. I Limit Voltage Tolerance vs. VCM

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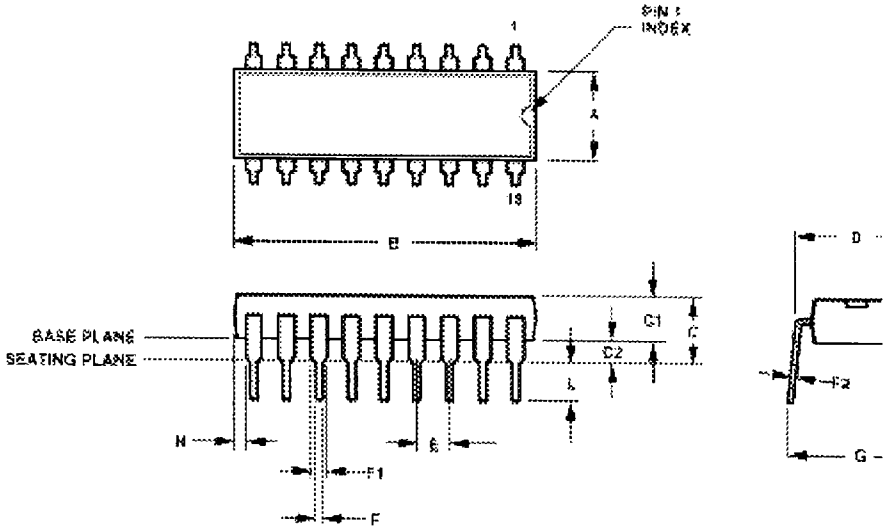
Mechanical Drawings

Back to Packaging Index

18-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.890	.920	22.61	23.39	1
C	-	.210	-	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	-	0.13	-	
L	.115	.160	2.92	4.06	



NOTES:

1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

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UNITRODE

Mechanical Drawings

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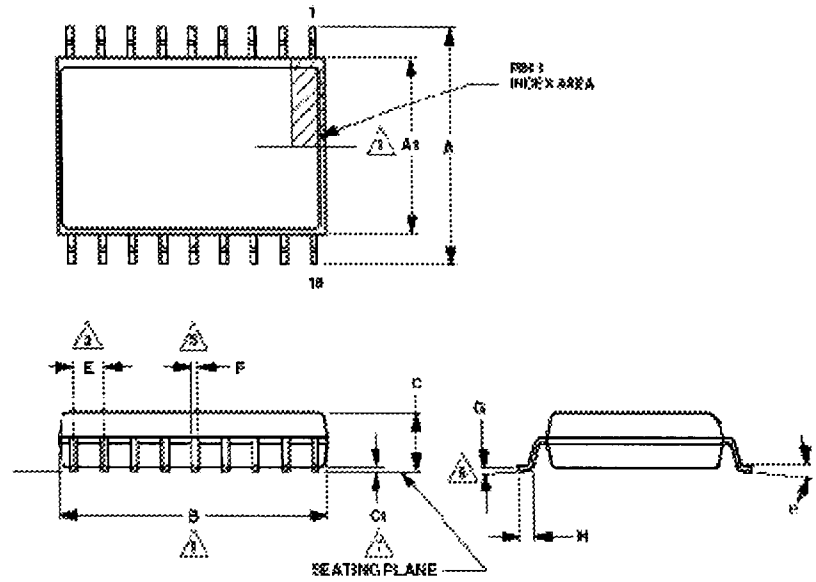
18-PIN SOIC SURFACE MOUNT~ DW PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.453	.462	11.51	11.73
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°



NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED "F" MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

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Mechanical Drawings

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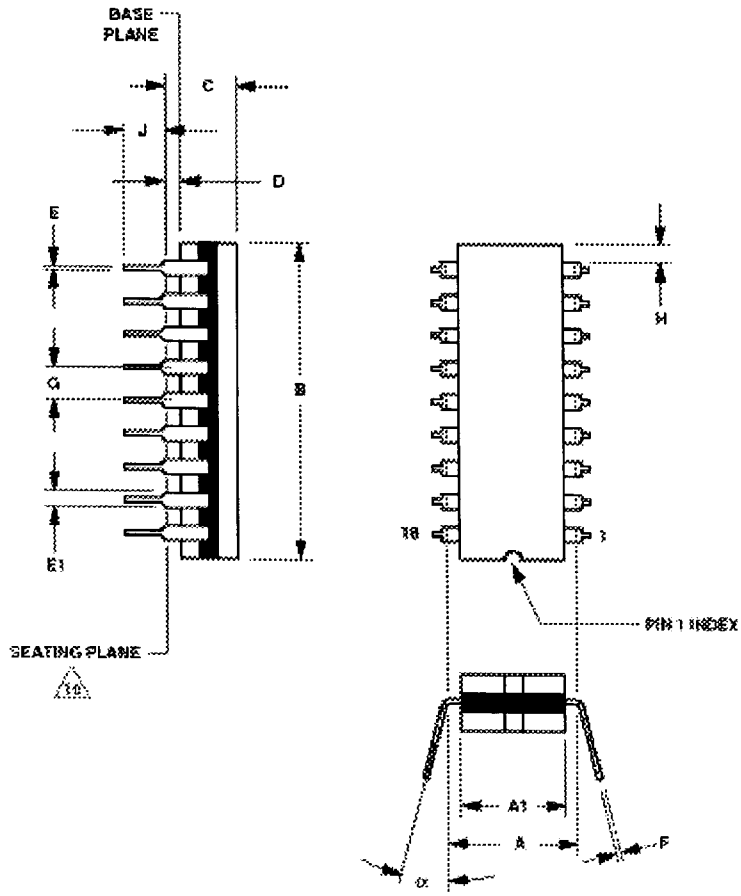
18-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	-	0.960	-	24.38	4
C	-	0.200	-	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	-	0.13	-	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	



NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION 'E1' MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 9, 10 AND 18 ONLY.
3. DIMENSION 'D' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 9, 10 AND 18).
7. DIMENSION 'A' SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS 'E' AND 'F' SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.

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Mechanical Drawings

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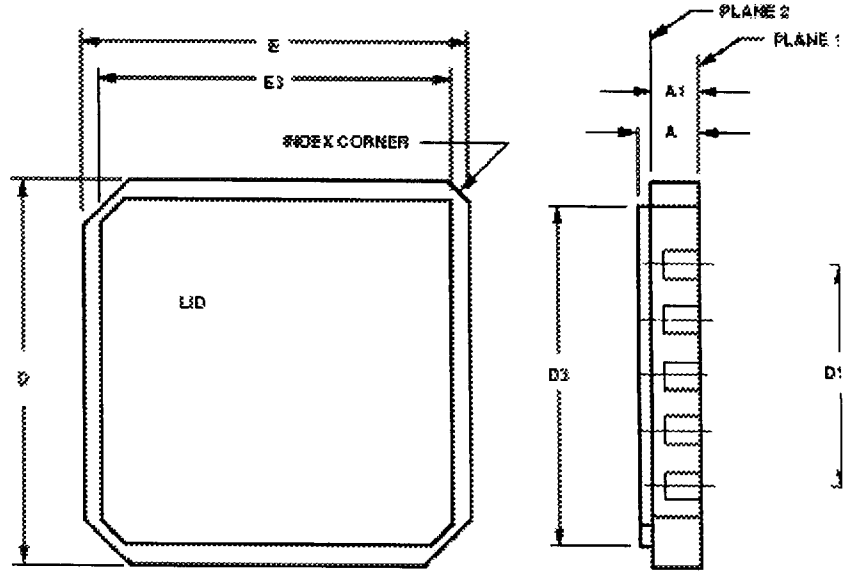
20-PIN CERAMIC LEADLESS SURFACE MOUNT ~ L PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.060	.100	1.52	2.54	6
A1	.050	.088	1.27	2.24	
B1	.022	.028	0.56	0.71	1,3
B2	.072 REF.		1.83 REF.		
B3	.006	.022	0.15	0.56	8
D/E	.342	.358	8.69	9.09	
D1/E1	.200 BSC		5.08 BSC		
D2/E2	.100 BSC		2.54 BSC		
D3/E3	-	.358	-	9.09	4
L	.045	.055	1.14	1.40	
L1	.045	.055	1.14	1.40	
L2	.075	.095	1.90	2.41	5
L3	.003	.015	0.08	0.38	
N	20		20		2
ND/NE	5		5		2
e	.050 BSC		1.27 BSC		10



NOTES:

1. A MINIMUM CLEARANCE OF 0.015 IN. (0.38mm) SHALL BE MAINTAINED BETWEEN ADJACENT TE
2. 'N' IS THE MAXIMUM QUANTITY OF TERMINAL POSITIONS. 'ND' AND 'NE' ARE THE NUMBERS OF AND 'E' RESPECTIVELY.
3. ELECTRICAL CONNECTION TERMINALS ARE REQUIRED ON PLANE 1 AND OPTIONAL ON PLANE THEY SHALL BE ELECTRICALLY CONNECTED TO OPPOSING TERMINALS ON PLANE 1.
4. A MINIMUM CLEARANCE OR 0.015 IN. (0.38mm) SHALL BE MAINTAINED BETWEEN A METAL LID TERMINALS, METALLIZED CASTELLATIONS, ETC.) THE LID SHALL NOT EXTEND BEYOND THE E
5. THE INDEX FEATURE FOR NUMBER 1 TERMINAL IDENTIFICATION, OPTIONAL ORIENTATION OR AREA DEFINED BY DIMENSIONS 'B2' AND 'L2' ON PLANE 1.
6. DIMENSION 'A' CONTROLS THE OVERALL PACKAGE THICKNESS.
7. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
8. CASTELLATIONS ARE REQUIRED ON BOTTOM TWO LAYERS. CASTELLATIONS IN THE TOP LAYE
9. WHEN SOLDER DIP LEAD FINISH APPLIES, SOLDER BUMP HEIGHT SHALL NOT EXCEED 0.007 INC NOT EXCEED 0.006 INCHES.
10. THE BASIC TERMINAL SPACING IS 0.050 INCHES BETWEEN CENTERLINES. EACH TERMINAL CEN INCHES OF ITS EXACT TRUE POSITION.

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UNITRODE

Mechanical Drawings

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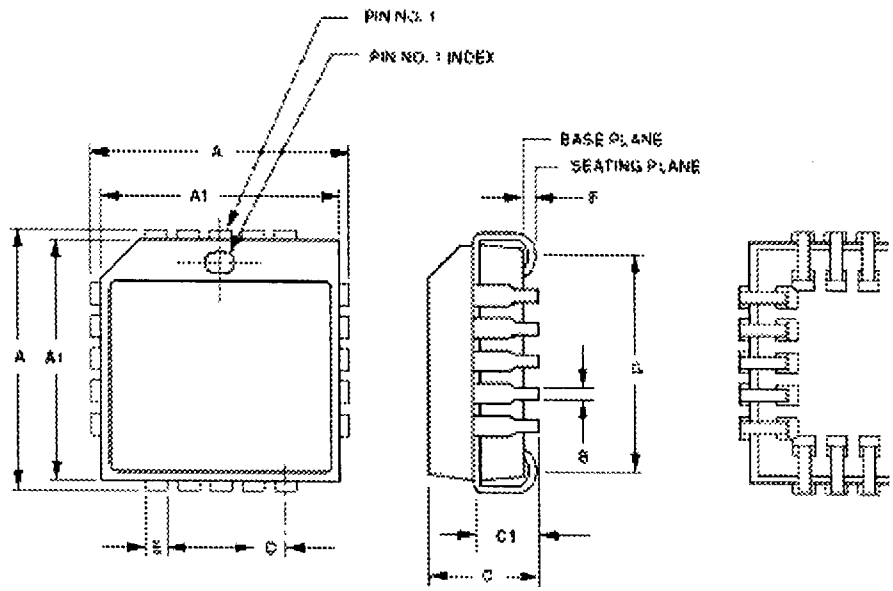
20-PIN PLASTIC PLCC SURFACE MOUNT~ Q PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.385	.395	9.78	10.03	
A1	.350	.356	8.89	9.04	1
B	.013	.021	0.33	0.53	
C	.170	.180	4.32	4.57	
C1	.100	.110	2.54	2.79	
D	.050 BSC		1.27 BSC		2
E	.026	.032	0.66	0.81	
F	.020	-	0.51	-	3, 4
G	.290	.330	7.37	8.38	



NOTES:

1. 'A1' DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
3. 'F' IS MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
5. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.