



High Current FET Driver

FEATURES

- Totem Pole Output with 6A Source/Sink Drive
- 5ns Delay
- 5ns Rise and Fall Time into 2.2nF
- 5ns Rise and Fall Time into 30nF
- 4.7V to 18V Operation
- Inverting and Non-Inverting Outputs
- Under-Voltage Lockout with Hysteresis
- Thermal Shutdown Protection
- MINIDIP and Power Packages

DESCRIPTION

The UC1710 family of FET drivers is made with a high-speed Schotky process to interface between low-level control functions and very high-power switching devices-particularly power MOSFET's. These devices accept low-current digital inputs to activate a high-current, totem pole output which can source or sink a minimum of 6A.

Supply voltages for both V_{IN} and V_C can independently range from 4.7V to 18V. These devices also feature under-voltage lockout with hysteresis.

The UC1710 is packaged in an 8-pin hermetically sealed dual in-line package for -55°C to $+125^{\circ}\text{C}$ operation. The UC3710 is specified for a temperature range of 0°C to $+70^{\circ}\text{C}$ and is available in either an 8-pin plastic dual in-line or a 5-pin, TO-220 package. Surface mount devices are also available.

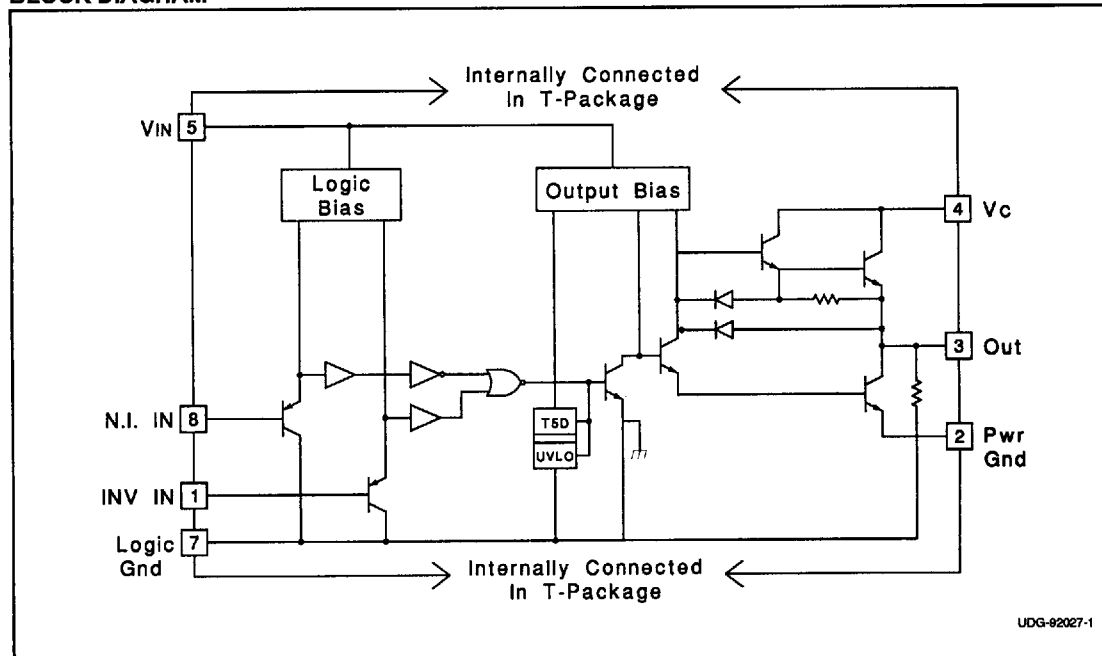
TRUTH TABLE

INV	N.I.	Out
H	H	L
L	H	H
H	L	L
L	L	L

$\text{OUT} = \overline{\text{INV}}$ and N.I.

$\text{OUT} = \text{INV}$ or N.I.

BLOCK DIAGRAM



UDG-92027-1

ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg	T-Pkg
Supply Voltage, V_{in}	20V	20V	20V
Collector Supply Voltage, V_c	20V	20V	20V
Operating Voltage	18V	18V	18V
Output Current (Source or Sink)			
Steady-State	$\pm 500\text{mA}$	$\pm 500\text{mA}$	$\pm 1\text{A}$
Digital Inputs	$-0.3\text{V}-V_{in}$	$-0.3\text{V}-V_{in}$	$-0.3\text{V}-V_{in}$
Power Dissipation at $T_a=25^\circ\text{C}$	1W	1W	3W
Power Dissipation at $T(\text{Case}) = 25^\circ\text{C}$	2W	2W	25W
Operating Junction Temperature	$-55^\circ\text{C}+150^\circ\text{C}$	$-55^\circ\text{C}+150^\circ\text{C}$	$-55^\circ\text{C}+150^\circ\text{C}$
Storage Temperature	$-65^\circ\text{C}+150^\circ\text{C}$	$-65^\circ\text{C}+150^\circ\text{C}$	$-65^\circ\text{C}+150^\circ\text{C}$
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C

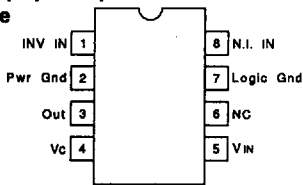
Note 1: All currents are positive into, negative out of the specified terminal.

Note 2: Consult Uniltron Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

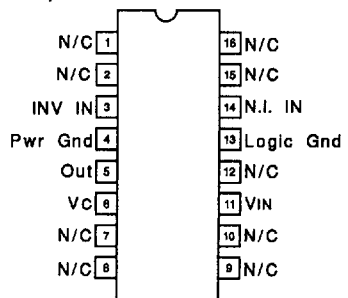
DIL-8 MINIDIP (Top View)

J or N Package



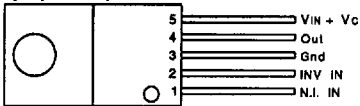
DIL-16 (Top View)

SP Package



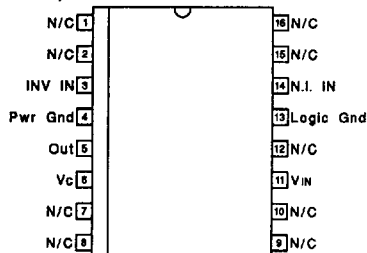
5-Pin TO-220 (Top View)

T Package



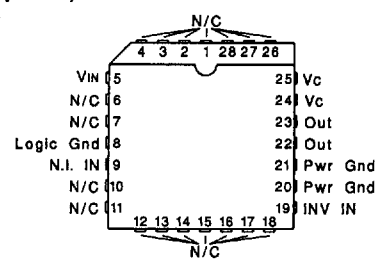
SOIC-16 (Top View)

DW Package



PLCC-28 (Top View)

QP Package



ELECTRICAL CHARACTERISTICS: (Unless otherwise stated, these specifications apply for $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for the UC1710 and $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$ for the UC3710; $V_{in} = V_c = 15\text{V}$, No load $T_A = T_J$.)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{in} Supply Current	$V_{in}=18\text{V}$, $V_c=18\text{V}$, Output Low		26	35	mA
	$V_{in}=18\text{V}$, $V_c=18\text{V}$, Output High		21	30	mA
V_c Supply Current	$V_{in}=18\text{V}$, $V_c=18\text{V}$, Output Low		1.5	5.0	mA
	$V_{in}=18\text{V}$, $V_c=18\text{V}$, Output High		5.0	8	mA
UVLO Threshold	V_{in} High to Low	3.8	4.1	4.4	V
	V_{in} Low to High	4.1	4.4	4.8	V
UVLO Threshold Hysteresis		0.1	0.3	0.5	V
Digital Input Low Level				0.8	V
Digital Input High Level		2.0			V

**ELECTRICAL
CHARACTERISTICS (cont.)**(Unless otherwise stated, these specifications apply for $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ for the UC1710 and $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ for the UC3710; $V_{IN} = V_C = 15\text{V}$, No load. $T_A = T_J$.)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input Current	Digital Input=0.0V	-70	-4.0		μA
Output High Sat., V_{C-V_O}	$I_O = -100\text{mA}$		1.35	2.2	V
	$I_O = -6\text{A}$		3.2	4.5	V
Output Low Sat., V_O	$I_O = 100\text{mA}$		0.25	0.6	V
	$I_O = 6\text{A}$		3.4	4.5	V
Thermal Shutdown			165		$^{\circ}\text{C}$
From Inv., Input to Output (Note 3, 4):					
Rise Time Delay	$C_L = 0$		35	70	ns
	$C_L = 2.2\text{nF}$		35	70	ns
	$C_L = 30\text{nF}$		35	70	ns
10% to 90% Rise	$C_L = 0$		20	40	ns
	$C_L = 2.2\text{nF}$		25	40	ns
	$C_L = 30\text{nF}$		85	150	ns
Fall Time Delay	$C_L = 0$		35	70	ns
	$C_L = 2.2\text{nF}$		35	70	ns
	$C_L = 30\text{nF}$		35	80	ns
90% to 10% Fall	$C_L = 0$		15	40	ns
	$C_L = 2.2\text{nF}$		20	40	ns
	$C_L = 30\text{nF}$		85	150	ns
From N.I. Input to Output (Note 3, 4):					
Rise Time Delay	$C_L = 0$		35	70	ns
	$C_L = 2.2\text{nF}$		35	70	ns
	$C_L = 30\text{nF}$		35	70	ns
10% to 90% Rise	$C_L = 0$		20	40	ns
	$C_L = 2.2\text{nF}$		25	40	ns
	$C_L = 30\text{nF}$		85	150	ns
Fall Time Delay	$C_L = 0$		35	70	ns
	$C_L = 2.2\text{nF}$		35	70	ns
	$C_L = 30\text{nF}$		35	80	ns
90% to 10% Fall	$C_L = 0$		15	40	ns
	$C_L = 2.2\text{nF}$		20	50	ns
	$C_L = 30\text{nF}$		85	150	ns

Note: 3. Delay measured from 50% input change to 10% output change.

Note: 4. Those parameters with $C_L = 30\text{nF}$ are not tested in production.

Note: 5. Inv. Input pulsed at 50% duty cycle with N.I. Input = 3V, or N.I. Input pulsed at 50% duty cycle with Inv. Input = 0V.