

Resonant Fluorescent Lamp Driver

FEATURES

- 1 μ A ICC when Disabled
- PWM Control for LCD Supply
- Zero Voltage Switched (ZVS) on Push-Pull Drivers
- Open Lamp Detect Circuitry
- 4.5V to 20V Operation
- Non-saturating Transformer Topology
- Smooth 100% Duty Cycle on Buck PWM and 0% to 95% on Flyback PWM

DESCRIPTION

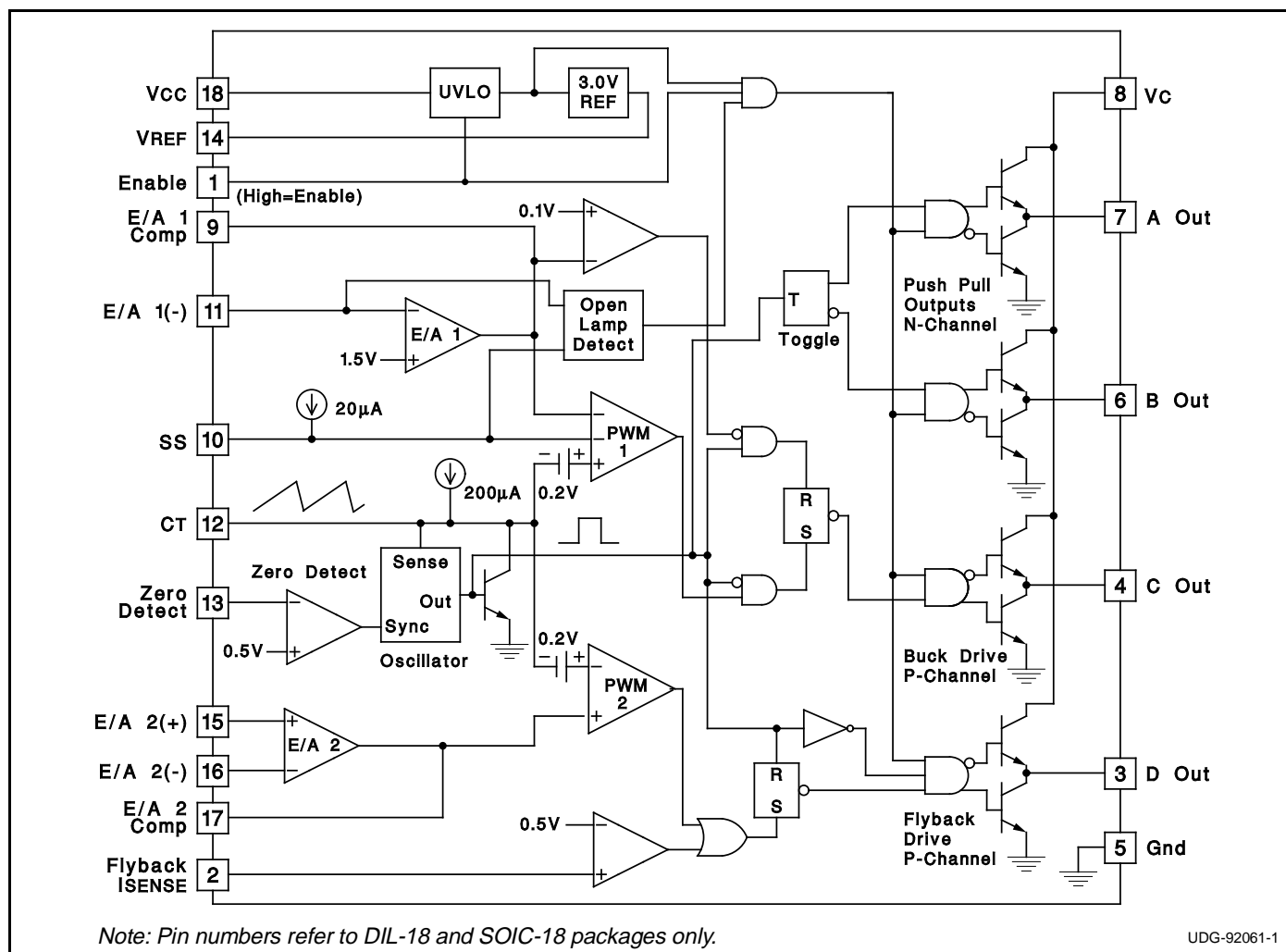
The UC1871 Family of IC's is optimized for highly efficient fluorescent lamp control. An additional PWM controller is integrated on the IC for applications requiring an additional supply, as in LCD displays. When disabled the IC draws only 1 μ A, providing a true disconnect feature, which is optimum for battery powered systems. The switching frequency of all outputs are synchronized to the resonant frequency of the external passive network, which provides Zero Voltage Switching on the Push-Pull drivers.

Soft-Start and open lamp detect circuitry have been incorporated to minimize component stress. An open lamp is detected on the completion of a soft-start cycle.

The Buck controller is optimized for smooth duty cycle control to 100%, while the flyback control ensures a maximum duty cycle of 95%.

Other features include a precision 1% reference, under voltage lockout, flyback current limit, and accurate minimum and maximum frequency control.

BLOCK DIAGRAM



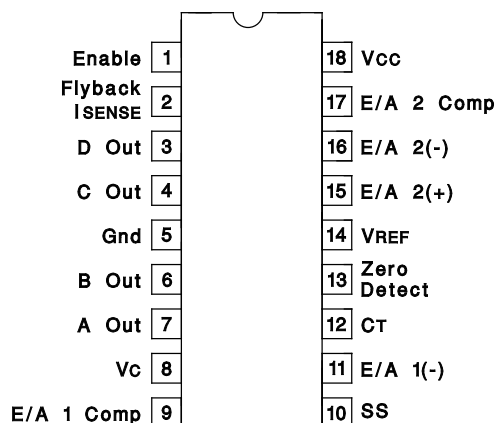
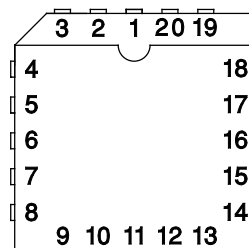
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ABSOLUTE MAXIMUM RATINGS

Analog Inputs	−0.3 to +10V
V _{CC} , V _C Voltage	+20V
Zero Detect Input Current	
High Impedance Source	+10mA
Zero Detect	
Low Impedance Source	+20V
Power Dissipation at T _A = 25°C	1W
Storage Temperature	−65°C to +150°C
Lead Temperature	300°C

Note 1: Currents are positive into, negative out of the specified terminal.

Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS**DIL-18, SOIC-18 (TOP VIEW)****J or N, DW Package****PLCC-20 (Top View)****Q Package****PACKAGE PIN FUNCTION**

FUNCTION	PIN
Gnd	1
B Out	2
A Out	3
V _C	4
E/A 1 Comp	5
SS	6
E/A 1(-)	7
N/C	8
CT	9
Zero Detect	10
N/C	11
VREF	12
E/A 2(+)	13
E/A 2(-)	14
E/A 2 Comp	15
V _{CC}	16
Enable	17
Flyback ISENSE	18
D Out	19
C Out	20

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these parameters apply for T_A = −55°C to +125°C for the UC1871; −25°C to +85°C for the UC2871; 0°C to +70°C for the UC3871; V_{CC} = 5V, V_C = 15V, V_{ENABLE} = 5V, C_T = 1nF, Zero Det = 1V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	T _J =25°C	2.963	3.000	3.037	V
	Overtemp	2.940	3.000	3.060	V
Line Regulation	V _{CC} = 4.75V to 18V			10	mV
Load Regulation	I _o =0 to −5mA			10	mV
Oscillator Section					
Free Running Freq	T _J =25°C	57	68	78	kHz
Max Sync Frequency	T _J =25°C	160	200	240	kHz
Charge Current	V _{CT} = 1.5V	180	200	220	μA
Voltage Stability				2	%
Temperature Stability			4	8	%
Zero Detect Threshold		0.46	0.5	0.56	V
Error Amp 1 Section					
Input Voltage	V _o = 2V	1.445	1.475	1.505	V
Input Bias Current			−0.4	−2	μA
Open Loop Gain	V _o = 0.5 to 3V	65	90		dB
Output High	V _{EA} (-) = 1.3V	3.1	3.5	3.9	V
Output Low	V _{EA} (-) = 1.7V		0.1	0.2	V
Output Source Current	V _{EA} (-) = 1.3V, V _o = 2V	−350	−500		μA
Output Sink Current	V _{EA} (-) = 1.7V, V _o = 2V	10	20		mA
Common Mode Range		0		V _{IN} −1V	V
Unity Gain Bandwidth	T _J = 25°C (Note 4)		1		MHz
Maximum Source Impedance	Note 5			100k	Ω

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated, these parameters apply for TA = -55°C to +125°C for the UC1871; -25°C to +85°C for the UC2871; 0°C to +70°C for the UC3871; VCC = 5V, VC = 15V, VENABLE = 5V, CT = 1nF, Zero Det = 1V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Open Lamp Detect Section					
Soft Start Threshold	VEA(-) = 0V	2.9	3.4	3.8	V
Error Amp Threshold	VSS = 4.2V	0.7	1.0	1.3	V
Soft Start Current	VSS = 2V	10	20	40	μA
Error Amp 2 Section					
Input Offset Voltage	Vo = 2V		0	10	mV
Input Bias Current			-0.2	-1	μA
Input Offset Current				0.5	μA
Open Loop Gain	Vo = 0.5 to 3V	65	90		dB
Output High	VID = 100mV, Vo = 2V	3.6	4	4.4	V
Output Low	VID = -100mV, Vo = 2V		0.1	0.2	V
Output Source Current	VID = 100mV, Vo = 2V	-350	-500		μA
Output Sink Current	VID = -100mV, Vo = 2V	10	20		mA
Common Mode Range		0		VIN-2V	V
Unity Gain Bandwidth	TJ = 25°C (Note 4)		1		MHz
Isense Section					
Threshold		0.475	0.525	0.575	V
Output Section					
Output Low Level	IOUT = 0, Outputs A and B		0.05	0.2	V
	IOUT = 10mA		0.1	0.4	V
	IOUT = 100mA		1.5	2.2	V
Output High Level	IOUT = 0, Outputs C and D	14.7	14.9		V
	IOUT = -10mA	13.5	14.3		V
	IOUT = -100mA	12.5	13.5		V
Rise Time	TJ = 25°C, Cl = 1nF (Note 4)		30	80	ns
Fall Time	TJ = 25°C, Cl = 1nF (Note 4)		30	80	ns
Output Dynamics					
Out A and B Duty Cycle		48	49.9	50	%
Out C Max Duty Cycle	VEA1(-) = 1V	100			%
Out C Min Duty Cycle	VEA1(-) = 2V			0	%
Out D Max Duty Cycle	VEA2(+)- VEA2(-) = 100mV		92	96	%
Out D Min Duty Cycle	VEA2(+)- VEA2(-) = -100mV			0	%
Under Voltage Lockout Section					
Start-Up Threshold		3.7	4.2	4.5	V
Hysteresis		120	200	280	mV
Enable Section					
Input High Threshold		2			V
Input low Threshold				0.8	V
Input Current	VENABLE = 5V		150	400	μA
Supply Current Section					
VCC Supply Current	VCC = 20V		8	14	mA
VC Supply Current	VC=20V		7	12	mA
ICC Disabled	VCC = 20V, VENABLE = 0V		1	10	μA

Note 3: Unless otherwise specified, all voltages are with respect to ground.

Currents are positive into, and negative out of the specified terminal.

Note 4: Guaranteed by design but not 100% tested in production.

Note 5: Impedance below specified maximum guarantees proper operation of the Open Lamp Detect.

TYPICAL APPLICATION

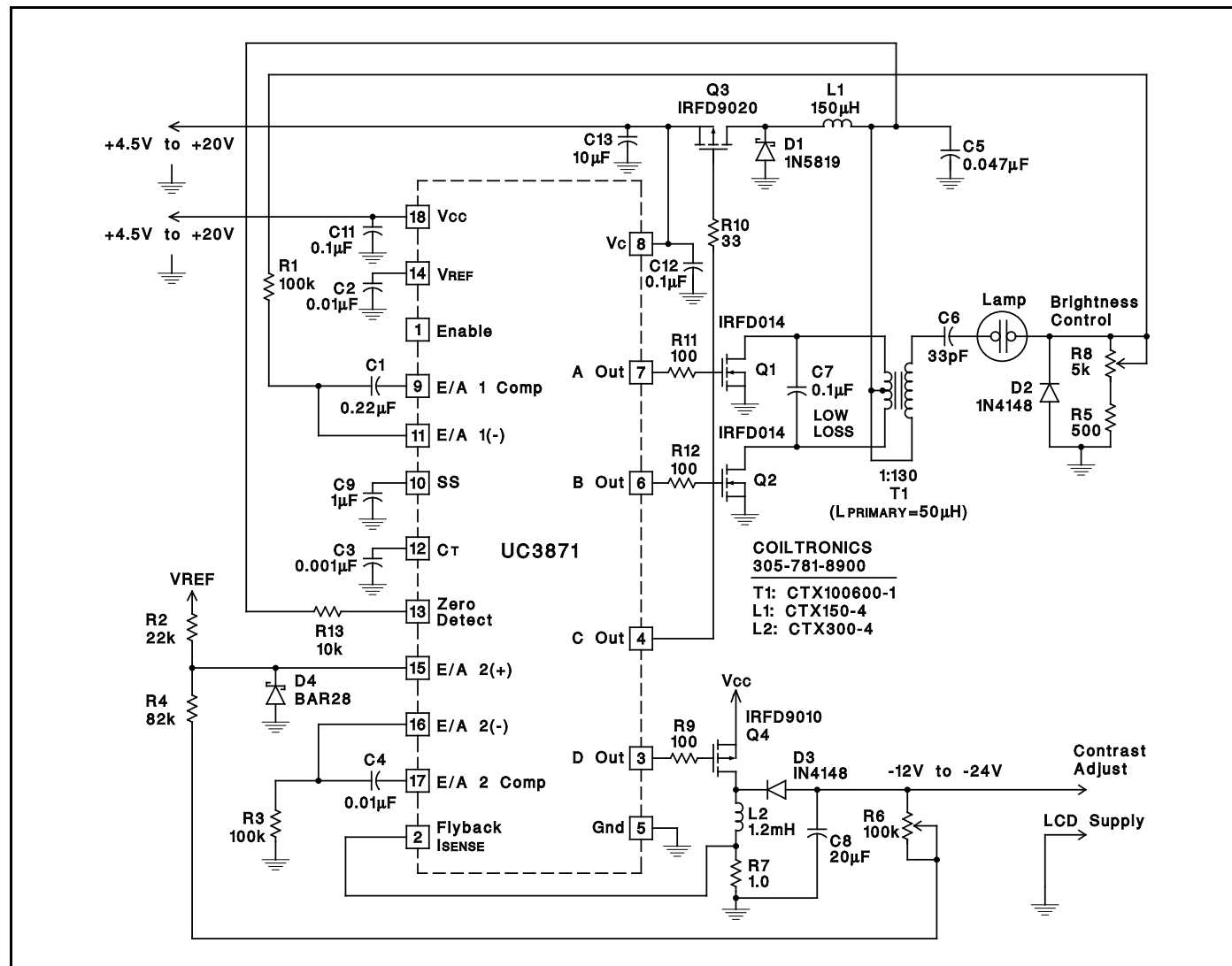


Figure 1

APPLICATION INFORMATION

Figure 1 shows a complete application circuit using the UC3871 Resonant Fluorescent lamp and LCD driver. The IC provides all drive, control and housekeeping functions to implement CCFL and LCD converters. The buck output voltage (transformer center-tap) provides the zero crossing and synchronization signal. The LCD supply modulator is also synchronized to the resonant tank.

The buck modulator drives a P-channel MOSFET directly, and operates over a 0-100% duty-cycle range. The modulation range includes 100%, allowing operation with minimal headroom. The LCD supply modulator also directly drives a P-channel MOSFET, but its duty-cycle is limited to 95% to prevent flyback supply foldback.

The oscillator and synchronization circuitry are shown in Figure 2. The oscillator is designed to synchronize over a 3:1 frequency range. In an actual application however, the frequency range is only about 1.5:1. A zero detect

comparator senses the primary center-tap voltage, generating a synchronization pulse when the resonant waveform falls to zero. The actual threshold is 0.5 volts, providing a small amount of anticipation to offset propagation delay.

The synchronization pulse width is the time that the 4mA current sink takes to discharge the timing capacitor to 0.1 volts. This pulse width sets the LCD supply modulator minimum off time, and also limits the minimum linear control range of the buck modulator. The 200µA current source charges the capacitor to a maximum of 3 volts. A comparator blanks the zero detect signal until the capacitor voltage exceeds 1 volt, preventing multiple synchronization pulse generation and setting the maximum frequency. If the capacitor voltage reaches 3 volts (a zero detection has not occurred) an internal clock pulse is generated to limit the minimum frequency.



Other features are included to minimize external circuitry

UC1871 Open Lamp Detect Circuitry



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