UNITRODE

UC1965
UC2965
UC3965

Precision Reference with Low Offset Error Amplifier

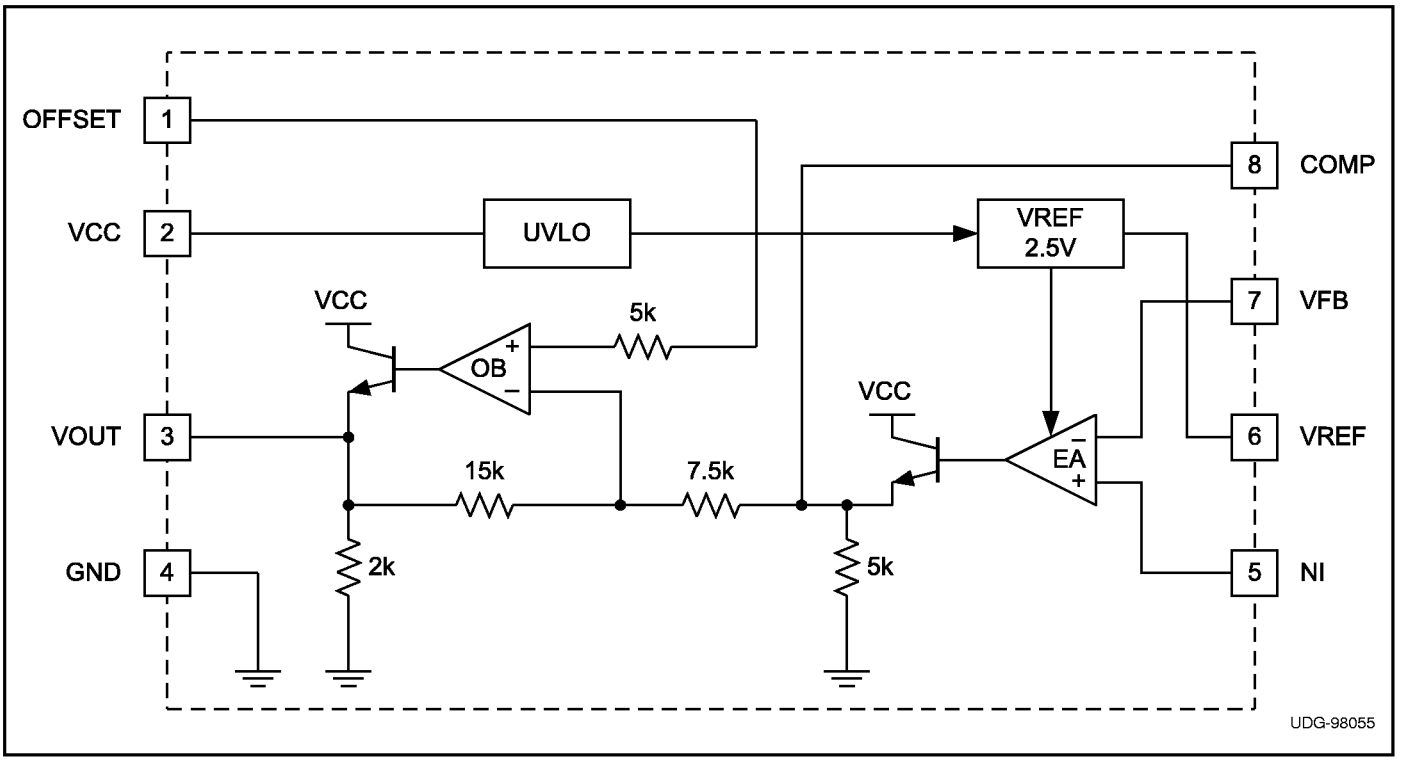
FEATURES

- Accessible 2.5V Precision Reference
- 0.4% Initial Reference Accuracy
- Low 1mV Offset Error Amplifier
- 2X Inverting Amplifier / Buffer Output
- 4.1V Undervoltage Lockout
- ICC 2mA at 5V
- 8-Pin SOIC or DIL Package

DESCRIPTION

The UC3965 includes an accessible 2.5V precision reference, a low offset error amplifier, a 2X inverting amplifier/buffer and an undervoltage lockout circuit. The IC is ideally suited for applications where high precision PWM power supply regulation is required. Typically, the error amplifier is connected to compare a fraction of the "to be regulated" power supply voltage to the on-chip 2.5V reference. The 2X amplifier/buffer output is then used to drive a PWM controller or regulator. The UC3965 is also capable of driving an optocoupler diode for isolated applications.

BLOCK DIAGRAM



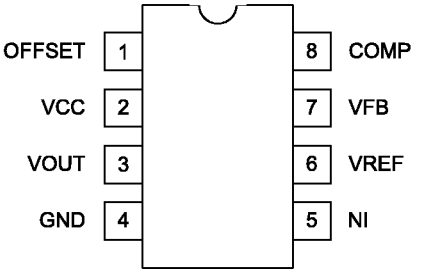
ABSOLUTE MAXIMUM RATINGS

VCC. . . . . –0.3V to 20V
VREF. . . . . –0.3V to 6V
VFB, COMP, NI, VOUT. . . . . –0.3V TO 6V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature. . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.). . . . . +300°C

Currents are positive into, negative out of the specified terminal. All voltages are with respect to ground. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
J or N Package, D Package



ELECTRICAL CHARACTERISTICS Unless otherwise specified, T_A = 0°C to +70°C for the UC3965, –40°C to +85°C for the UC2965 and –55°C to +125°C for the UC1965; VCC = 5V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
General					
VCC		4.3		20	V
Operating Current	VCC = 5V	1.5	2	4	mA
Undervoltage Current				200	µA
Minimum Voltage to Start		3.9	4.1	4.3	V
Hysteresis		200	300	400	mV
VREF					
VREF Initial Accuracy	+25°C	2.49	2.5	2.51	V
VREF Over Temperature	–55°C to +125°C	2.48	2.5	2.52	V
Total Output Variation	Line, Load, Temperature	2.475	2.5	2.525	V
Line Regulation	VCC = 4.3V to 20V		2	10	mV
Load Regulation	0µA to 500µA		2	10	mV
Short Circuit Current	VREF = 0V		2		mA
Error Amplifier					
Input Bias	V_{CM} = 2.5V		200	400	nA
Input Offset Voltage	V_{CM} = 2.5V		1	2	mV
Input Offset Current	V_{CM} = 2.5V	–100	0	100	nA
Gain Bandwidth Product	V_{IN} = 50mV P-P (Note 1)		6		MHz
Open Loop Gain	VOUT = 1V to 3.75V	80	100		dB
Output Low Level	I_{OUT} = 0µA		0.8		V
	I_{OUT} = 100µA		1.2		V
Output High Level	I_{OUT} = 0µA		4		V
	I_{OUT} = –500µA		4		V
Short Circuit Circuit	V_{COMP} = 0V		8		mA
CMRR	V_{CM} = 1.25V to 3.75V	70	100		dB
PSRR	VCC = 4.3V to 20V	70	100		dB
Rising Slew Rate			2		V/µs
Falling Slew Rate			0.4		V/µs

ELECTRICAL CHARACTERISTICS Unless otherwise specified, T_A = 0°C to +70°C for the UC3965, –40°C to +85°C for the UC2965 and –55°C to +125°C for the UC1965; VCC = 5V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Inverting Buffer Amplifier					
Input Bias	V_{CM} = 2.5V		1	2	µA
Output Offset Voltage	V_{CM} = 2.5V	–20	0	20	mV
Gain Bandwidth Product	V_{IN} = 50mV P-P (Note 1)		1.5		MHz
Closed Loop Gain	Inverting Gain	–2.04	–2	–1.96	V/V
Output Low Level	I_{OUT} = 0µA		0.3		V
	I_{OUT} = 100µA		0.5		V
Output High Level	I_{OUT} = 0mA		4		V
	I_{OUT} = –4mA		4		V
Short Circuit Circuit	VOUT = 0V		18		mA
CMRR	V_{CM} = 1.25V to 3.75V	70	100		dB
PSRR	VCC = 4.3V to 20V	70	100		dB
Rising Slew Rate			0.9		V/µs
Falling Slew Rate			0.9		V/µs

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

COMP: Error amplifier output.

GND: Ground.

NI: Error amplifier non-inverting input.

OFFSET: Inverting buffer non-inverting input.

VCC: VCC supply and UVLO input.

VFB: Error amplifier inverting input.

VOUT: Inverting buffer output.

VREF: VREF output.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

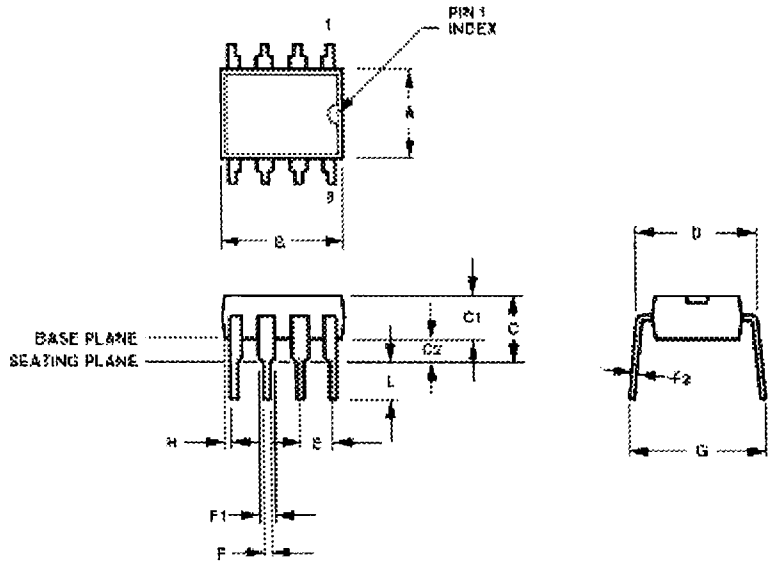
UNITRODE

Mechanical Drawings

Back to Packaging Index

8-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.320	.400	9.40	10.16	1
C	-	.210	-	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	-	0.13	-	
L	.115	.160	2.92	4.06	



NOTES:

1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

P-1

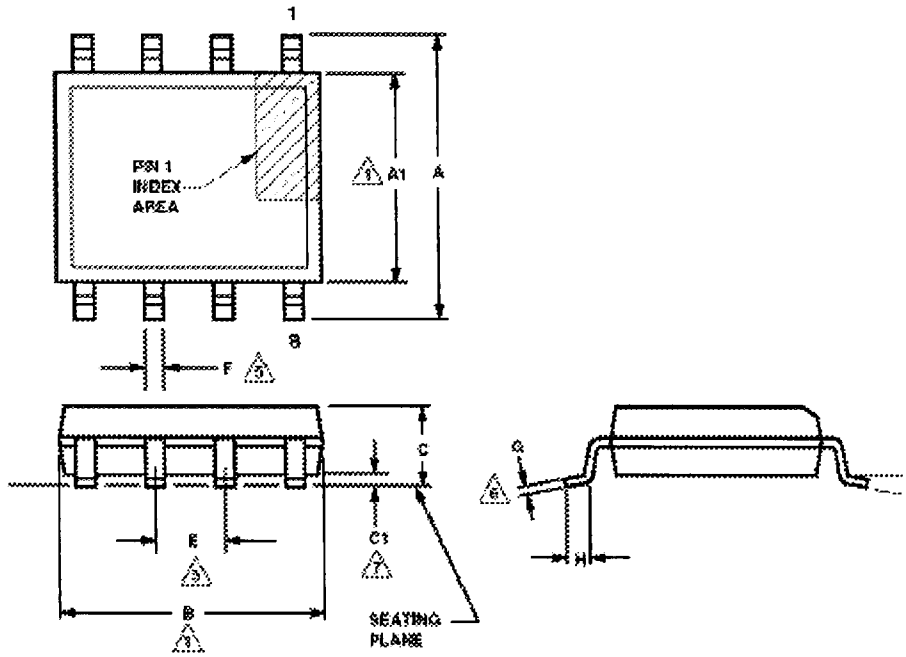
UNITRODE

Mechanical Drawings

Back to Packaging Index

8-PIN SOIC SURFACE MOUNT~ D, DP PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.189	.196	4.80	4.98
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.23
E	.050 BSC		1.27 BSC	
F	.014	.019	0.35	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°



NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

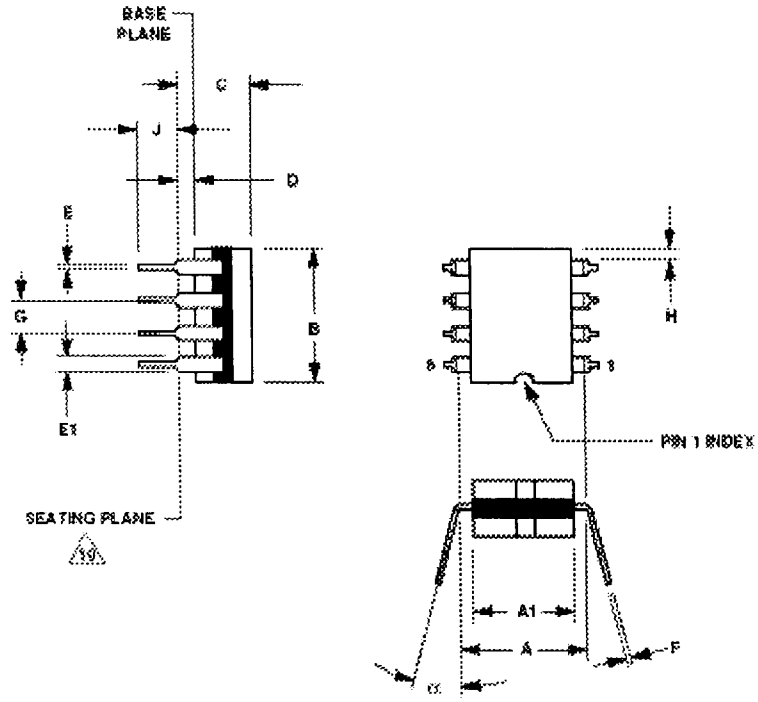
UNITRODE

Mechanical Drawings

Back to Packaging Index

8-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	-	0.405	-	10.29	4
C	-	0.200	-	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	-	0.13	-	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	



NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION 'E1' MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 4, 5 AND 8 ONLY.
3. DIMENSION 'D' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 4, 5 AND 8).
7. DIMENSION 'A' SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS 'E' AND 'F' SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.