32 Line VME Bus Bias Generator

FEATURES

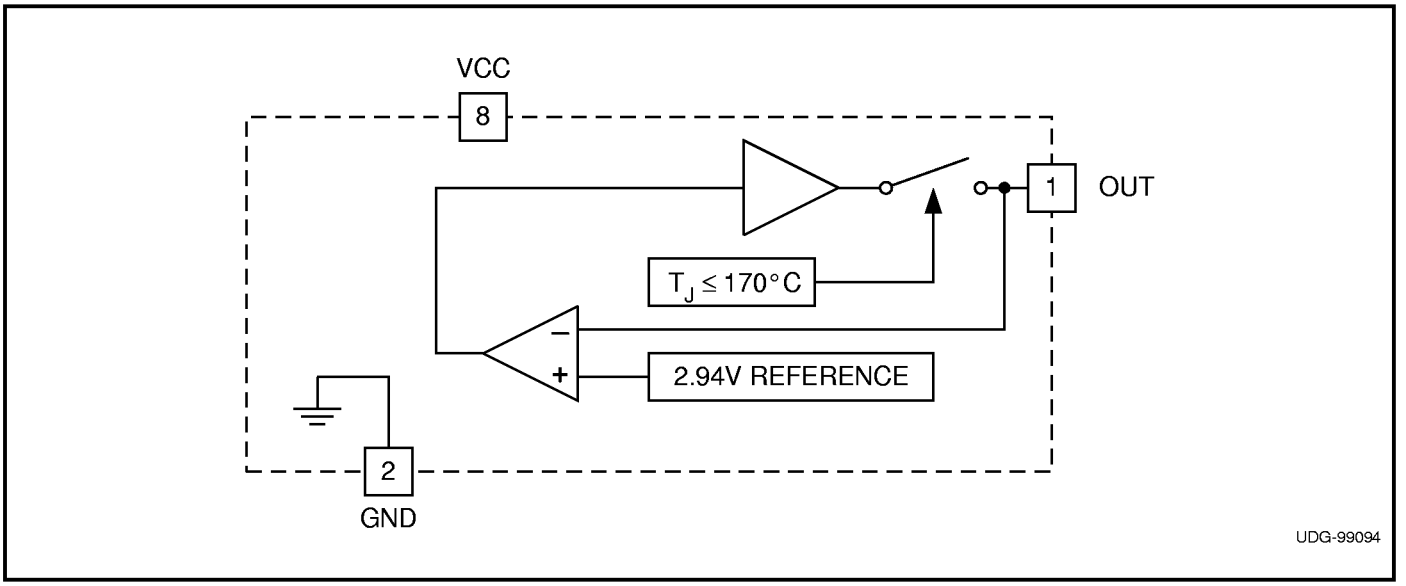
- Complies with VME64 Standard
- 2.94V Regulated Output Voltage With 1% Tolerance at 25°C
- Provides Bias for up to 32 Lines of Active Termination for VME busses
- –575mA Sourcing Current for Termination
- +475mA Sinking Current for Active Negation Drivers
- Current Limit and Thermal Shutdown Protection
- Low Thermal Resistance Surface Mount Packages

DESCRIPTION

The VME bus bias generator provides current for up to 32 lines of active termination for a VME64 parallel bus. The VME standards require termination at both ends of the bus. The voltage regulator and internal logic circuits of these parts provide all the functionality and performance necessary to bias termination resistors for the VME Bus. The VME bus bias generator sink current maintains regulation with all active negation drivers negated. Internal circuit trimming is used to trim the output voltage to a 1% tolerance. Other features include thermal shutdown and current limit for short circuit conditions. This device is available in low thermal resistance versions of the industry standard 8-pin power SOIC, 3 pin TO-220 and 3 pin TO-263.

Termination is a VME requirement but passive is also an option.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

VCC . . . . . +7V
Regulator Output Current 600mA
Storage Temperature . . . . . -65°C to +150°C
Junction Temperature . . . . . -55°C to +150°C
Lead Temperature (Soldering, 10 secretary.) . . . . . +300°C

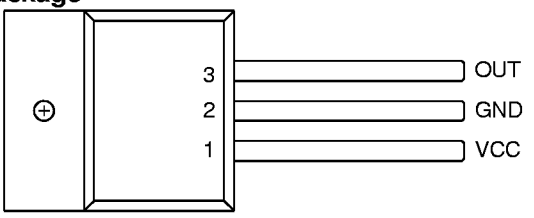
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to ground.

RECOMMENDED OPERATING CONDITIONS

VCC Voltage . . . . . 4.875V to 5.25V

TO220-3 (Top View)

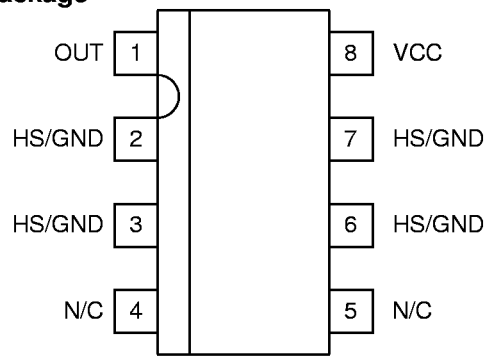
T Package



CONNECTION DIAGRAMS

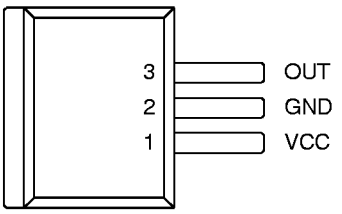
SOIC-8 (Top View)

DP Package



TO263-3 (Top View)

TD Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C, V_{CC} = 5.00V; C_{OUT} = 4.7µF; T_A = T_J

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Supply Current	No load		25		mA
	I_{OUT} = –600mA		602	650	mA
Regulator Section					
Output Voltage	25°C, No load	2.793	2.94	3.087	V
Load Regulation	–575mA ≤ I_{OUT} ≤ 475mA (Note 1)		25	30	mV
Line Regulation	4.875V ≤ V_{CC} ≤ 5.25V, No load		10	20	mV
Short Circuit Current	V_{OUT} = 0V			–600	mA
	V_{OUT} = 3.5V	500			
Thermal Shutdown	(Note 2)		170		°C
Thermal Shutdown Hysteresis	(Note 2)		10		°C

Note 1: Tested at a constant junction temperature by low duty cycle pulse testing.

Note 2: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

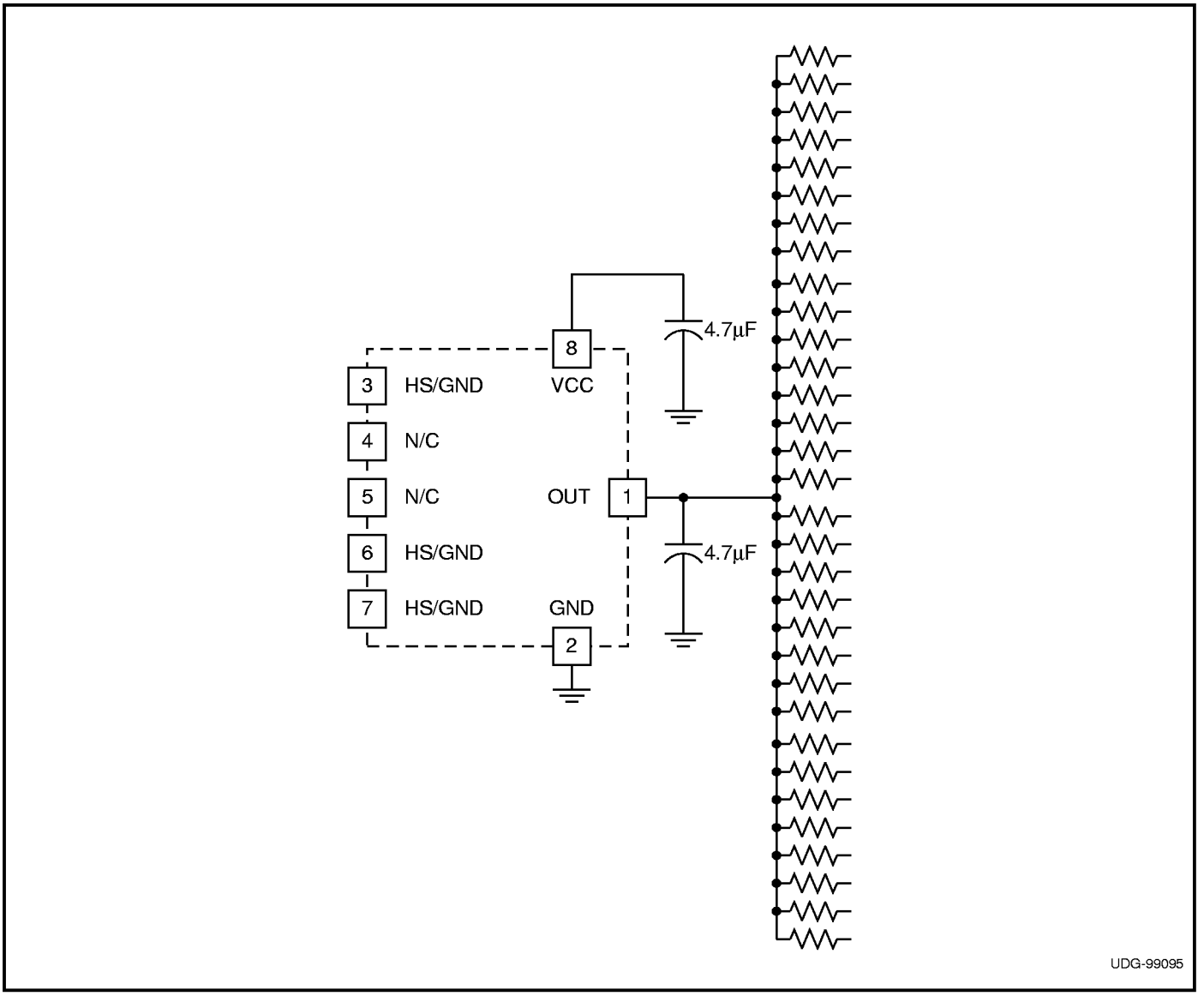
GND: Ground pin.

HS/GND: Heat sink GND. Connect to large area PC board traces to increase power dissipation capability.

OUT: 2.94V regulated output voltage pin. The part is internally current limited for both sinking and sourcing current to prevent damage. For best performance, a 4.7µF low ESR capacitor is recommended.

VCC: Supply voltage pin. The pin should be de-coupled with at least a 2.2µF low ESR capacitor. For best performance, a 4.7µF low ESR capacitor is recommended. Lead lengths should be kept at a minimum.

TYPICAL APPLICATION



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