UNITRODE

Economy Primary Side Controller

UCC1809-1/-2
UCC2809-1/-2
UCC3809-1/-2

FEATURES

- User Programmable Soft Start With Active Low Shutdown
- User Programmable Maximum Duty Cycle
- Accessible 5V Reference
- Undervoltage Lockout
- Operation to 1MHz
- 0.4A Source/0.8A Sink FET Driver
- Low 100µA Startup Current

PART NUMBER	TURN ON THRESHOLD	TURN OFF THRESHOLD
UCCX809-1	10V	8V
UCCX809-2	15V	8V

DESCRIPTION

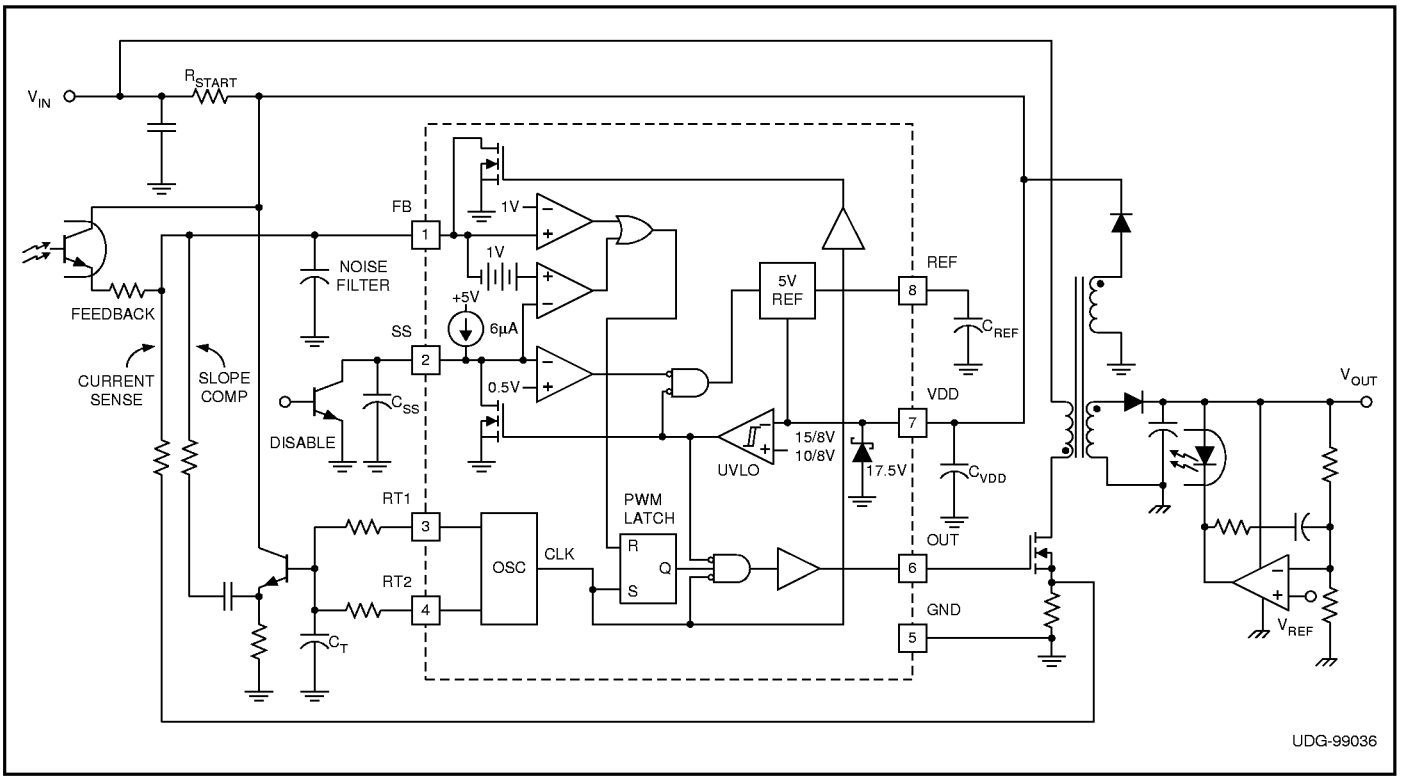
The UCC3809 family of BCDMOS economy low power integrated circuits contains all the control and drive circuitry required for off-line and isolated DC-to-DC fixed frequency current mode switching power supplies with minimal external parts count. Internally implemented circuits include undervoltage lockout featuring startup current less than 100µA, a user accessible voltage reference, logic to ensure latched operation, a PWM comparator, and a totem pole output stage to sink or source peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off state.

Oscillator frequency and maximum duty cycle are programmed with two resistors and a capacitor. The UCC3809 family also features full cycle soft start.

The family has UVLO thresholds and hysteresis levels for off-line and DC-to-DC systems as shown in the table to the left.

The UCC3809 and the UCC2809 are offered in the 8 pin SOIC (D), PDIP (N), TSSOP (PW), and MSOP (P) packages. The small TSSOP and MSOP packages make the device ideal for applications where board space and height are at a premium.

TYPICAL APPLICATION DIAGRAM



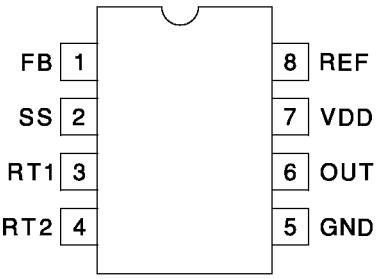
ABSOLUTE MAXIMUM RATINGS

VDD 19V
I_{VDD} 25mA
I_{OUT} (tpw < 1µs and Duty Cycle < 10%) . . . . . –0.4A to 0.8A
RT1, RT2, SS . . . . . –0.3V to REF + 0.3V
I_{REF} . . . . . –15mA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

All voltages are with respect to ground unless otherwise stated. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

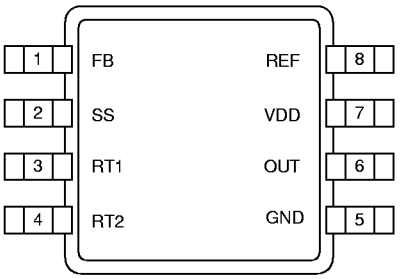
CONNECTION DIAGRAM

SOIC-8, DIL-8 (Top View)
D, N and J Packages



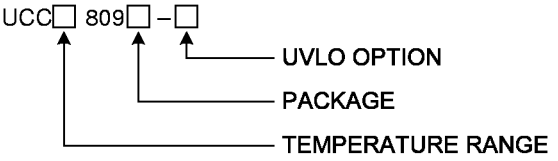
TSSOP-8 (Top View)
PW Package

MSOP-8 (Top View)
P Package



	Temperature Range	Available Packages
UCC1809-X	–55°C to +125°C	J
UCC2809-X	–40°C to +85°C	N, D, P, PW
UCC3809-X	0°C to +70°C	N, D, P, PW

ORDERING INFORMATION



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VDD = 12V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Section					
VDD Clamp	I_{VDD} = 10mA	16	17.5	19	V
I_{VDD}	No Load		600	900	µA
I_{VDD} Starting				100	µA
Undervoltage Lockout Section					
Start Threshold (UCCx809-1)		9.4		10.4	V
UVLO Hysteresis (UCCx809-1)		1.65			V
Start Threshold (UCCx809-2)		14.0		15.6	V
UVLO Hysteresis (UCCx809-2)		6.2			V
Voltage Reference Section					
Output Voltage	I_{REF} = 0mA	4.75	5	5.25	V
Line Regulation	VDD = 10V to 15V		2		mV
Load Regulation	I_{REF} = 0mA to 5mA		2		mV
Comparator Section					
I_{FB}	Output Off		–100		nA
Comparator Threshold		0.9	0.95	1	V
OUT Propagation Delay (No Load)	V_{FB} = 0.8V to 1.2V at T_R = 10ns		50	100	ns

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VDD = 12V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Soft Start Section					
I_{SS}	VDD = 16V, V_{SS} = 0V	–3	–6	–16	µA
V_{SS} Low	VDD = 7.5V, I_{SS} = 200µA			0.2	V
Shutdown Threshold		0.44	0.48	0.52	V
Oscillator Section					
Frequency	RT1 = 10k, RT2 = 4.32k, CT = 820pF	90	100	110	kHz
Frequency Change with Voltage	VDD = 10V to 15V		0.1		%/V
C_T Peak Voltage			3.33		V
C_T Valley Voltage			1.67		V
C_T Peak to Peak Voltage		1.54	1.67	1.80	V
Output Section					
Output V_{SAT} Low	I_{OUT} = 80mA (dc)		0.8	1.5	V
Output V_{SAT} High	I_{OUT} = –40mA (dc), VDD – OUT		0.8	1.5	V
Output Low Voltage During UVLO	I_{OUT} = 20mA (dc)			1.5	V
Minimum Duty Cycle	V_{FB} = 2V		0		%
Maximum Duty Cycle			70		%
Rise Time	C_{OUT} = 1nF		35		ns
Fall Time	C_{OUT} = 1nF		18		ns

PIN DESCRIPTIONS

FB: This pin is the summing node for current sense feedback, voltage sense feedback (by optocoupler) and slope compensation. Slope compensation is derived from the rising voltage at the timing capacitor and can be buffered with an external small signal NPN transistor. External high frequency filter capacitance applied from this node to GND is discharged by an internal 250Ω on resistance NMOS FET during PWM off time and offers effective leading edge blanking set by the RC time constant of the feedback resistance from current sense resistor to FB input and the high frequency filter capacitor capacitance at this node to GND.

GND: Reference ground and power ground for all functions.

OUT: This pin is the high current power driver output.

REF: The internal 5V reference output. This reference is buffered and is available on the REF pin. REF should be bypassed with a 0.47µF ceramic capacitor.

RT1: This pin connects to timing resistor RT1 and controls the positive ramp time of the internal oscillator (Tr = 0.74 • (C_T + 27pF) • RT1). The positive threshold of the internal oscillator is sensed through inactive timing resistor RT2 which connects to pin RT2 and timing capacitor C_T.

RT2: This pin connects to timing resistor RT2 and controls the negative ramp time of the internal oscillator (Tf = 0.74 • (C_T + 27pF) • RT2). The negative threshold of the internal oscillator is sensed through inactive timing resistor RT1 which connects to pin RT1 and timing capacitor C_T.

SS: This pin serves two functions. The soft start timing capacitor connects to SS and is charged by an internal 6µA current source. Under normal soft start SS is discharged to at least 0.4V and then ramps positive to 1V during which time the output driver is held low. As SS charges from 1V to 2V soft start is implemented by an increasing output duty cycle. If SS is taken below 0.5V, the output driver is inhibited and held low. The user accessible 5V voltage reference also goes low and I_{VDD} < 100µA.

VDD: The power input connection for this device. This pin is shunt regulated at 17.5V which is sufficiently below the voltage rating of the DMOS output driver stage. VDD should be bypassed with a 1µF ceramic capacitor.

APPLICATION INFORMATION

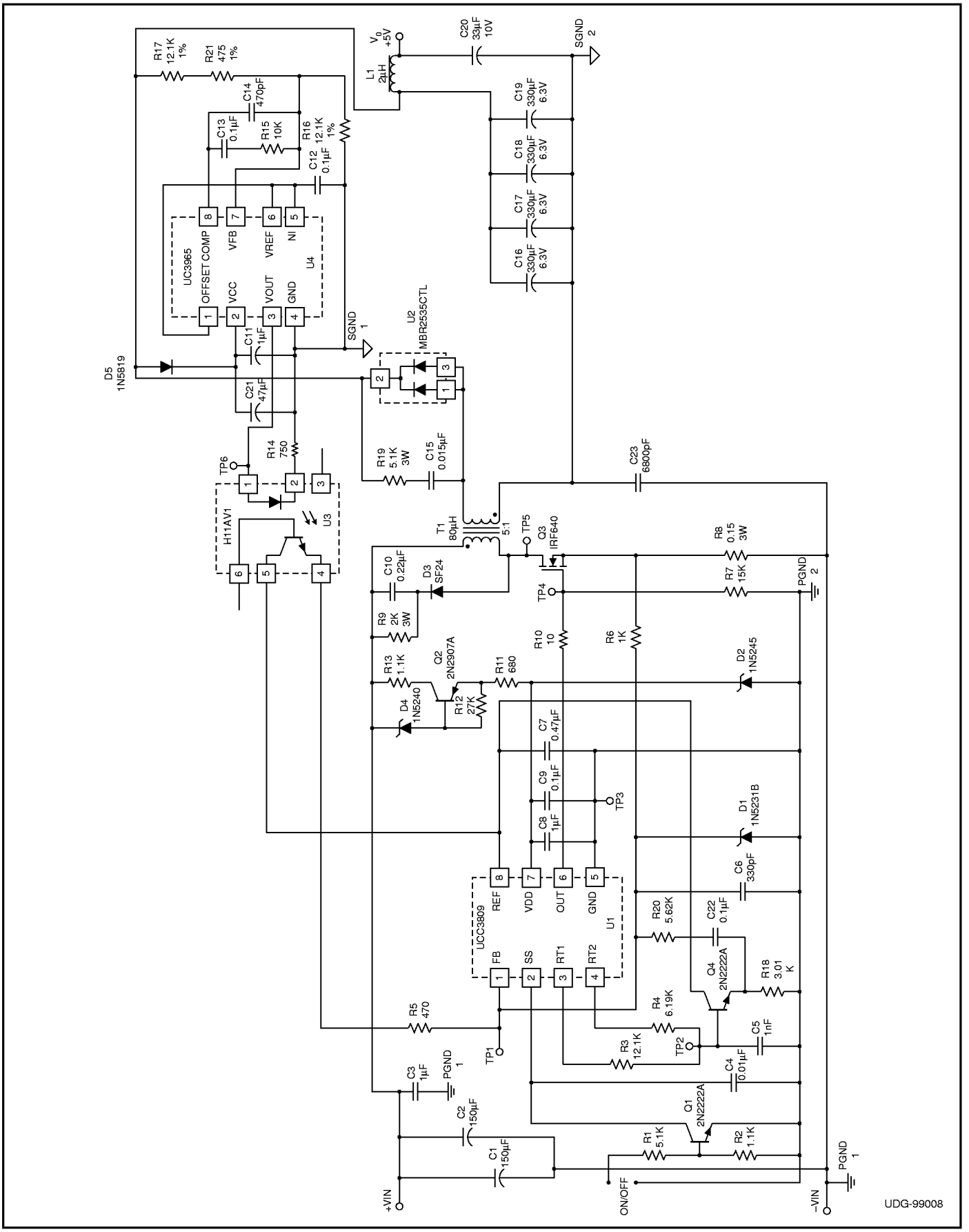


Figure 1. Detailed application diagram: –48V to +5V flyback converter.

APPLICATION INFORMATION (cont.)

The Typical Application Diagram shows an isolated flyback converter utilizing the UCC3809. Note that the capacitors C_{REF} and C_{VDD} are local decoupling capacitors for the reference and IC input voltage, respectively. Both capacitors should be low ESR and ESL ceramic, placed as close to the IC pins as possible, and returned directly to the ground pin of the chip for best stability. REF provides the internal bias to many of the IC functions and C_{REF} should be at least 0.47µF to prevent REF from drooping.

FB Pin

The basic premise of the UCC3809 is that the voltage sense feedback signal originates from an optocoupler that is modulated by an external error amplifier located on the secondary side. This signal is summed with the current sense signal and any slope compensation at the FB pin and compared to a 1V threshold, as shown in the Typical Application Diagram. Crossing this 1V threshold resets the PWM latch and modulates the output driver on-time much like the current sense comparator used in the UC3842. In the absence of a FB signal, the output will follow the programmed maximum on-time of the oscillator.

When adding slope compensation, it is important to use a small capacitor to AC couple the oscillator waveform before summing this signal into the FB pin. By correctly selecting the emitter resistor of the optocoupler, the voltage sense signal can force the FB node to exceed the 1V threshold when the output that is being compared exceeds a desired level. Doing so drives the UCC3809 to zero percent duty cycle.

Oscillator

The following equation sets the oscillator frequency:

$$F_{OSC} = \left[0.74 \bullet (CT + 27pF) \bullet (RT1 + RT2)\right]^{-1}$$

$$D_{MAX} = 0.74 \bullet RT1 \bullet (CT + 27pF) \bullet F_{OSC}$$

Referring to Figure 2 and the waveforms in Figure 3, when Q1is on, CT charges via the $R_{DS(on)}$ of Q1 and RT1. During this charging process, the voltage of CT is sensed through RT2. The S input of the oscillator latch, S(OSC), is level sensitive, so crossing the upper threshold (set at 2/3 VREF or 3.33V for a typical 5.0V reference) sets the Q output (CLK signal) of the oscillator latch high. A high CLK signal results in turning off Q1 and turning on Q2. CT now discharges through RT2 and the $R_{DS(on)}$ of Q2. CT discharges from 3.33V to the lower threshold (set at 1/3 VREF or 1.67V for a typical 5.0V reference) sensed through RT1. The R input to the oscillator latch, R(OSC), is also level sensitive and resets the CLK signal low when CT crosses the 1.67V threshold, turning off Q2 and turning on Q1, initiating another charging cycle.

Figure 3 shows the waveforms associated with the oscillator latch and the PWM latch (shown in the Typical Application Diagram). A high CLK signal not only initiates a discharge cycle for CT, it also turns on the internal NMOS FET on the FB pin causing any external capacitance used for leading edge blanking connected to this pin to be discharged to ground. By discharging any external capacitor completely to ground during the external switch's off-time, the noise immunity of the converter is enhanced allowing the user to design in smaller RC components for leading edge blanking. A high CLK signal also sets the level sensitive S input of the PWM latch, S(PWM), high, resulting in a high output, Q(PWM), as shown in Figure 3. This Q(PWM) signal will remain high until a reset signal, R(PWM) is received. A high R(PWM) signal results from the FB signal crossing the 1V threshold, or during soft start or if the SS pin is disabled.

Assuming the UVLO threshold is satisfied, the OUT signal of the IC will be high as long as Q(PWM) is high and S(PWM), also referred to as CLK, is low. The OUT signal will be dominated by the FB signal as long as the FB signal trips the 1V threshold while CLK is low. If the FB signal does not cross the 1V threshold while CLK is low, the OUT signal will be dominated by the maximum duty cycle programmed by the user. Figure 3 illustrates the various waveforms for a design set up for a maximum duty cycle of 70%.

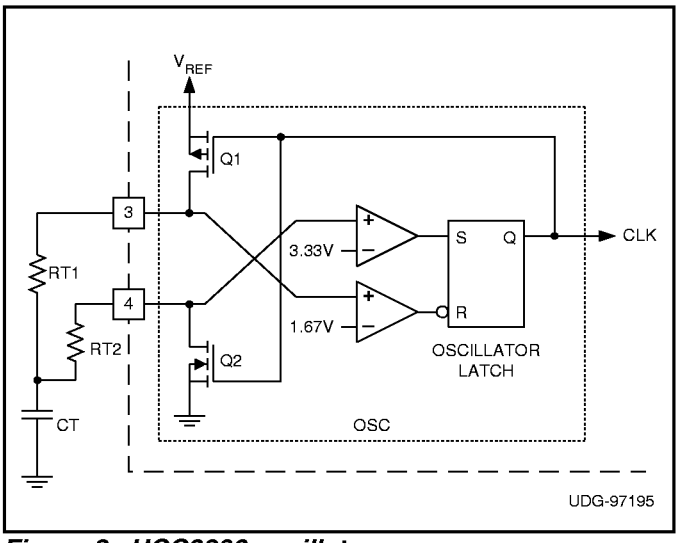


Figure 2. UCC3809 oscillator.

APPLICATION INFORMATION (cont.)

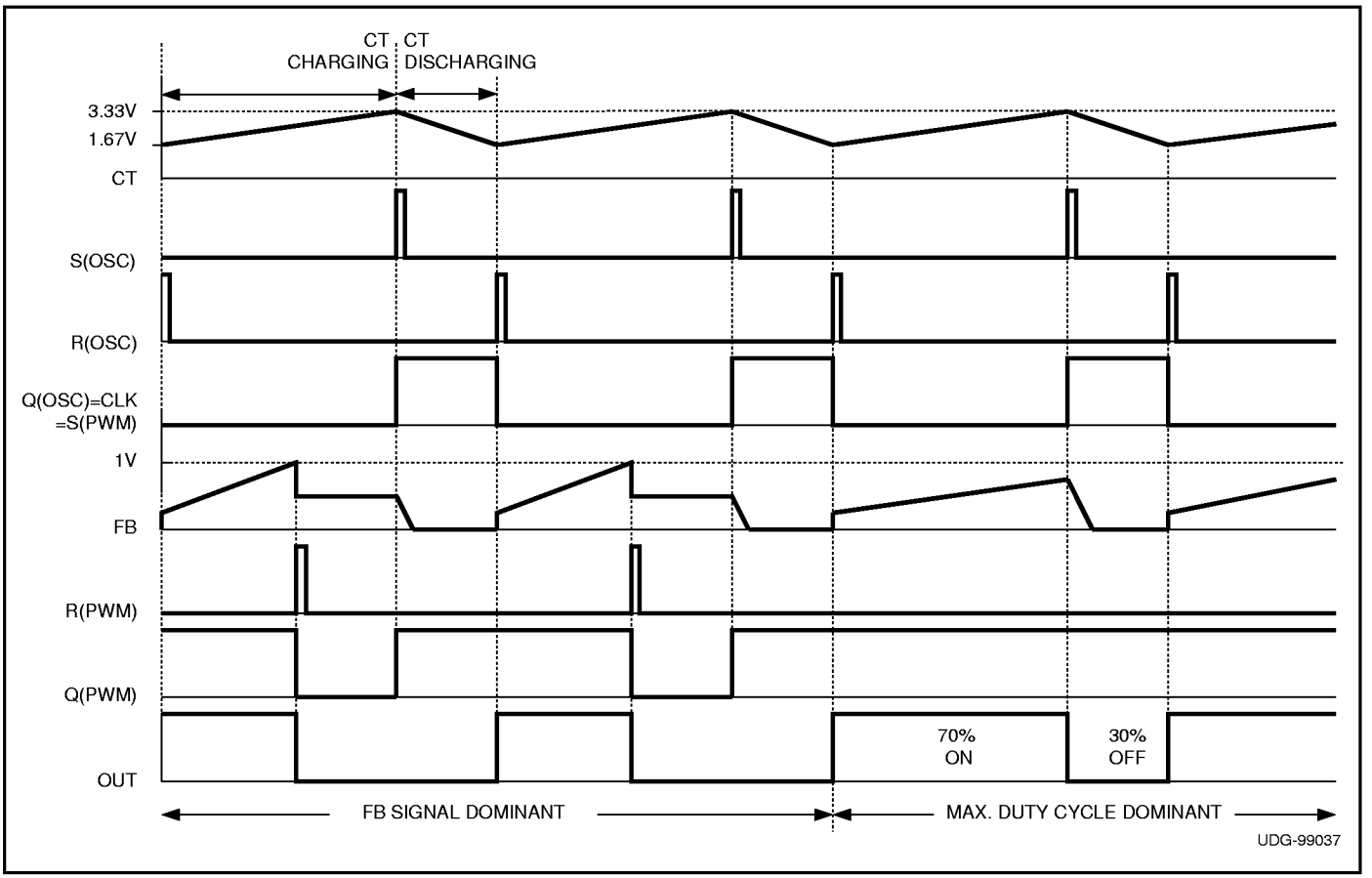


Figure 3. Waveforms associated with the oscillator latch and the PWM latch.

The recommended value for CT is 1nF for frequencies in the 100 kHz or less range and smaller CT for higher frequencies. The minimum recommended values of RT1 and RT2 are 10kΩ and 4.32kΩ, respectively. Using these values maintains a ratio of at least 20:1 between the $R_{DS(on)}$ of the internal FETs and the external timing resistors, resulting in minimal change in frequency over temperature. Because of the oscillator's susceptibility to capacitive coupling, examine the oscillator frequency by looking at the common RT1-RT2-CT node on the circuit board as opposed to looking at pins 3 and 4 directly. For good noise immunity, RT1 and RT2 should be placed as close to pins 3 and 4 of the IC as possible. CT should be returned directly to the ground pin of the IC with minimal stray inductance and capacitance.

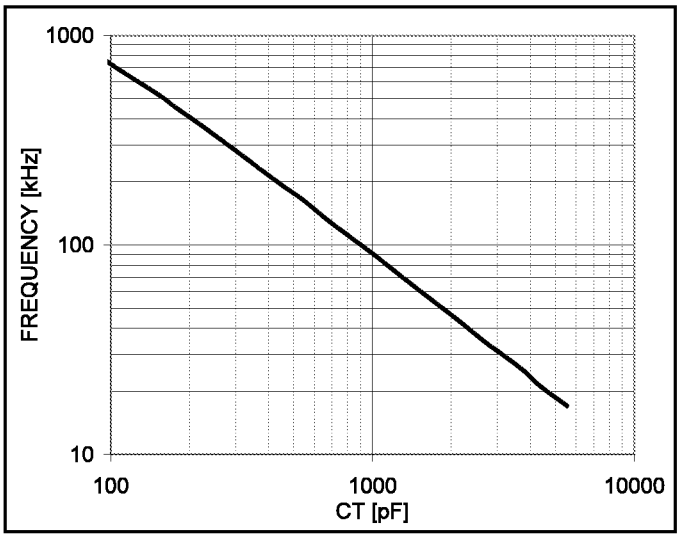


Figure 4. Oscillator frequency vs. C_T (RT1 = 10k, RT2 = 4.32k)

APPLICATION INFORMATION (cont.)

Synchronization

Both of the synchronization schemes shown in Figure 5 can be successfully implemented with the internal oscillator of the UCC3809. Both schemes allow access to the timing ramp needed for slope compensation and have minimal impact on the programmed maximum duty cycle. In the absence of a sync pulse, the PWM controller will run independently at the frequency set by RT1, RT2, and CT. This free running frequency must be approximately 15 to 20% lower than the sync pulse frequency to insure the free running oscillator does not cross the comparator threshold before the desired sync pulse.

Option I uses the synchronization pulse to pull pin 3 low, triggering the internal 1.67V comparator to reset the RS latch and initiate a charging cycle. The valley voltage of the CT waveform is higher when synchronized using this configuration, decreasing the ramp charge and discharge times, thereby increasing the operating frequency; otherwise the overall shape of the CT voltage waveform is unchanged.

Option II uses the synchronization pulse to superimpose the sync voltage onto the peak of the CT waveform. This triggers the internal 3.33V comparator, initiating a discharge cycle. The sync pulse is summed with the free running oscillator waveform at the CT node, resulting in a spike on top of the CT peak voltage.

ADDITIONAL INFORMATION

Please refer to the following Unitrode application topics for additional information.

[1] Application Note U-165, *Design Review: Isolated 50W Flyback Converter with the UCC3809 Primary Side Controller and the UC3965 Precision Reference and Error Amplifier* by Lisa Dinwoodie.

[2] Design Note DN-89, *Comparing the UC3842, UCC3802, and UCC3809 Primary Side PWM Controllers* by Lisa Dinwoodie.

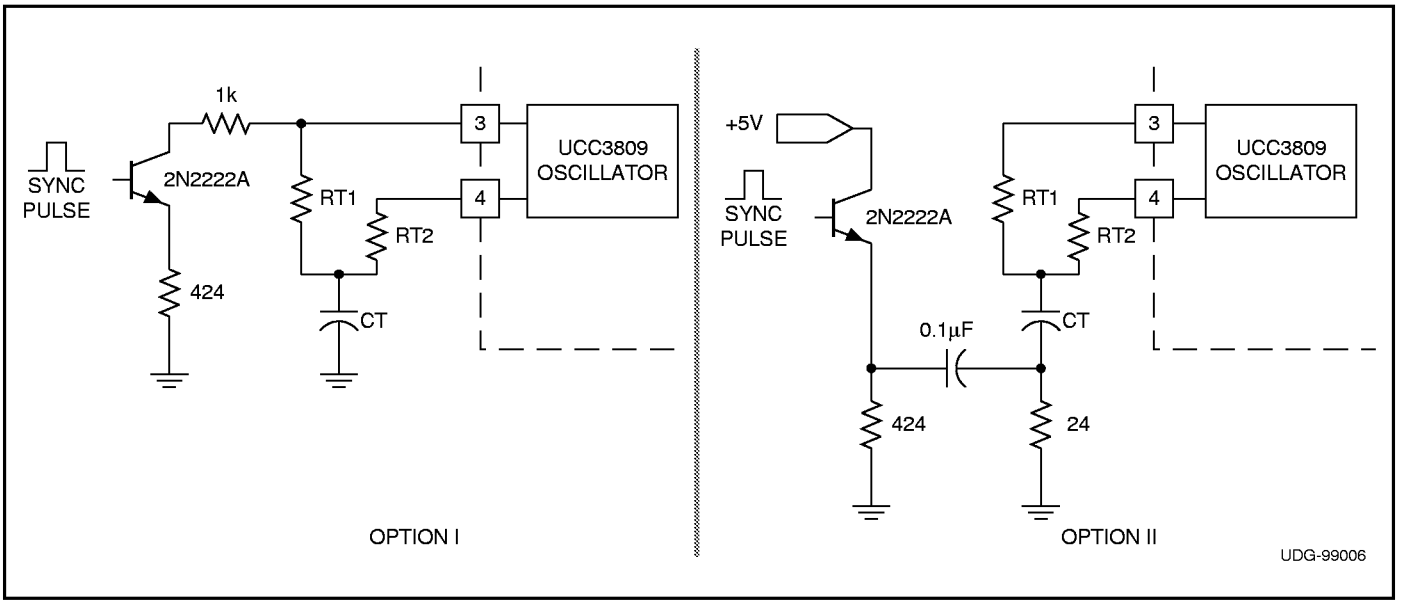


Figure 5. UCC3809 synchronization options.

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Mechanical Drawings

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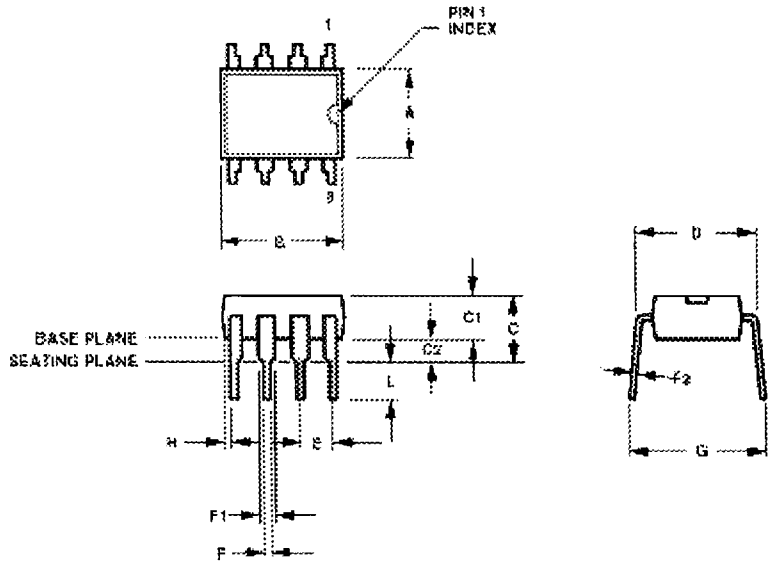
8-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.320	.400	9.40	10.16	1
C	-	.210	-	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	-	0.13	-	
L	.115	.160	2.92	4.06	



NOTES:

1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

P-1

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Mechanical Drawings

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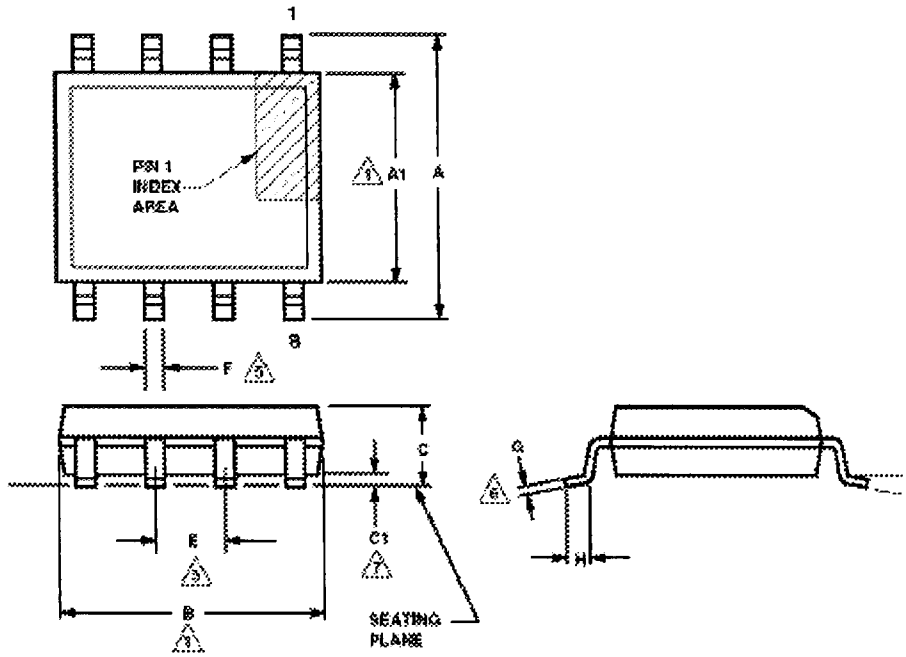
8-PIN SOIC SURFACE MOUNT~ D, DP PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.189	.196	4.80	4.98
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.23
E	.050 BSC		1.27 BSC	
F	.014	.019	0.35	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°



NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

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Mechanical Drawings

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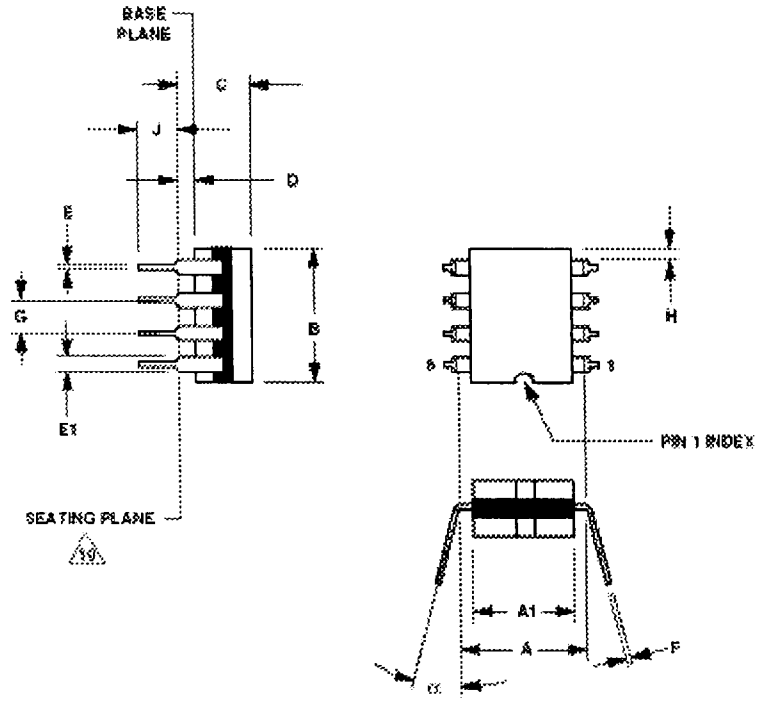
8-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	-	0.405	-	10.29	4
C	-	0.200	-	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	-	0.13	-	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	



NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION 'E1' MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 4, 5 AND 8 ONLY.
3. DIMENSION 'D' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 4, 5 AND 8).
7. DIMENSION 'A' SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS 'E' AND 'F' SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.