5-Bit Microprocessor Power Supply Controller

FEATURES

- 5-Bit Digital-to-Analog Converter (DAC)
- Supports 4-Bit and 5-Bit Microprocessor VID Codes
- Combined DAC/Voltage Monitor and PWM Functions
- 1% DAC/Reference
- Current Sharing
- 100kHz, 200kHz, 400kHz Oscillator Frequency Options
- Foldback Current Limiting
- Overvoltage and Undervoltage Fault Windows
- Undervoltage Lockout
- 4Ω Totem Pole Output
- Chip Disable Function

DESCRIPTION

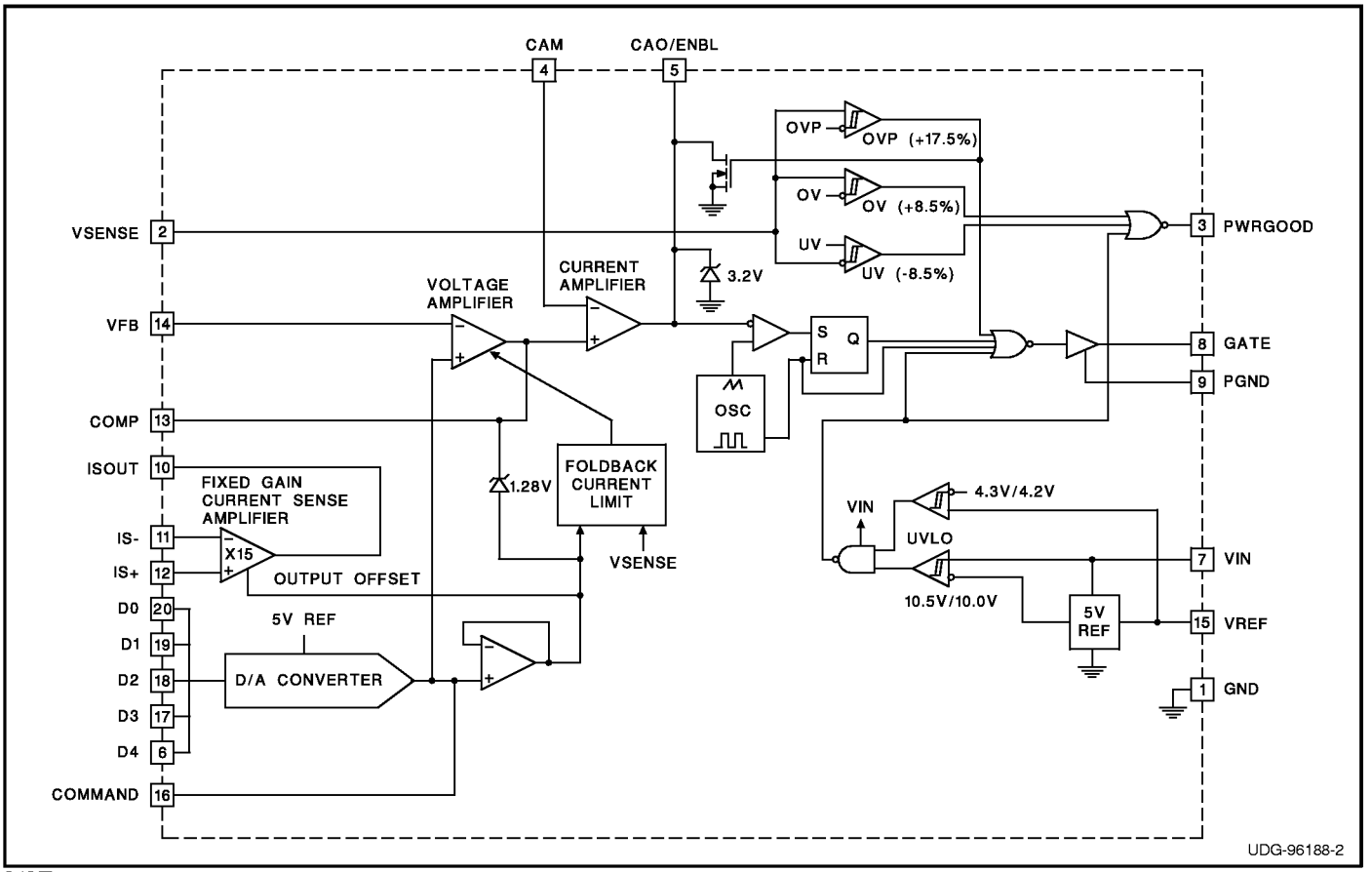
The UCC3830-4/-5/-6 is a fully integrated single chip solution ideal for powering high performance microprocessors. The chip includes an average current mode PWM controller, has a fully integrated 5-Bit DAC, and includes an onboard precision reference and voltage monitor circuitry. The UCC3830-x converts 5VDC to an adjustable output, ranging from 3.5VDC down to 1.8VDC with 1% DC system accuracy (see Table 1). The UCC3830-x fully supports Intel's 4-bit Pentium® Pro and 5-bit Pentium® II VID codes.

The accuracy of the DAC/reference combination is 1%. The overvoltage and undervoltage comparators monitor the system output voltage and indicate when it rises above or falls below its programmed value by more than 8.5%. A second overvoltage protection comparator pulls the current amplifier output voltage low to force zero duty cycle when the system output voltage exceeds its designed value by more than 17.5%. This comparator also terminates the cycle. Undervoltage lockout circuitry assures the correct logic states at the outputs during powerup and powerdown. The gate output can be disabled by bringing the CAO/ENBL pin to below 0.8V.

The voltage and current amplifiers have a 3MHz gain bandwidth product to satisfy high performance system requirements. The internal current sense amplifier permits the use of a low value current sense resistor, minimizing power loss. The oscillator frequency is fixed internally at 100kHz, 200kHz, or 400kHz,

(continued)

BLOCK DIAGRAM



DESCRIPTION (cont.)

depending upon the option selected. The foldback circuit reduces the converter short circuit current limit to 50% of its nominal value when the converter is short circuited. The gate driver is a 4Ω totem pole output stage capable of driving an external MOSFET.

This device is available in 20-pin dual in-line and surface mount packages. The UCC2830-x is specified for operation from –25°C to 85°C, and the UCC3830-x is specified for operation from 0°C to 70°C.

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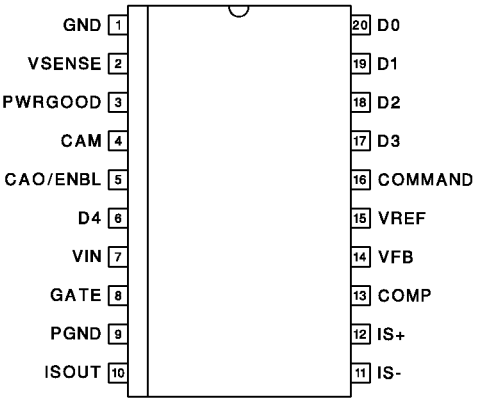
CONNECTION DIAGRAM

SOIC-20 (Top View)
DW Package



ABSOLUTE MAXIMUM RATING

Input Supply Voltage VIN 15V
D0, D1, D2, D3, D4, VSENSE, VFB, IS+, IS–, CAM Inputs
Maximum Forced Voltage . . . . . –0.3V to 5.3V
PWRGOOD Output Maximum Voltage 5.5V
COMMAND Ouput Maximum Current . . . . . Internally Limited
Reference Output Current . . . . . Internally Limited
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C
Currents are positive into negative out of the specified terminal. Pulse is defined as a less than 10% duty cycle with a maximum duration of 500µS. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

ORDERING INFORMATION

UCC □ 830 □ - □
- See Frequency Table
- Package
- Temperature Range

Consult factory for temperature range or package options not shown.

Frequency Table

	Frequency		
	100kHz	200kHz	400kHz
UCC3830-4	X		
UCC3830-5		X	
UCC3830-6			X

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VIN = 12V, VSENSE = 3.5V, VD0 = VD1 = VD2 = VD3 = VD4 = 0V, 0°C < T_A < 70°C, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout					
VIN UVLO Turn-on Threshold			10.5	10.8	V
VIN UVLO Turn-off Threshold		9.5	10		V
UVLO Threshold Hysteresis		200	500	700	mV
Supply Current					
I_{IN}	D0 through D4 = Open		7.5	13.5	mA
DAC/Reference					
COMMAND Voltage Accuracy	10.8V < VIN < 13.2V, I_{VREF} = 0mA, 0°C < T_A < 70°C	–1		1	%
	10.8V < VIN < 13.2V, I_{VREF} = 0mA, –25°C < T_A < 85°C	–1.25		1.25	%
D0-D4 Voltage High	DX Pin Floating	4	5	5.2	V
D0-D4 Input Bias Current	DX Pin Tied to GND	–100	–70	–20	µA
OVP Comparator					
Trip Point	% Over COMMAND Voltage (Note 1), D0 = D1 = D2 = D4 = Open, D3 = GND	10	17.5	25	%
Hysteresis			20	30	mV
VSENSE Input Bias Current	OV, OVP, UV Combined	–0.5	–0.1	0.5	µA

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, VIN = 12V, VSENSE = 3.5V, VD0 = VD1 = VD2 = VD3 = VD4 = 0V, 0°C < T_A < 70°C, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OV Comparator					
Trip Point	% Over COMMAND Voltage (Note 1), D0 = D1 = D2 = D4 = Open, D3 = GND	5	8.5	12	%
Hysteresis			20	30	mV
PWRGOOD Equivalent Resistance	VSENSE = 2.0V			470	Ω
UV Comparator					
Trip Point	% Over COMMAND Voltage (Note 1), D0 = D1 = D2 = D4 = Open, D3 = GND	–12	–8.5	–5	%
Hysteresis			20	30	mV
Voltage Error Amplifier					
Input Bias Current	V_{CM} = 3.0V	–0.5	–0.02	0.5	µA
Open Loop Gain	1.5V < V_{COMP} < 2.5V, D4 = D3 = D2 = D1 = GND, D0 = Open		80		dB
Power Supply Rejection Ratio	10.8V < VIN < 15V		85		dB
Output Sourcing Current	V_{VFB} = 2V, $V_{COMMAND}$ = V_{COMP} = 2.5V		–0.5	–0.3	mA
Output Sinking Current	V_{VFB} = 3V, $V_{COMMAND}$ = V_{COMP} = 2.5V	0.5	1		mA
Current Sense Amplifier					
Gain		14.25		15.25	V/V
Input Resistance			3		kΩ
Common Mode Rejection Ratio	0V < V_{CM} < 4.5V		60		dB
Power Supply Rejection Ratio	10.8V < VIN < 15V		80		dB
Output Sourcing Current	$V_{IS–}$ = 2V, V_{ISOUT} = V_{IS+} = 2.5V		–0.5	–0.3	mA
Output Sinking Current	$V_{IS–}$ = 3V, V_{ISOUT} = V_{IS+} = 2.5V	5	8		mA
Current Amplifier					
Input Offset Voltage	V_{CM} = 3.0V	–12		12	mV
Input Bias Current	V_{CM} = 3.0V		–0.1		µA
Open Loop Gain	1V < $V_{CAO/ENBL}$ < 2.5V		80		dB
Output Voltage High	V_{COMP} = 3V, V_{CAM} = 2.5V		3.2		V
Power Supply Rejection Ratio	10.8V < VIN < 15V		80		dB
Output Sourcing Current	V_{CAM} = 2V, $V_{CAO/ENBL}$ = V_{COMP} = 2.5V		–1	–0.5	mA
Output Sinking Current	V_{CAM} = 3V, $V_{CAO/ENBL}$ = V_{COMP} = 2.5V	3	5		mA
Oscillator					
Frequency (-4)		85	100	115	kHz
Frequency (-5)		170	200	230	kHz
Frequency (-6)		340	400	460	kHz
Frequency Change With Voltage	10.8V < VIN < 15V		1		%
Output Section					
Maximum Duty Cycle		90	95	99	%
Output Low Voltage	I_{GATE} = –100mA		0.2		V
Output High Voltage	I_{GATE} = 100mA		11.8		V
Rise Time	C_{GATE} = 3.3nF		20	70	ns
Fall Time	C_{GATE} = 3.3nF		15	70	ns
Foldback Current Limit					
Clamp Level	Measured at Voltage EA Output; V_{SENSE} = $V_{COMMAND}$ = 3V		4.28		V
	$V_{COMMAND}$ = 3V, V_{SENSE} = 0		3.64		V

Note 1: This percentage is measured with respect to the ideal COMMAND voltage programmed by the D0 - D4 pins.

PIN DESCRIPTIONS

CAM (Current Amplifier Inverting Input): The average load current feedback from ISOUT is applied through a resistor to this pin. The current loop compensation network is also connected to this pin (see CAO/ENBL below).

CAO/ENBL (Current Amplifier Output/Chip Enable): The current loop compensation network is connected between this pin and CAM. The voltage on this pin is the input to the PWM comparator and regulates the output voltage of the system. The GATE output is disabled (held low) unless the voltage on this pin exceeds 1V, allowing the PWM to force zero duty cycle when necessary. The PWM forces maximum duty cycle when the voltage on CAO/ENBL exceeds the oscillator peak voltage (3V). A 3.2V clamp circuit prevents the CAO/ENBL voltage from rising excessively past the oscillator peak voltage for excellent transient response. The user can force this pin below 0.8V externally with an open collector, disabling the GATE drive.

COMMAND (Digital-to-Analog Converter Output Voltage): This pin is the output of the 5-bit digital-to-analog converter (DAC) and the noninverting input of the voltage amplifier. The voltage on this pin sets the switching regulator output voltage. This voltage ranges from 1.8V to 3.5V as programmed by the 5-bit DAC according to Table 1. The GATE output is disabled when all 1s or illegal codes are presented at the 5 Bit DAC. The COMMAND source impedance is typically 1.2kΩ and must therefore drive only high impedance inputs if accuracy is to be maintained. Bypass COMMAND with a 0.01µF, low ESR, low ESL capacitor for best circuit noise immunity.

COMP (Voltage Amplifier Output): The system voltage compensation network is applied between COMP and VFB.

D0 - D4 (DAC Digital Input Control Codes): These are the DAC digital input control codes, with D0 representing the least significant bit (LSB) and D4, the most significant bit (MSB) as shown in Table 1. A bit is set low by being connected to GND. A bit is set high by floating it, or connecting it to a 5V source. Each control pin is pulled up to approximately 5V by an internal 70µA current source.

GATE (PWM Output, MOSFET Driver): This output provides a 4Ω totem pole driver. Use a series resistor between this pin and the gate of the external MOSFET to prevent excessive overshoot.

GND (Signal Ground): All voltages are measured with respect to GND. Bypass capacitors on the VCC and VREF pins should be connected directly to the ground plane near the GND pin.

IS– (Current Sense Amplifier Inverting Input): This pin is the inverting input to the current sense amplifier and is connected to the low side of the average current sense resistor.

IS+ (Current Sense Amplifier Noninverting Input): This pin is the noninverting input to the current sense amplifier and is connected to the high side of the average current sense resistor.

ISOUT (Current Sense Amplifier Output): This pin is the output of the current sense amplifier. The voltage on this pin is (COMMAND + G_{CSA} • I • R_{SENSE}), where COMMAND is the voltage on the COMMAND pin, G_{CSA} is the fixed gain of the current sense amplifier, equal to 15, I is the current through the sense resistor, and R_{SENSE} is the value of the average current sensing resistor.

PGND (Power Ground): This pin provides a dedicated ground for the output gate driver. The GND and PGND pins should be connected externally using a short printed circuit board trace close to the IC. Decouple VIN to PGND with a low ESR capacitor ≥ 0.10µF.

PWRGOOD (Undervoltage/Lower Overvoltage Output): This pin is an open drain output which is driven low to reset the microprocessor when VSENSE rises above or falls below its nominal value by 8.5%. The on resistance of the open drain switch will be no higher than 470Ω. The OV and UV comparators' hysteresis is fixed at 20mV independent of the COMMAND voltage.

VIN (Positive Supply Voltage): This pin supplies power to the chip. Connect VIN to a stable voltage source of at least 10.8V. The GATE and PWRGOOD outputs will be held low until VCC exceeds the upper undervoltage lockout threshold. This pin should be bypassed directly to the GND pin.

VFB (Voltage Amplifier Inverting Input): This input is connected to COMP through a feedback network and to the power supply output through a resistor or a divider network.

VREF (Voltage Reference Output): This pin provides an accurate 5V reference and is internally short circuit current limited. VREF powers the D/A converter and also provides a threshold voltage for the UVLO comparator. For best reference stability, bypass VREF directly to GND with a low ESR, low ESL capacitor of at least 0.01µF.

PIN DESCRIPTIONS (cont.)

VSENSE (Output Voltage Sensing Input): This pin is connected to the system output voltage through a low pass filter. When the voltage on VSENSE rises above or falls below the COMMAND voltage by 8.5%, the PWRGOOD output is driven low to reset the microprocessor. When the voltage on VSENSE rises above the COMMAND voltage by 17.5%, the OVP comparator pulls the current amplifier output voltage below the oscillator valley voltage to force zero duty cycle at the GATE output. This pin is also used by the foldback current limiting circuitry.

TYPICAL PERFORMANCE CURVES

The curves shown in Figures 1 and 2 depict the typical high gain-bandwidth products for the UCC3830-x Voltage Amplifier, Current Amplifier and Current Sense Amplifiers. These high gain-bandwidth devices help achieve an excellent transient response to load and line changes.

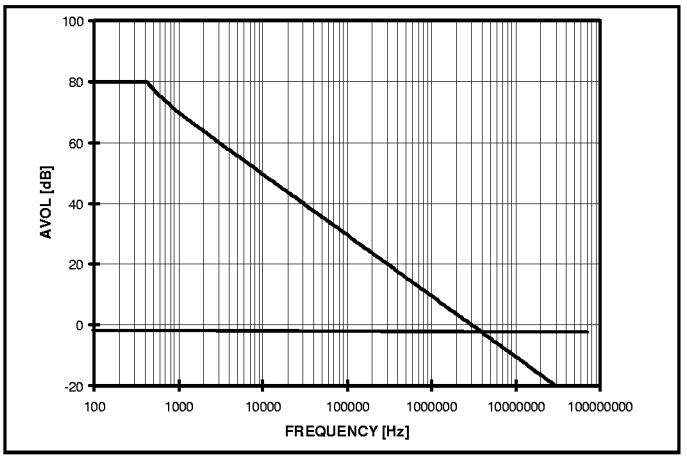


Figure 1. Open Loop Gain for UCC3830 Voltage and Current Amplifier

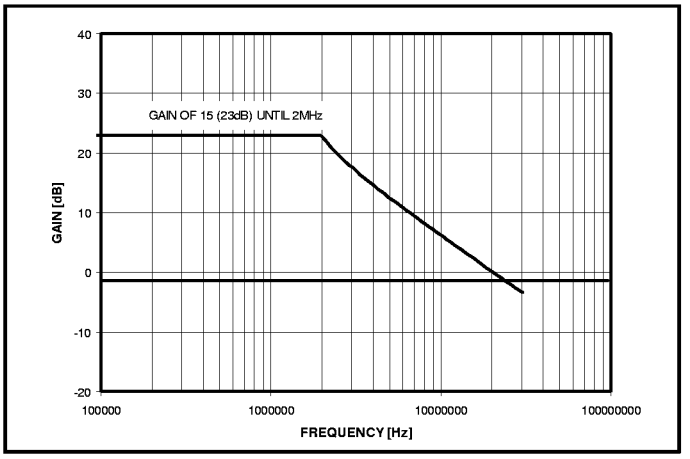


Figure 2. Current Sense Amplifier Gain vs Frequency

APPLICATION INFORMATION

Short Circuit Current Limit

The short circuit current limit, I_{SC}, is set according to:

$$I_{SC} = \frac{1.28V}{R_{SENSE} \bullet G_{CSA}}$$

where R_{SENSE} is the average current sense resistor and G_{CSA} is the current sense amplifier gain. G_{CSA} equals 15.

Example: Choose R_{SENSE} to set the short circuit limit at 17A using the UCC3830-5

$$R_{SENSE} = \frac{1.28V}{17A \bullet 15} = 0.005\Omega.$$

A lower resistance value may be needed if the AC ripple current in the inductor is more than 20% of the load current.

The UCC3830-x incorporates short circuit current foldback, as shown in Figure 3. When the output of the power supply is short circuited, the output voltage falls. When the output voltage reaches 1/2 of its nominal voltage (COMMAND/2) then the output current is reduced. This feature reduces the amount of current in the MOSFET, diode and capacitors, and insures high reliability.

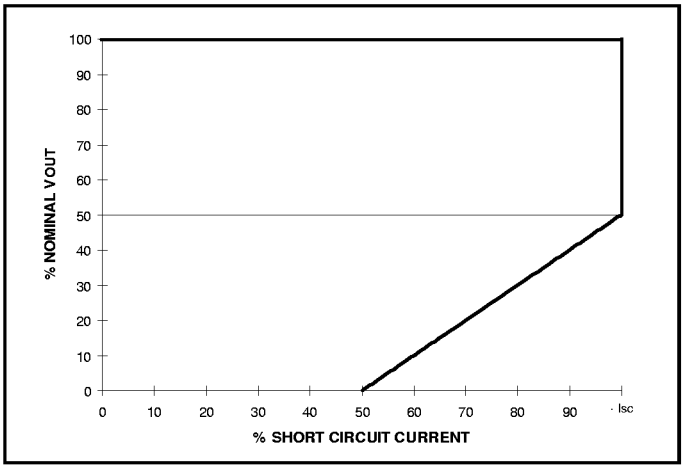


Figure 3. Short Circuit Foldback Reduces Stress on Circuit Components by Reducing Short Circuit Current

Enabling/Disabling the UCC3830-x Gate Drive

The CAO/ENBL pin can be used to disable the UCC3830 gate drive by forcing this pin below 0.8V, as shown in Figure 4. Bringing the voltage below the valley of the PWM oscillator ramp will insure a 0% duty cycle, effec-

APPLICATION INFORMATION

tively disabling the gate drive. A low noise open collector signal should be used as an Enable/Disable command.

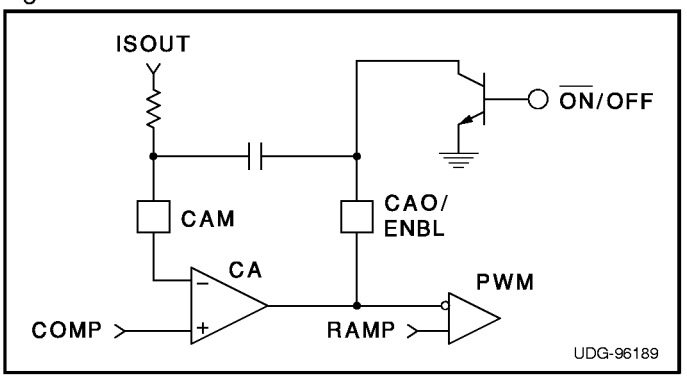


Figure 4. Disabling the UCC3830-x

Setting the Output Voltage Using the DAC

The 5-bit Digital-to-Analog Converter (DAC) is programmed according to Table 1. The COMMAND voltage is always active as long as the UCC3830 VIN pin is above the undervoltage lockout voltage. The output gate drive, GATE, is disabled at certain DAC codes, as shown in Table 1. Disabling the gate drive disables the power supply.

Operating the 5-Bit Controller with Intel's 4-Bit Pentium Pro

The UCC3830-x 5-Bit Controller is completely backward compatible. When the fifth bit, D4 is left open (4-Bit Processor in circuit), the UCC3830-x acts as a 4-Bit controller with the COMMAND voltage fully compatible with Intel's 4-Bit Pentium® Pro family.

Choosing the Input Capacitor

The input capacitors are chosen primarily based on their switching frequency RMS current handling capability and their voltage rating. The input capacitors must handle virtually all of the RMS current at the switching frequency, even if the circuit does not have an input inductor. The switching current in the input capacitors appears as shown in Figure 5.

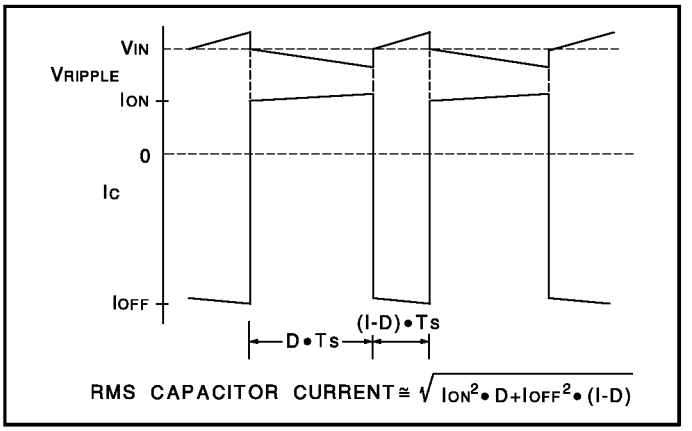


Figure 5. Input Capacitors Current Waveform

The amount of RMS current in an Aluminum Electrolytic capacitor has a strong impact on the reliability and lifetime of the capacitor. Other factors which affect the life of an input capacitor are internal heat rise, external airflow, the amount of time that the circuit operates at maximum current and the operating voltage. The curves in Figure 6 show the RMS current handled by the total input capacitance in typical VRM circuits delivering 1.8V to 2.8V and powered from 5V.

Digital Command					Command	GATEHI/GATELO	Digital Command					Command	GATEHI/GATELO
D4	D3	D2	D1	D0	Voltage	Status	D4	D3	D2	D1	D0	Voltage	Status
0	1	1	1	1	1.300	Note 1	1	1	1	1	1	2.000	Note 1
0	1	1	1	0	1.350	Note 1	1	1	1	1	0	2.100	Enabled
0	1	1	0	1	1.400	Note 1	1	1	1	0	1	2.200	Enabled
0	1	1	0	0	1.450	Note 1	1	1	1	0	0	2.300	Enabled
0	1	0	1	1	1.500	Note 1	1	1	0	1	1	2.400	Enabled
0	1	0	1	0	1.550	Note 1	1	1	0	1	0	2.500	Enabled
0	1	0	0	1	1.600	Note 1	1	1	0	0	1	2.600	Enabled
0	1	0	0	0	1.650	Note 1	1	1	0	0	0	2.700	Enabled
0	0	1	1	1	1.700	Note 1	1	0	1	1	1	2.800	Enabled
0	0	1	1	0	1.750	Note 1	1	0	1	1	0	2.900	Enabled
0	0	1	0	1	1.800	Enabled	1	0	1	0	1	3.000	Enabled
0	0	1	0	0	1.850	Enabled	1	0	1	0	0	3.100	Enabled
0	0	0	1	1	1.900	Enabled	1	0	0	1	1	3.200	Enabled
0	0	0	1	0	1.950	Enabled	1	0	0	1	0	3.300	Enabled
0	0	0	0	1	2.000	Enabled	1	0	0	0	1	3.400	Enabled
0	0	0	0	0	2.050	Enabled	1	0	0	0	0	3.500	Enabled

Table 1. Programming the Command Voltage for the UCC3830-x

APPLICATION INFORMATION (cont.)

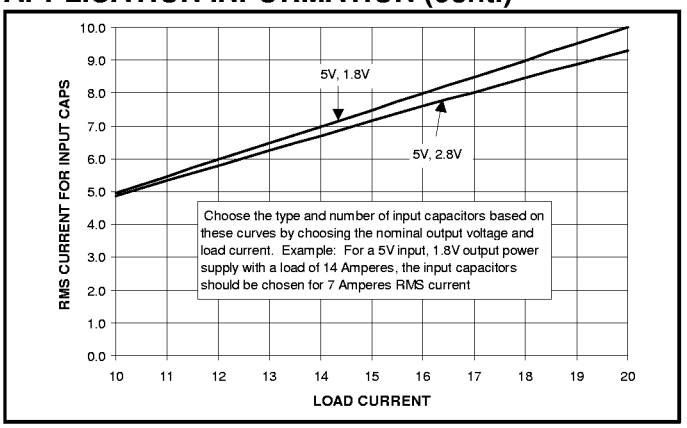


Figure 6. Load Current vs RMS Current for Input Capacitors

Related Publications

U-156 and U-157 are Unitrode Application Notes describing the operation of the UC3886 and the UC3886/UC3910 together in a Pentium® Pro application.

TYPICAL APPLICATION

The UCC3830-x is ideal for converting the 5.0V system bus into the required Pentium® Pro bus voltage. The 3.3V system bus can also be converted using the UCC3830-x when the Pentium® Pro requires lower bus voltages.

Figure 7. Efficiency of UCC3830-5 200kHz Demo Kit at 2.8V Ouput

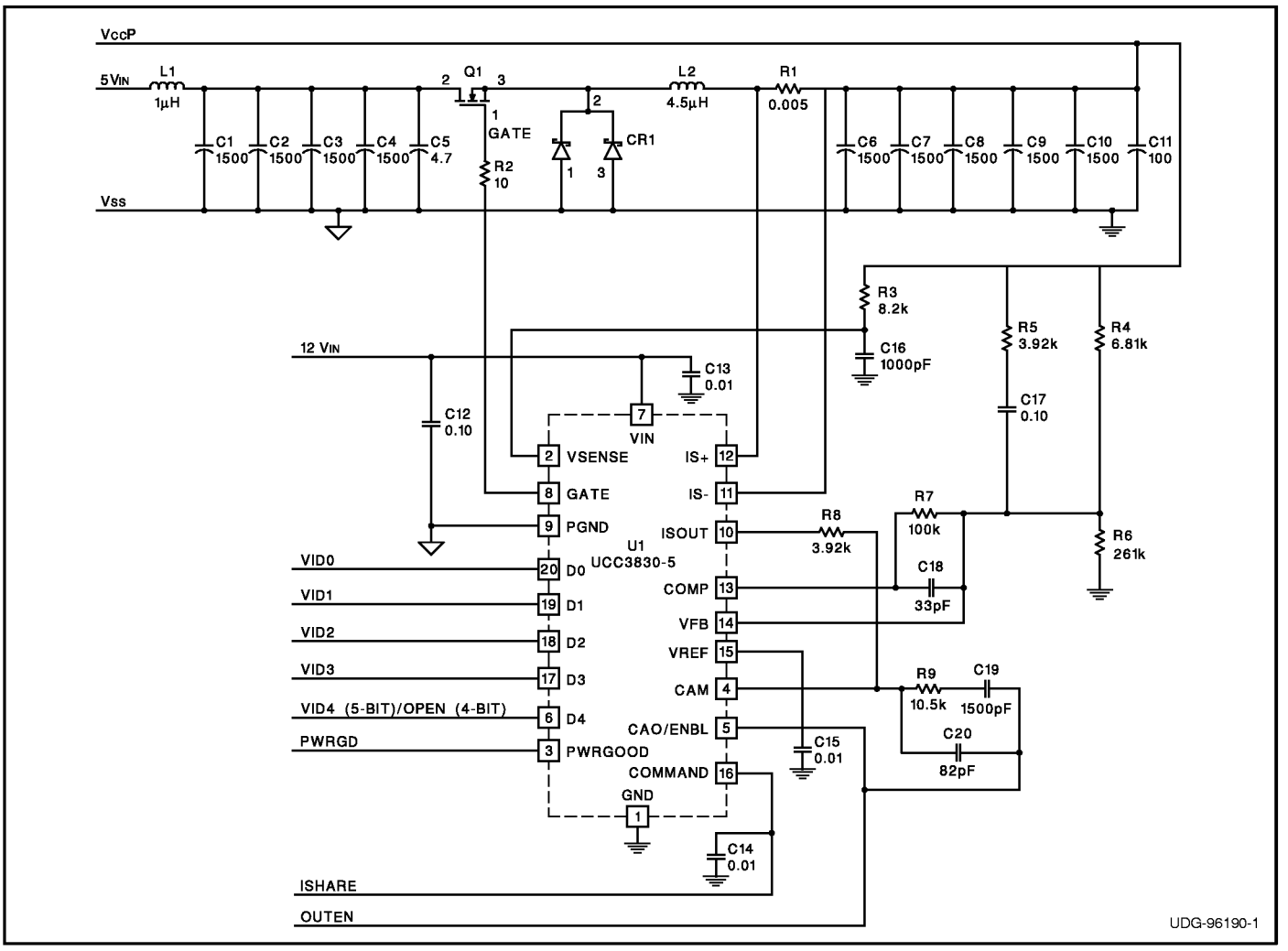


Figure 8. UCC3830 Configured for 4-Bit or 5-Bit Operation

PARTS LIST

REF.	DESCRIPTION	PACKAGE
U1	Unitrode UCC3830DWP-5 DAC/PWM	SOIC-20 Wide
C1	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C2	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C3	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C4	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C5	Sprague/Vishay 595D475X0016A2B, 4.7µF 16V Tantalum	SPRAGUE Size A
C6	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C7	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C8	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C9	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C10	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C11	Sprague 593D107X9010D2, 100µF, 6.3V Tantalum	EIA Size D SMD
C12	0.10µF Ceramic	1206 SMD
C13	0.01µF Ceramic	0603 SMD
C14	0.01µF Ceramic	0603 SMD
C15	0.01µF Ceramic	0603 SMD
C16	1000pF Ceramic	0603 SMD
C17	0.10µF Ceramic	1206 SMD
C18	33pF NPO Ceramic	0603 SMD
C19	1500pF Ceramic	0603 SMD
C20	82pF NPO Ceramic	0603 SMD
C21	0.10µF Ceramic	1206 SMD
C22	0.10µF Ceramic	1206 SMD
CR1	International Rectifier 32CTQ030 30V, 30A Schottky Diode	TO-220AB
L1	Micrometals T50-52B, 10 Turns #16AWG, 4.5µH	Toroid
Q1	International Rectifier IRL3103, 30V, 56A	TO-220AB
R1	Dale/Vishay WSR-2 0.005Ω 1%	SMD Power Package
R2	10Ω, 5%, 1/16 Watt	0603 SMD
R3	8.2kΩ, 5%, 1/16 Watt	0603 SMD
R4	6.81kΩ, 1%, 1/16 Watt	0603 SMD
R5	3.92kΩ, 1%, 1/16 Watt	0603 SMD
R6	261kΩ, 1%, 1/16 Watt	0603 SMD
R7	100kΩ, 1%, 1/16 Watt	0603 SMD
R8	3.92kΩ, 1%, 1/16 Watt	0603 SMD
R9	10.5kΩ, 1%, 1/16 Watt	0603 SMD
Q1-HS	AAVID 576802 TO-220 Heat Sink	TO-220AB
CR1-HS	AAVID 577002 TO-220 Heat Sink	TO-220AB

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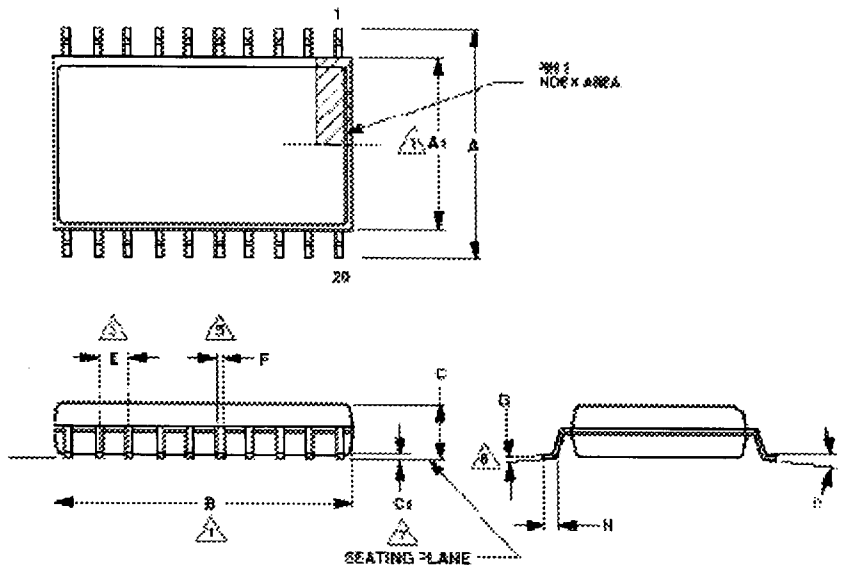
Mechanical Drawings

Back to Packaging Index

20-PIN SOIC SURFACE MOUNT~ DW PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.504	.511	12.80	12.98
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°



NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).