

# Off-line Power Supply Controller

## FEATURES

- Transformerless Off-line Applications
- Ideal Primary-side Bias Supply
- Efficient BiCMOS Design
- Wide Input Range
- Fixed or Adjustable Low Voltage Output
- Uses Low Cost SMD Inductors
- Short Circuit Protected
- Optional Isolation Capability

## DESCRIPTION

The UCC1889 controller is optimized for use as an off-line, low power, low voltage, regulated bias supply. The unique circuit topology utilized in this device can be visualized as two cascaded flyback converters, each operating in the discontinuous mode, and both driven from a single external power switch. The significant benefit of this approach is the ability to achieve voltage conversion ratios of 400V to 12V with no transformer and low internal losses.

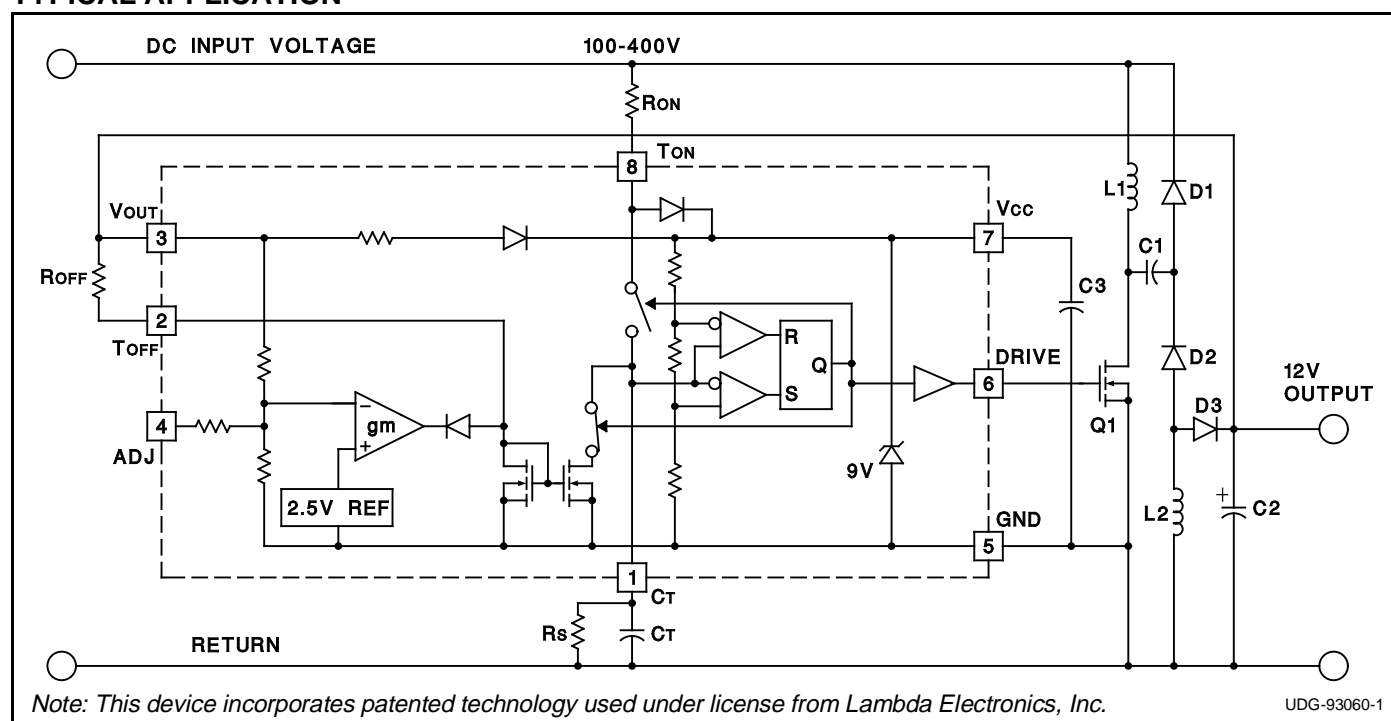
The control algorithm utilized by the UCC1889 is to force the switch on time to be inversely proportional to the input line voltage while the switch off time is made inversely proportional to the output voltage. This action is automatically controlled by an internal feedback loop and reference. The cascaded configuration allows a voltage conversion from 400V to 12V to be achieved with a switch duty cycle greater than 10%. This topology also offers inherent short circuit protection since as the output voltage falls to zero, the switch off time approaches infinity.

The output voltage can be easily set to 12V or 18V. Moreover, it can be programmed for other output voltages less than 18V with a few additional components. An isolated version can be achieved with this topology as described further in Unitrode Application Note U-149.

## OPERATION

With reference to the application diagram below, when input voltage is first applied, the RON current into TON is directed to VCC where it charges the external capacitor, C3, connected to VCC. As voltage builds on VCC, an internal undervoltage lockout holds the circuit off and the output at DRIVE low until Vcc reaches 8.4V. At this time, DRIVE goes high turning on the power switch, Q1, and redirecting the current into TON to the timing capacitor, CT. CT charges to a fixed threshold with a current  $I_{CHG} = 0.8 \cdot (V_{IN} - 4.5V)/R_{ON}$ . Since DRIVE will only be high for as long as CT charges, the power switch on time will be inversely proportional to line voltage. This provides a constant line voltage-switch on time product.

## TYPICAL APPLICATION





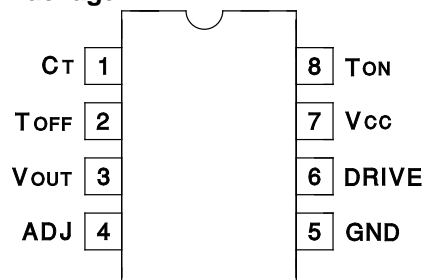
## ABSOLUTE MAXIMUM RATINGS

$I_{CC}$ . . . . .	5mA
Current into TON Pin . . . . .	1.5mA
Voltage on VOUT Pin . . . . .	20V
Current into TOFF Pin . . . . .	250 $\mu$ A
Storage Temperature . . . . .	-65°C to +150°C

Note: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.

## CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)  
N or J, D Package



**ELECTRICAL CHARACTERISTICS** Unless otherwise stated, these specifications hold for  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  for the UCC3889,  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  for the UCC2889, and  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$  for the UCC1889. No load at DRIVE pin ( $C_{LOAD}=0$ ).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>General</b>					
VCC Zener Voltage	$I_{CC} < 1.5\text{mA}$	8.6	9.0	9.3	V
Startup Current	$V_{OUT} = 0$		150	250	$\mu\text{A}$
Operating Current $I(V_{OUT})$	$V_{OUT} = 11\text{V}$ , $F = 150\text{kHz}$		1.2	2.5	mA
<b>Under-Voltage-Lockout</b>					
Start Threshold	$V_{OUT} = 0$	8.0	8.4	8.8	V
Minimum Operating Voltage after Start	$V_{OUT} = 0$	6.0	6.3	6.6	V
Hysteresis	$V_{OUT} = 0$	1.8			V
<b>Oscillator</b>					
Amplitude	$V_{CC} = 9\text{V}$	3.5	3.7	3.9	V
$C_T$ to DRIVE high Propagation Delay	Overdrive = 0.2V		100	200	ns
$C_T$ to DRIVE low Propagation Delay	Overdrive = 0.2V		50	100	ns
<b>Driver</b>					
VOL	$I = 20\text{mA}$ , $V_{CC} = 9\text{V}$		0.15	0.4	V
	$I = 100\text{mA}$ , $V_{CC} = 9\text{V}$		0.7	1.8	V
VOH	$I = -20\text{mA}$ , $V_{CC} = 9\text{V}$	8.5	8.8		V
	$I = -100\text{mA}$ , $V_{CC} = 9\text{V}$	6.1	7.8		V
Rise Time	$C_{LOAD} = 1\text{nF}$		35	70	ns
Fall Time	$C_{LOAD} = 1\text{nF}$		30	60	ns
<b>Line Voltage Detection</b>					
Charge Coefficient: $I_{CHG} / I(TON)$	$V_{CT} = 3\text{V}$ , DRIVE = High, $I(TON) = 1\text{mA}$	0.73	0.79	0.85	
Minimum Line Voltage for Fault	$R_{ON} = 330\text{k}$	60	80	100	V
Minimum Current $I(TON)$ for Fault	$R_{ON} = 330\text{k}$		220		$\mu\text{A}$
On Time During Fault	$C_T = 150\text{pF}$ , $V_{LINE} = \text{Min} - 1\text{V}$		2		$\mu\text{s}$
Oscillator Restart Delay after Fault			0.5		ms
<b>Vout Error Amp</b>					
VOUT Regulated 12V (ADJ Open)	$V_{CC} = 9\text{V}$ , $I_{DCHG} = I(TOFF)/2$	11.2	11.9	12.8	V
VOUT Regulated 18V (ADJ = 0V)	$V_{CC} = 9\text{V}$ , $I_{DCHG} = I(TOFF)/2$	16.5	17.5	19.5	V
Discharge Ratio: $I_{DCHG} / I(TOFF)$	$I(TOFF) = 50\mu\text{A}$	0.95	1.01	1.07	
Voltage at TOFF	$I(TOFF) = 50\mu\text{A}$	0.6	0.95	1.3	V
Regulation gm (Note 1)	Max $I_{DCHG} = 50\mu\text{A}$		1.0		mA/V
	Max $I_{DCHG} = 125\mu\text{A}$	0.8	1.7	2.9	mA/V

Note 1: gm is defined as  $\frac{\Delta I_{DCHG}}{\Delta V_{OUT}}$  for the values of VOUT when VOUT is in regulation. The two points used to calculate gm are for  $I_{DCHG}$  at 65% and 35% of its maximum value.

## PIN DESCRIPTIONS

**ADJ:** The ADJ pin is used to provide a 12V or an 18V regulated supply without additional external components. To select the 12V option, ADJ pin is left open. To select the 18V option, ADJ pin must be grounded. For other output voltages less than 18V, a resistor divider between VOUT, ADJ and GND is needed. Note, however, that for output voltages less than VCC, the device needs additional bootstrapping to VCC from an external source such as the line voltage. If so, precautions must be taken to ensure that total ICC does not exceed 5mA.

**CT (timing capacitor):** The signal voltage across CT has a peak-to-peak swing of 3.7V for 9V VCC. As the voltage on CT crosses the oscillator upper threshold, DRIVE goes low. As the voltage on CT crosses the oscillator lower threshold, DRIVE goes high.

**DRIVE:** This output is a CMOS stage capable of sinking 200mA peak and sourcing 150mA peak. The output voltage swing is 0 to VCC.

**GND (chip ground):** All voltages are measured with respect to GND.

**TOFF (regulated output control):** TOFF sets the discharge current of the timing capacitor through an external

resistor connected between VOUT and TOFF.

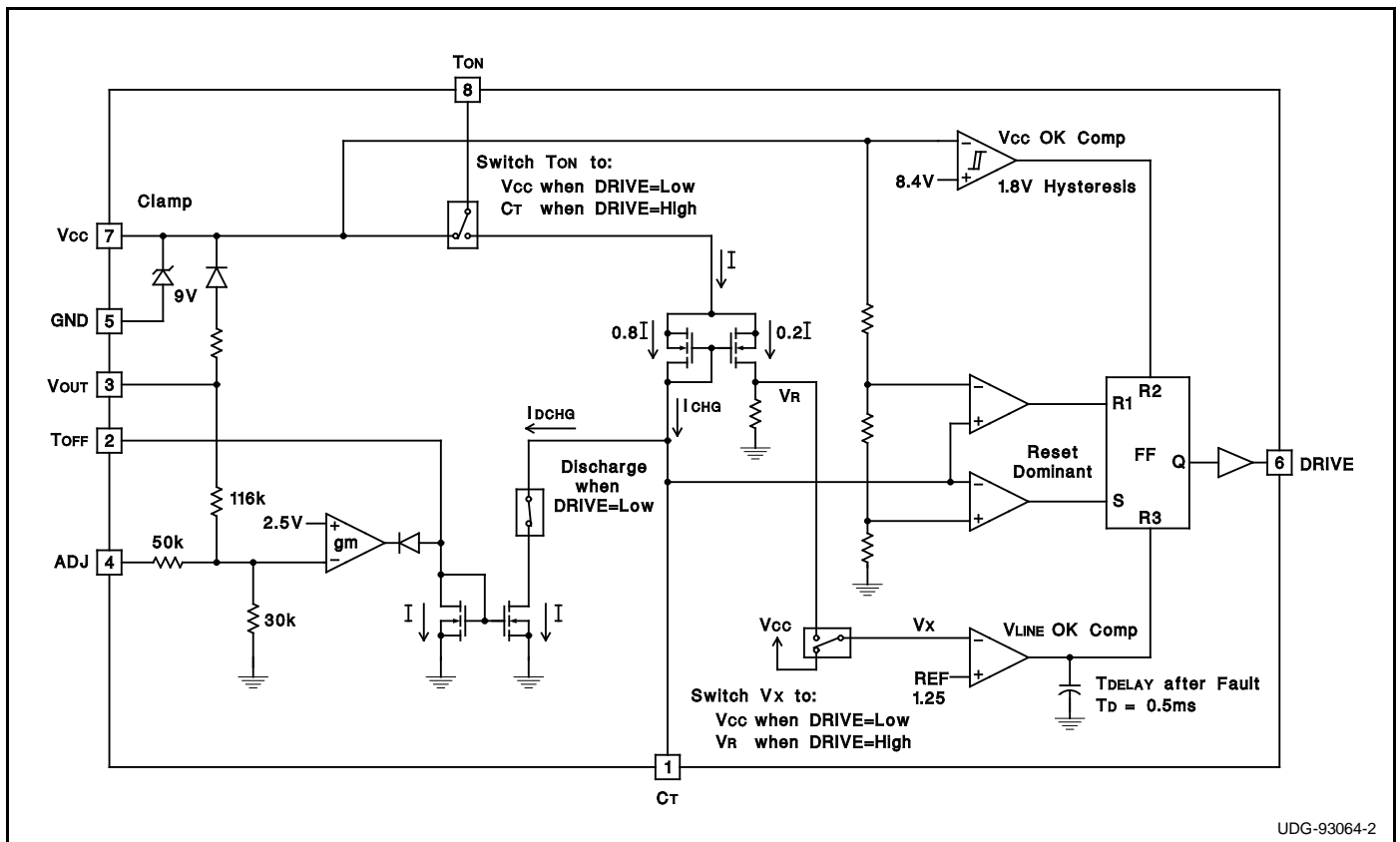
**TON (line voltage control):** TON serves three functions. When CT is discharging (off time), the current through TON is routed to VCC. When CT is charging (on time), the current through TON is split 80% to set the CT charge time and 20% to sense minimum line voltage which occurs for a TON current of 220μA. For a minimum line voltage of 80V, RON is 330kΩ.

The CT voltage slightly affects the value of the charge current during the on time. During this time, the voltage at the TON pin increases from approximately 2.5V to 6.5V.

**VCC (chip supply voltage):** The supply voltage of the device at pin VCC is internally clamped at 9V. Normally, VCC is not directly powered from an external voltage source such as the line voltage. In the event that VCC is directly connected to a voltage source for additional bootstrapping, precautions must be taken to ensure that total ICC does not exceed 5mA.

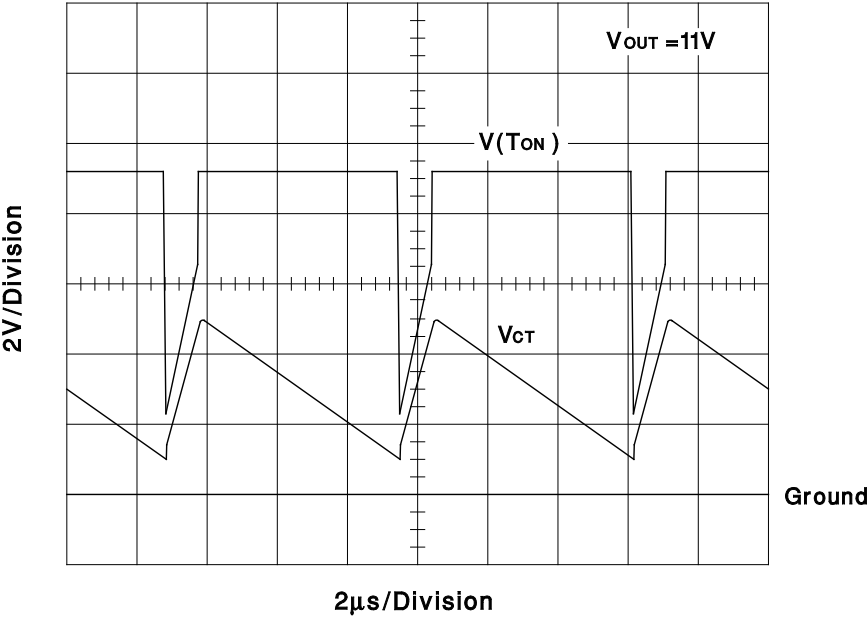
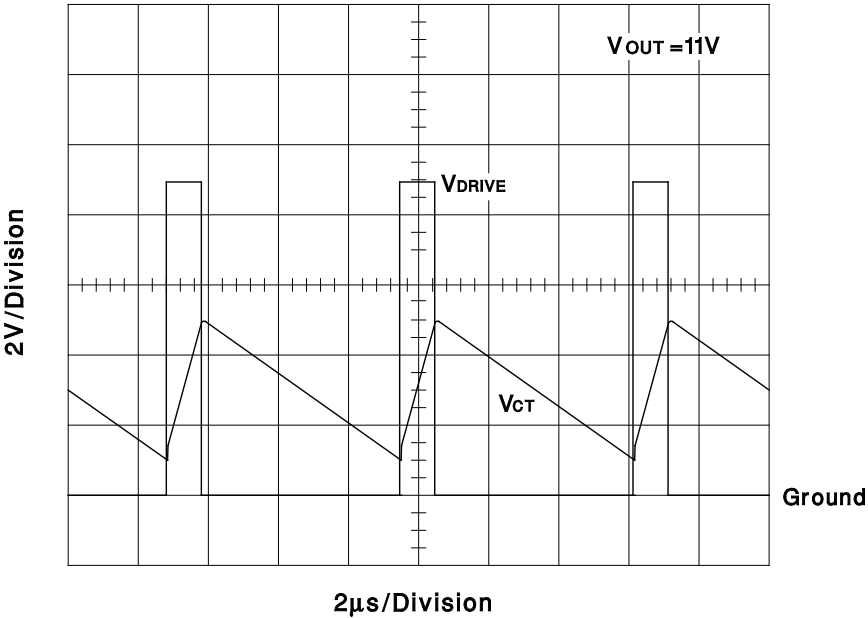
**VOUT (regulated output):** The VOUT pin is directly connected to the power supply output voltage. When VOUT is greater than VCC, VOUT bootstraps VCC.

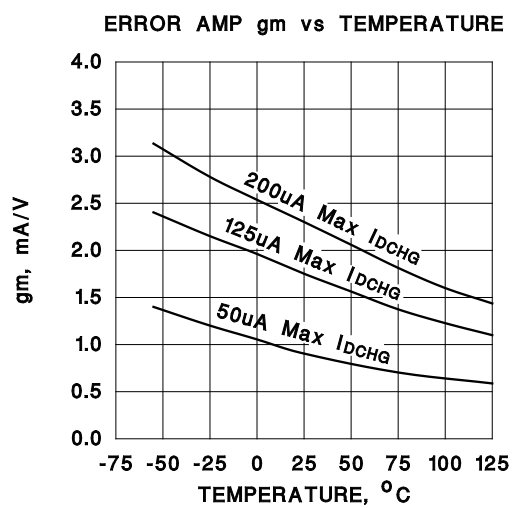
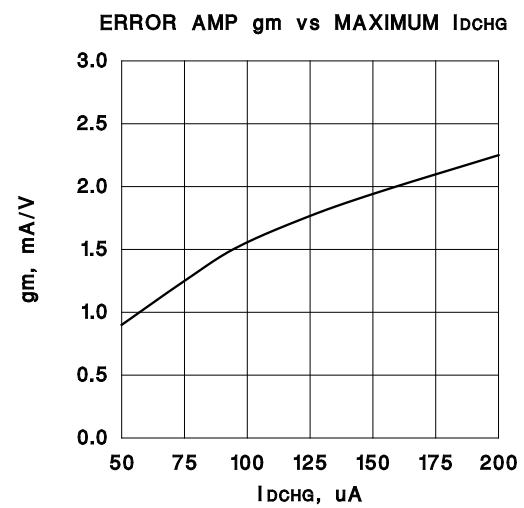
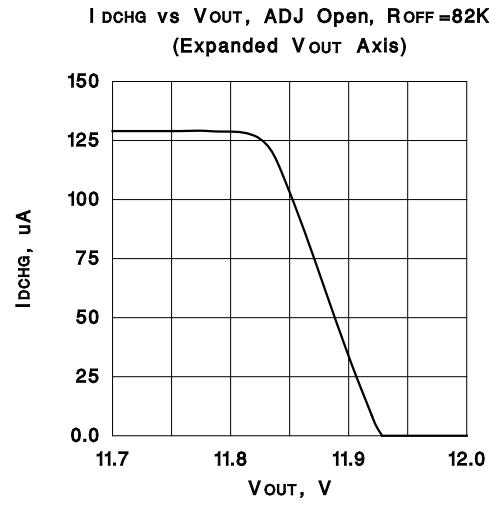
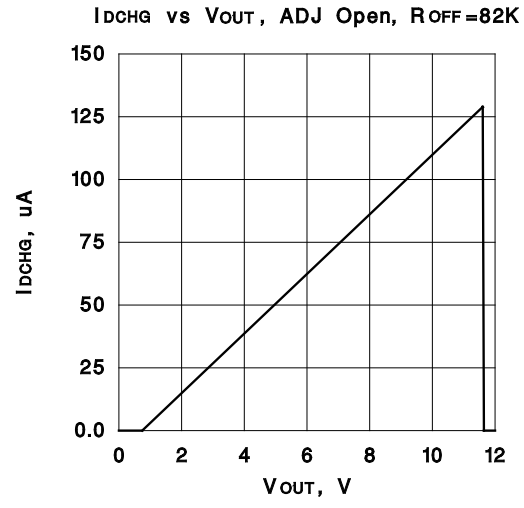
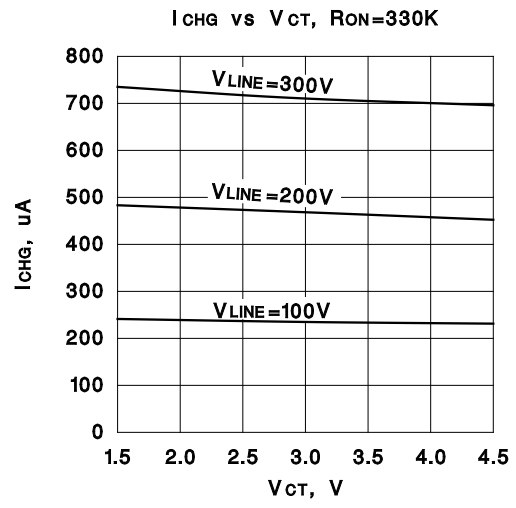
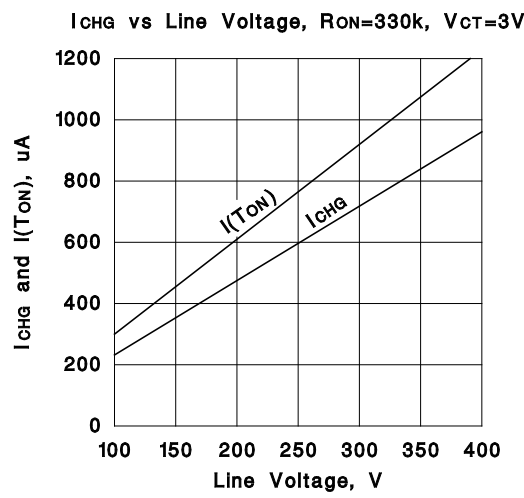
## BLOCK DIAGRAM



UDG-93064-2

TYPICAL WAVEFORMS





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