UNITRODE

application INFO available

UCC2918
UCC3918

Low On Resistance Hot Swap Power Manager

FEATURES

- Integrated 0.06Ω Power MOSFET
- 3V to 6V Operation
- External Analog control of Fault Current from 0A to 4A
- Independent Analog Control of Current Limit up to 5A
- Fast Overload Protection
- Uni-directional Switch
- Minimal External Components
- 1μA I_{CC} when Disabled
- Programmable On Time
- Programmable Start Delay
- Fixed 3% Duty Cycle

DESCRIPTION

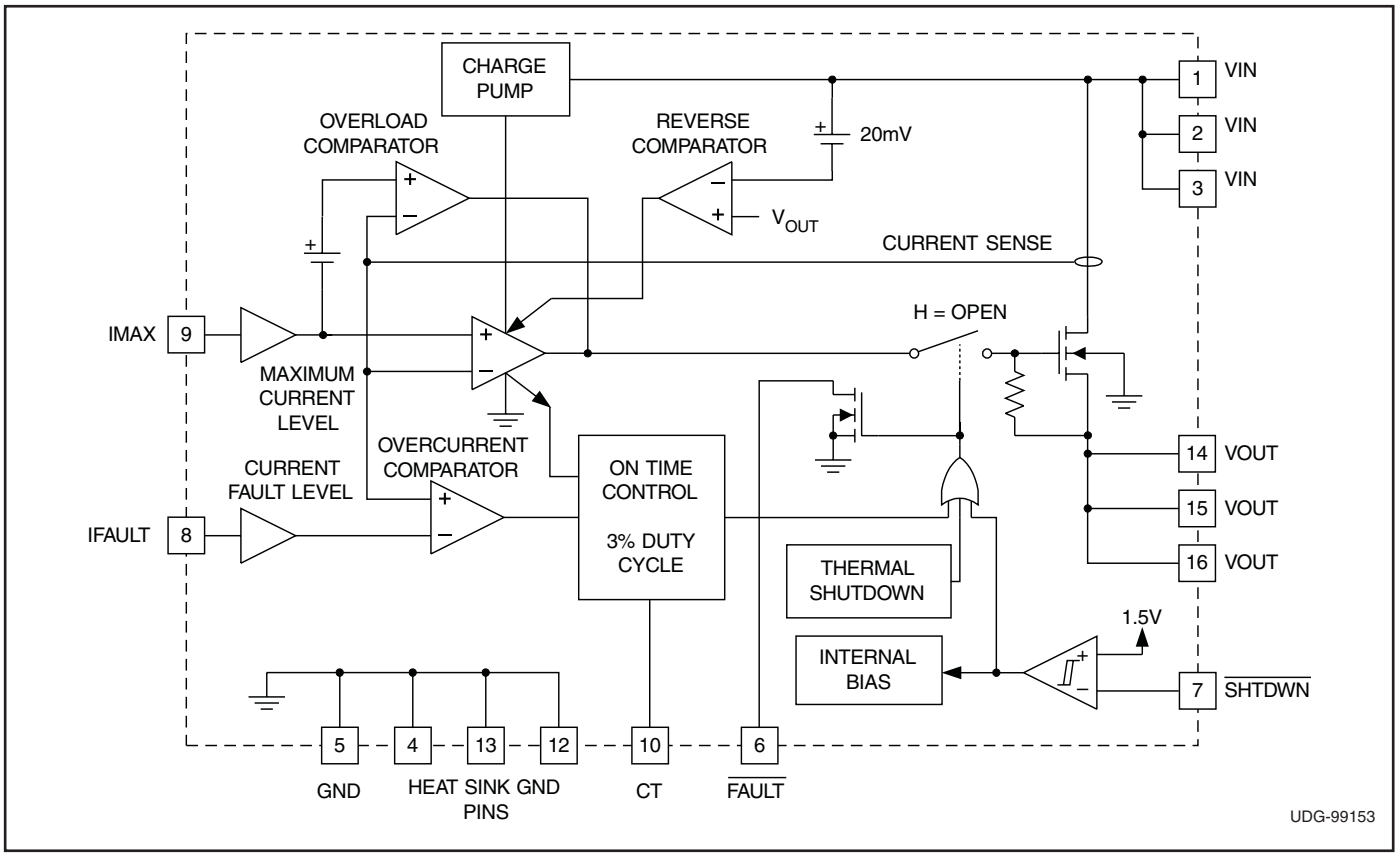
The UCC3918 Low on Resistance Hot Swap Power Manager provides complete power management, hot swap capability, and circuit breaker functions. The only components needed to operate the device, other than supply bypassing, are a timing capacitor, and 2 programming resistors. All control and housekeeping functions are integrated, and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, and startup delay. In the event of a constant fault, the internal fixed 3% duty cycle ratio limits the average output power. The IFAULT pin allows linear programming of the fault level current from 0A to 4A.

Fast overload protection is accomplished by an additional overload comparator. Its threshold is internally set above the maximum sourcing current limit setting. In the event of a short circuit or extreme current condition, this comparator is tripped, shutting down the output. This function is needed since the maximum sourcing current limit loop has a finite bandwidth.

When the output current is below the fault level, the output MOSFET is switched on with a nominal resistance of 0.06Ω. When the output current exceeds the fault level or the maximum sourcing level, the output remains on, but the fault timer starts charging CT. Once CT charges to a preset threshold, the switch is turned off, and remains off for 30 times the programmed fault time. When the output current reaches the maximum sourcing level, the MOSFET transitions form a switch to a constant current source.

(continued)

BLOCK DIAGRAM



DESCRIPTION (continued)

The UCC3918 is designed for unidirectional current flow, emulating an ideal diode in series with the power switch. This feature is particularly attractive in applications where many devices are powering a common bus, such as with SCSI Termpwr. The UCC3918 can also be put into the sleep mode, drawing only 1µA of supply current.

Other features include an open drain fault output indicator, thermal shutdown, undervoltage lockout, 3V to 6V operation, and a low thermal resistance small outline power package.

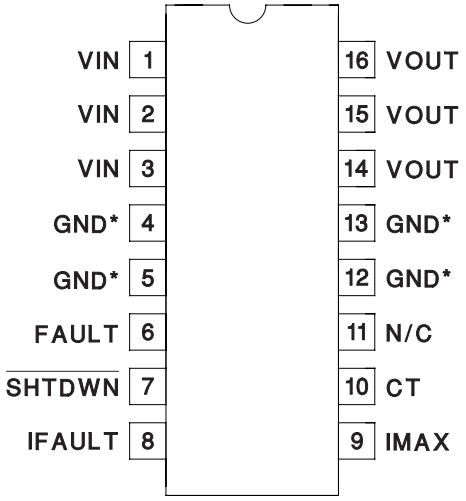
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (VIN) 8V
SOIC Power Dissipation 2.5W
Fault Output Sink Current. 50mA
Fault Output Voltage . . . . . VIN
Output Current (DC) . . . . . Internally Limited
Input Voltage
SHTDWN, IFAULT, IMAX . . . . . –0.3V to VIN
Storage Temperature Range . . . . . –65°C to +150°C
Operating Junction Temperature Range . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of the specified terminal. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500µS. Consult Packaging Section of Databook for thermal limitations and considerations of package.

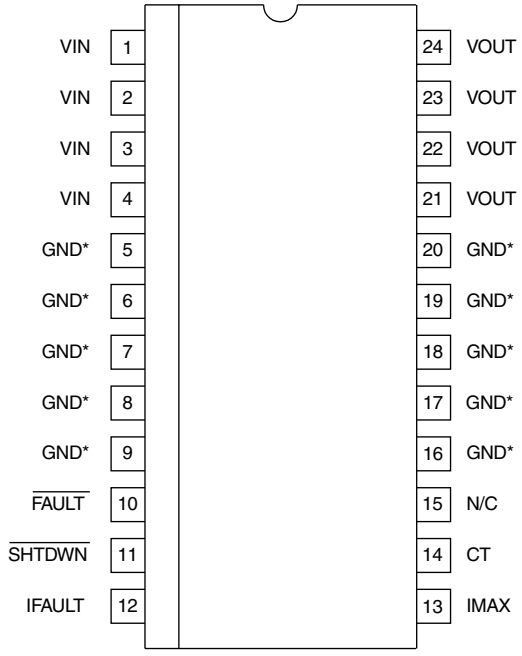
CONNECTION DIAGRAM

DIL-16, SOIC-16 (Top View)
N Package, DP Package



** Pin 5 serves as the lowest impedance to the electrical ground. Pins 4, 12, and 13 serve as heat sink/ground. These pins should be connected to large etch PCB areas to help dissipate heat. For N Package, pins 4, 12, and 13 are N/C.*

TSSOP-24 (Top View)
PWP Package



** Pin 9 serves as the lowest impedance to the electrical ground. Pins 5, 6, 7, 8, 16, 17, 18, 19 and 20 serve as heat sink/ground.*

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C for the UCC3918, –40°C to 85° for the UCC2918, VIN = 5V. R_{IMAX} = 42.2k, R_{IFAULT} = 52.3k, SHTDWN = 2.4. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Section					
Voltage Input Range, VIN		3	5	6	V
V_{DD} Supply Current	No Load		1	2	mA
Sleep Mode Current	$\overline{SHTDWN}$ = 0.2V		0.5	5	µA
Output Section					
RDS_{ON}	I_{OUT} = 1A to 4A, VIN = 5V, TA = 25°C		0.075	0.095	Ω
	I_{OUT} = 1A to 4A, VIN = 3V, TA = 25°C		0.09	0.116	Ω
	I_{OUT} = 1A to 4A, VIN = 5V		0.75	0.125	Ω
	I_{OUT} = 1A to 4A, VIN = 3V		0.09	0.154	Ω
Reverse Leakage Current	V_{IN} = 0V, V_{OUT} = 5V, $\overline{SHTDWN}$ = 0V			20	µA
Initial Startup Time	(Note 1)		100		µS
Thermal Shutdown	(Note 1)		170		DEG
Output Section (cont)					
Thermal Hysteresis	(Note 1)		10		DEG
Output Leakage	$\overline{SHTDWN}$ = 0.2V			20	µA
Trip Current	R_{IFAULT} = 105k	0.75	1	1.25	A
	R_{IFAULT} = 52.3k	1.7	2	2.3	A
	R_{IFAULT} = 34.8k	2.5	3	3.5	A
	R_{IFAULT} = 25.5k	3.3	4	4.7	A
Maximum Output Current	R_{IMAX} = 118k	0.3	1	1.7	A
	R_{IMAX} = 60.4k	1	2	3	A
	R_{IMAX} = 42.2k	2	3	4	A
	R_{IMAX} = 33.2k	2.5	3.8	5.1	A
	R_{IMAX} = 27.4k	3.0	4.6	6.2	A
Fault Section					
C_T Charge Current	V_{CT} = 1V	–50	–36	–22	µA
C_T Discharge Current	V_{CT} = 1V	0.5	1.2	2.0	µA
Fault Section (cont.)					
Output Duty Cycle	VOUT = 0V	1.5	3	6	%
C_T Fault Threshold		0.8	1.3	1.8	V
C_T Reset Threshold		0.25	0.5	0.75	V
Shutdown Section					
Shutdown Threshold		1.1	1.5	2.0	V
Shutdown Hysteresis			100		mV
Input Low Current	$\overline{SHTDWN}$ = 0V	–500	0	500	nA
Input High Current	$\overline{SHTDWN}$ = 2V	–2	–1	–0.5	µA
Open Drain Fault Output					
High Level Output Current				1	µA
Low Level Output Voltage	I_{OUT} = 1mA		0.4	0.9	V

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CT: A capacitor connected to this pin sets the maximum fault time. The maximum must be more than the time to charge external load capacitance. The maximum fault time is defined as

$$T_{FAULT} = 27.8 \bullet 10^{3} \bullet C_T$$

Once the fault time is reached the output will shutdown for a time given by

$$T_{SD} = 0.833 \bullet 10^{6} \bullet C_T,$$

this equates to a 3% duty cycle.

FAULT: Open drain output, which pulls low upon any condition which causes the output to open; Fault, Thermal Shutdown, Shutdown, and maximum sourcing current greater than the fault time.

GND: This is the most negative voltage in the circuit. All 4 ground pins should be used, and properly heat sunk on the PCB.

IFAULT: A resistor connected from this pin to ground sets the fault threshold. The resistor vs fault current is set by the formula

$$R_{FAULT} = \frac{105k}{I_{TRIP}}$$

IMAX: A resistor connected from this pin to ground sets the maximum sourcing current. The resistor vs the output sourcing current is set by the formula,

$$R_{FAULT} = \frac{126k}{Maximum\ Sourcing\ Current}$$

$\overline{\text{SHTDWN}}$: When this pin is brought low, the IC is put into sleep mode. The input threshold is hysteretic, allowing the user to program a startup delay with an external RC circuit.

VIN: This is the input voltage to the UCC3918. The recommended operating voltage range is 3V to 6V. All VIN pins should be connected together and to the power source.

VOUT: Output voltage for the circuit breaker. When switched the output voltage will be approximately VIN – 0.06Ω • I_{OUT}. All VOUT pins should be connected together and to the load.

APPLICATION INFORMATION

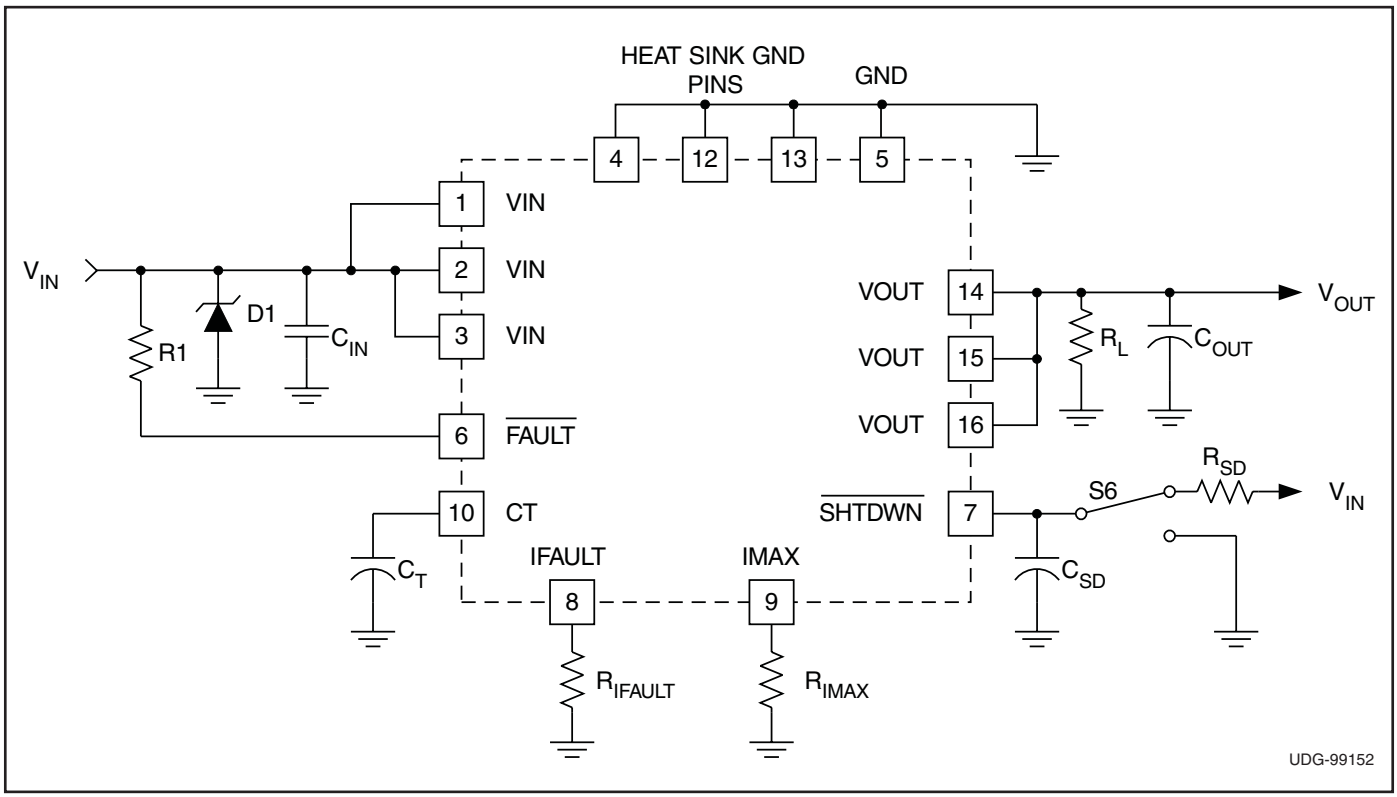


Figure 1. Evaluation circuit.

APPLICATION INFORMATION (cont.)

Protecting The UCC3918 From Voltage Transients

The parasitic inductance associated with the power distribution can cause a voltage spike at V_{IN} if the load current is suddenly interrupted by the UCC3918. *It is important to limit the peak of this spike to less than 6V to prevent damage to the UCC3918*. This voltage spike can be minimized by:

- Reducing the power distribution inductance (e.g., twist the positive "+" and negative "–" leads of the power supply feeding V_{IN}, locate the power supply close to the UCC3918 or use a PCB ground plane).
- Decoupling V_{IN} with a capacitor, C_{IN} (refer to Fig. 1), located close to the V_{IN} pin. This capacitor is typically less than 1µF to limit the inrush current.
- Clamping the voltage at V_{IN} below 6V with a Zener diode, D1 (refer to Fig. 1), located close to the V_{IN} pin.

Estimating Maximum Load Capacitance

For circuit breaker applications, the rate at which the total output capacitance can be charged depends on the maximum output current available and the nature of the load. For a constant-current current-limited circuit breaker, the output will come up if the load asks for less than the maximum available short-circuit current.

To guarantee recovery of a duty-cycle of the current-limited circuit breaker from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit ON time (Fault time). The design value of ON or Fault time can be adjusted by changing the timing capacitor C_T.

For worst-case constant-current load of value just less than the trip limit; $C_{OUT(max)}$ can be estimated from:

$$C_{OUT}(\max) \approx (I_{MAX} - I_{LOAD}) \left(\frac{28 \bullet 10^3 \bullet C_T}{V_{OUT}} \right)$$

Where V_{OUT} is the output voltage and I_{MAX} is the maximum, sourcing current.

For a resistive load of value RI, the value of $C_{OUT(max)}$ can be estimated from:

$$C_{OUT}(\max) \approx \left(\frac{28 \bullet 10^3 \bullet C_T}{R_L \bullet \ln \left[\frac{1}{1 - \frac{V_{OUT}}{I_{MAX} \bullet R_L}} \right]} \right)$$

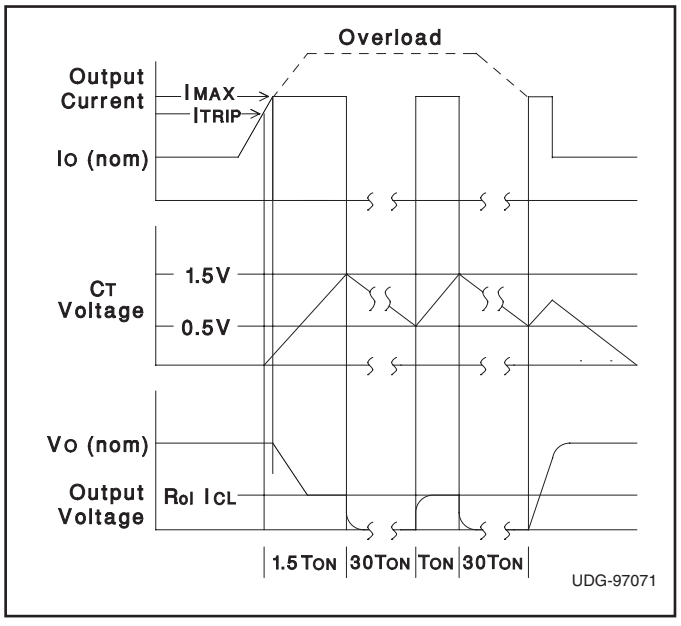
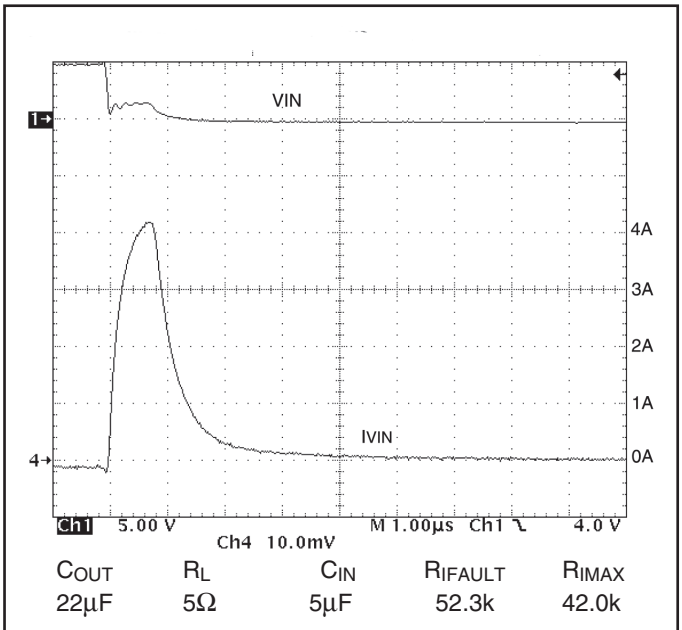


Figure 2. Load current, timing capacitor voltage and output voltage of the UCC3918 under fault.

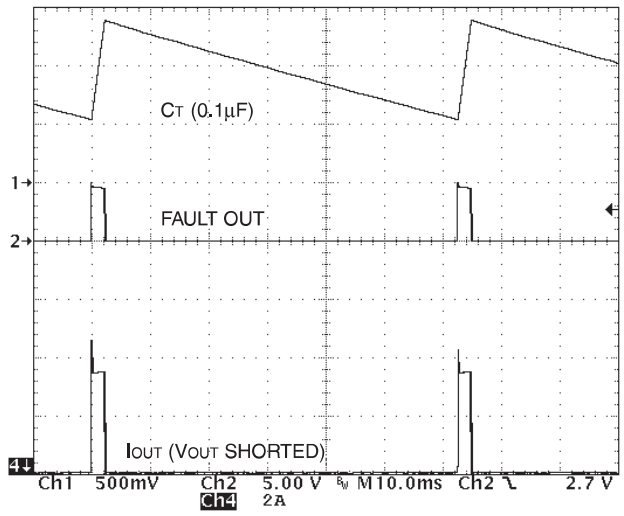


C_{OUT}	R_L	C_{IN}	R_{IFAULT}	R_{IMAX}
22µF	5Ω	5µF	52.3k	42.0k

Input driven with a pulse generator, shows C_{OUT} discharging through R_L and conducting through UCC3918 FET in the reverse direction.

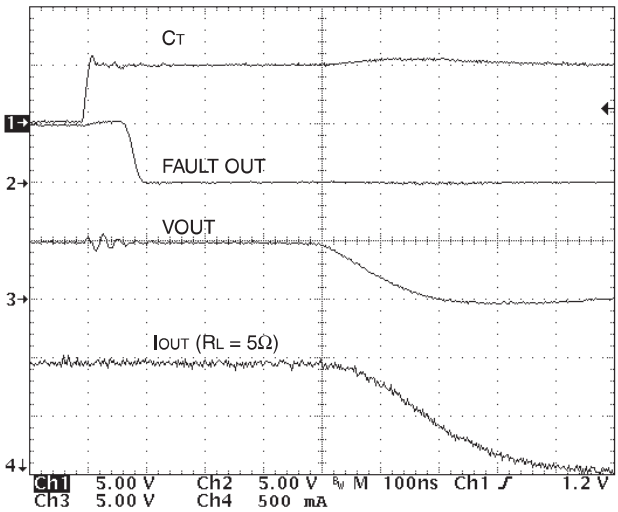
Figure 3.

APPLICATION INFORMATION (cont.)



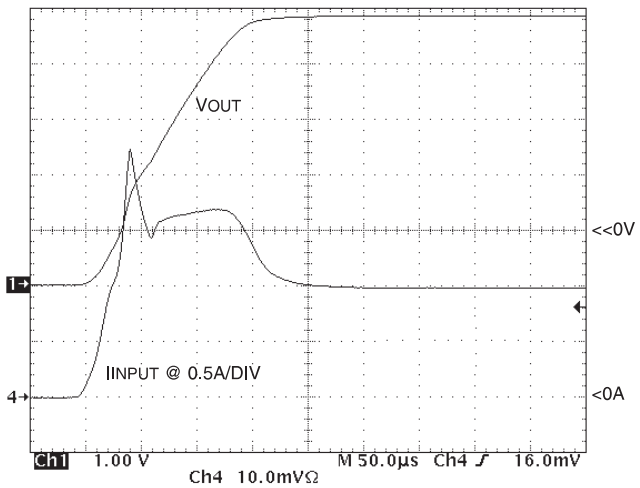
V_{OUT}	R_L	C_{IN}	R_{IFAULT}	R_{IMAX}
0V	SHORT	5µF	52.3k	42.2k

Figure 4. UCC3918 in shorted condition.



C_{OUT}	R_L	C_{IN}	R_{IFAULT}	R_{IMAX}	C_T
0µF	5Ω	5µF	52.3k	42.4k	OPEN

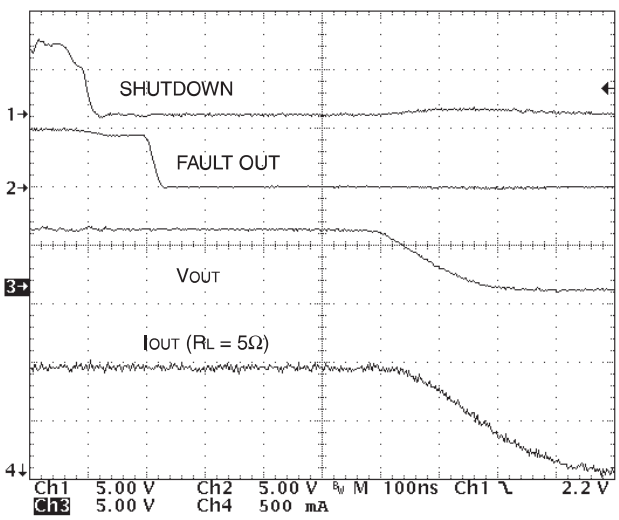
Figure 6. C_T to V_{OUT} delay (fault condition).



C_{OUT}	R_L	C_{IN}	R_{IFAULT}	R_{IMAX}
22µF	5Ω	5µF	52.3k	60.4k

Input switched on through external FET. V_{OUT} shows I_{MAX} linear amplifier limiting the changing current of C_{OUT}.

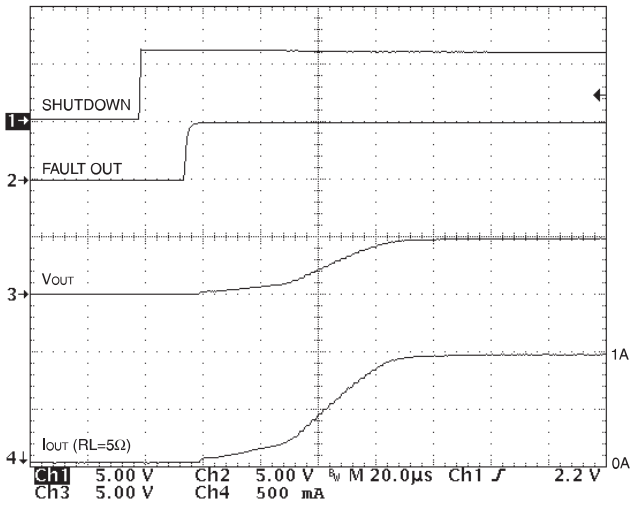
Figure 5. Input hot swap.



C_{OUT}	R_L	C_{IN}	R_{IFAULT}	R_{IMAX}
0µF	5Ω	5µF	52.3k	42.4k

Figure 7. Shutdown delay to V_{OUT} off.

APPLICATION INFORMATION (cont.)



C_{OUT}	R_L	C_{IN}	R_{IFAULT}	R_{IMAX}
0µF	5Ω	5µF	52.3k	42.4k

Figure 8. Shutdown delay to V_{OUT} on.

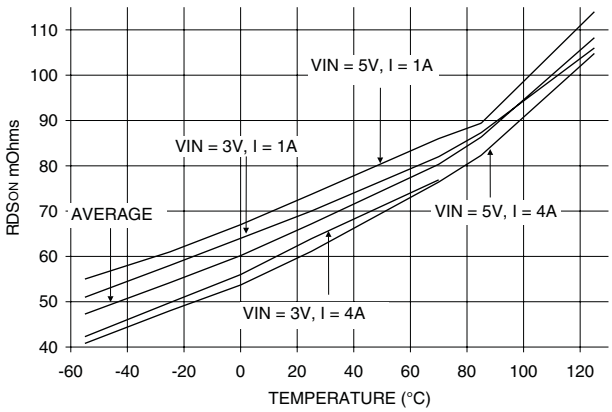


Figure 10. RDS_{ON} vs temperature.

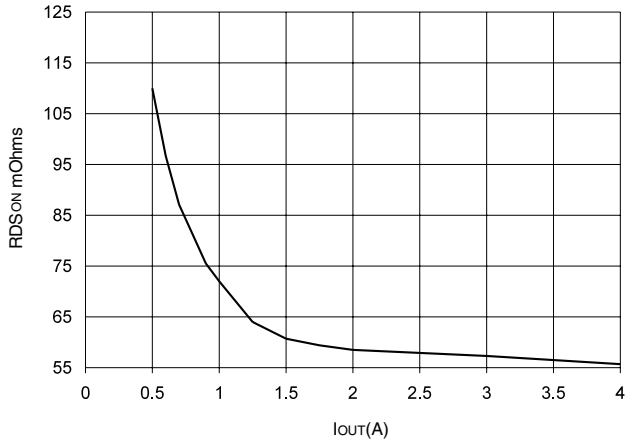


Figure 9. RDS_{ON} vs I_{OUT}.

SAFETY RECOMMENDATIONS

Although the UCC3918 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3918 is intended for use in safety critical applications where UL© or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the power device. The UCC3918 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

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