UNITRODE

PRELIMINARY

Enhanced Single Cell Lithium-Ion Battery Protection IC

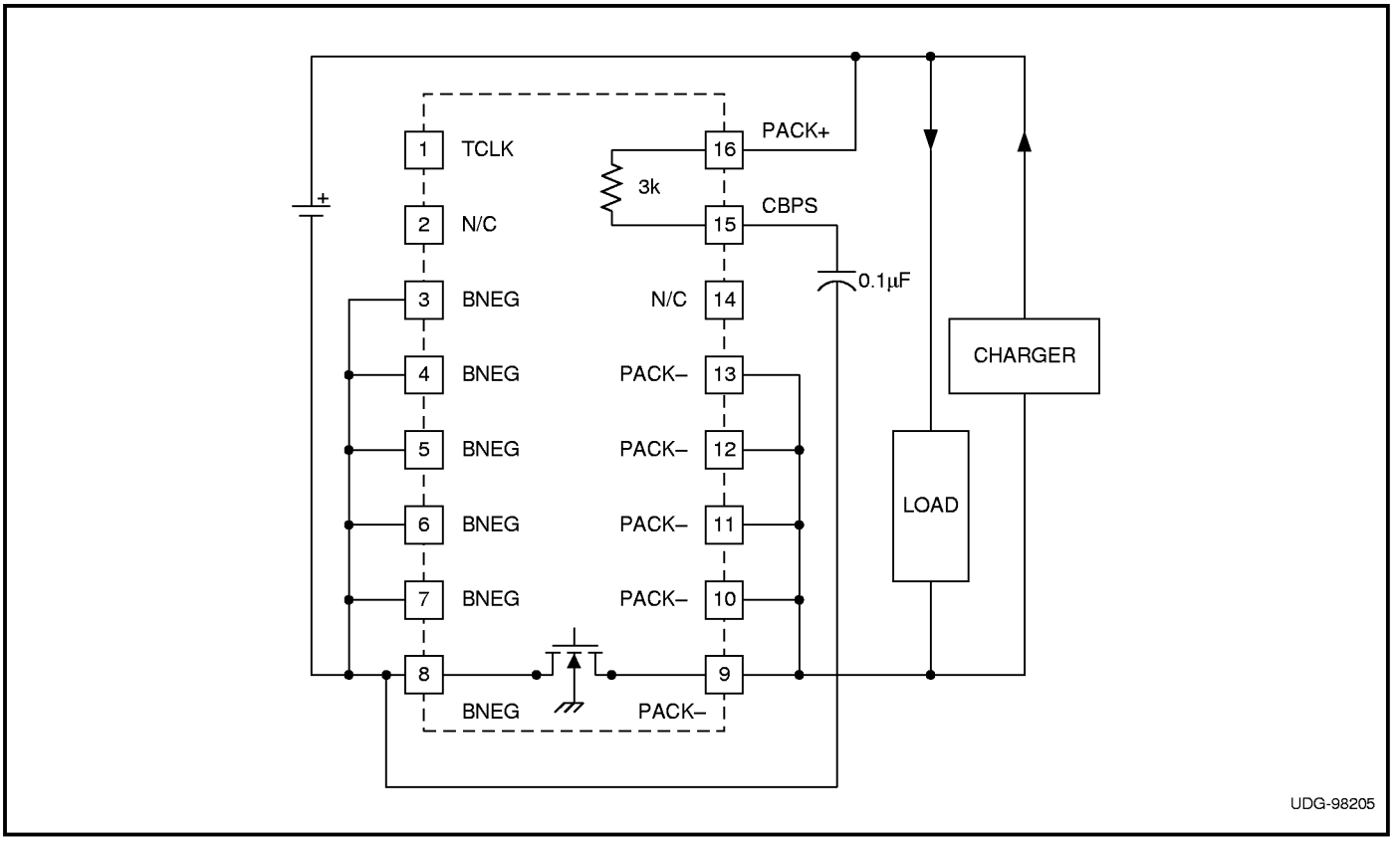
FEATURES

- Protects sensitive Lithium Ion cells from over-charging and over-discharging
- Dedicated for one cell applications
- Integrated low impedance MOSFET switch and sense resistor
- Precision trimmed overcharge and overdischarge voltage limits
- Extremely low power drain
- 2A current capacity
- Overcurrent and Short Circuit Protection
- Reverse Charger Protection
- Thermal Protection

DESCRIPTION

The UCC3952 is a monolithic BiCMOS lithium-ion battery protection circuit that is designed to enhance the useful operating life of one cell rechargeable battery pack. Cell protection features consist of internally trimmed charge and discharge voltage limits, discharge current limit with a delayed shutdown and an ultra low current sleep mode state when the cell is discharged. Additional features include an on chip MOSFET for reduced external component count and a charge pump for reduced power losses while charging or discharging a low cell voltage battery pack. This protection circuit requires one external capacitor and is able to operate and safely shutdown in the presence of a short circuit condition.

APPLICATION DIAGRAM

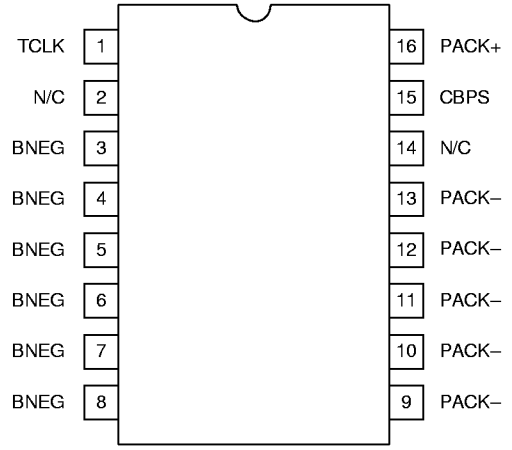


ABSOLUTE MAXIMUM RATINGS

Supply Voltage (PACK+ to BNEG) 7V
Maximum Forward Voltage (PACK+ to PACK–) 16V
Maximum Reverse Voltage
(where PACK+ to BNEG = 5V) . . . . . –8V
Maximum Cell Continuous Charge Current 3A
Junction Temperature . . . . . –55°C to 150°C
Storage Temperature Range . . . . . –40°C to 125°C

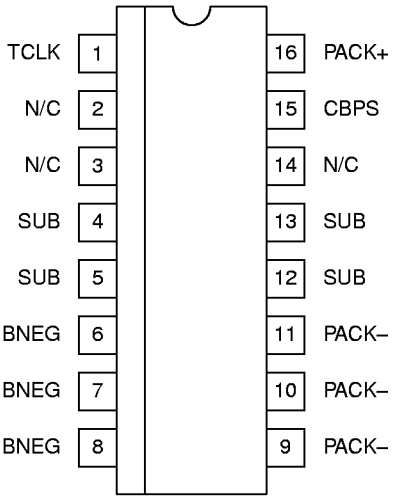
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

TSSOP-16 (TOP VIEW)
PW Package

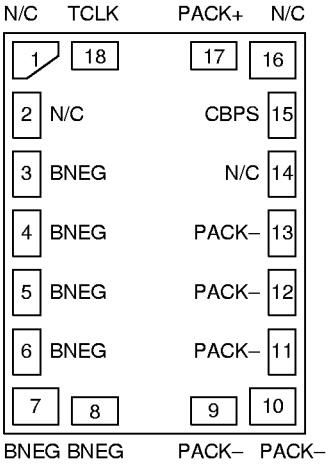


CONNECTION DIAGRAMS

SOIC-16 (TOP VIEW)
DP Package



BCC-18 (TOP VIEW)
BC Package



Consult factory for BC package availability.

ELECTRICAL CHARACTERISTICS: Temperature Range: –20°C < T_A < 70°C, Unless otherwise stated. All voltages are with respect to BNEG. $T_A = T_J$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
State Transition Threshold Section					
NORM to OV (V_{OV})	UCC3952-1	4.15	4.20	4.25	V
OV to NORM (V_{OVR})	UCC3952-1	3.85	3.90	3.95	V
NORM to OV (V_{OV})	UCC3952-2	4.20	4.25	4.30	V
OV to NORM (V_{OVR})	UCC3952-2	3.90	3.95	4.00	V
NORM to OV (V_{OV})	UCC3952-3	4.25	4.30	4.35	V
OV to NORM (V_{OVR})	UCC3952-3	3.95	4.00	4.05	V
NORM to OV (V_{OV})	UCC3952-4	4.30	4.35	4.40	V
OV to NORM (V_{OVR})	UCC3952-4	4.00	4.05	4.10	V

ELECTRICAL CHARACTERISTICS: Temperature Range: –20°C < T_A < 70°C, Unless otherwise stated. All voltages are with respect to BNEG. $T_A = T_J$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
State Transition Threshold Section (cont.)					
OV Delay Time (T_{OV})		1		2	sec
NORM to UV (V_{UV})	UCC3952-1, UCC3952-2, UCC3952-3, UCC3952-4	2.25	2.35	2.45	V
UV to NORM (V_{UVR})	UCC3952-1, UCC3952-2, UCC3952-3, UCC3952-4	2.55	2.65	2.75	V
Overdischarge Delay Time (T_{OD})		10	25	40	ms
Short Circuit Protection Section					
ITHLD	Discharge current limit, PACK+ = 3.7V	3.0		4.5	A
TDLY	Discharge current delay, PACK+ = 3.7V, I = 6A	1		2.5	ms
R_{RESET}	Discharge current reset resistance, PACK+ = 4.0	7.5			MΩ
Bias Section					
IDD	Normal operating current. $V_{UV} < V_{PACK} < V_{OV}$		5	8	µA
	Operating current in overvoltage $V_{OV} < V_{PACK}$		11	14	µA
	Shutdown operating current $V_{PACK} < V_{UV}$			2.5	µA
V_{MIN}	Minimum cell voltage when all circuits are guaranteed to be fully functional			1.7	V
FET Switch Section					
V_{PACK}–	PACK+ > V_{OV}, I(SWITCH) = 1mA to 2A Battery overcharged state switch permits discharge current only.		100	400	mV
V_{PACK}–	PACK+ = 2.5V, I(SWITCH) = –1mA to –2A Battery overdischarged state switch permits charge current only.	–600	–100		mV
R_{ON}	In Normal Mode (when not in OV or UV). This value includes package and bondwire resistance. PACK+ = 2.5V		50	75	mΩ
Thermal Shutdown Section					
TS	Thermal shutdown temperature. (Note 1)		135		°C

Note 1. This parameter is guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

BNEG: Connect the negative terminal of the battery to this pin.

PACK+: Connect to the positive terminal of the battery. This pin is available to the user.

CBPS: This power supply bypass pin is connected to PACK+ through an internal 10K resistor. An external 0.1µF capacitor must be connected between this pin and BNEG.

PACK–: The negative terminal of the battery pack (negative terminal available to the user). The internal FET switch connects this terminal to the BNEG terminal to give the battery pack user appropriate access to the battery. In an over-charged state, only discharge current is permitted. In an over-discharged state, only charge current is permitted.

SUB: (DP Package Only) Do not connect. These pins must be electrically isolated from all other pins. These pins may be soldered to isolated coppper pads for heatsinking. However, most applications do not require heatsinking.

TCLK: Production Test Mode pin. This pin is used to provide a high frequency clock to the IC during production testing. In an application this pin may be left unconnected, or tied to BNEG.

APPLICATION INFORMATION

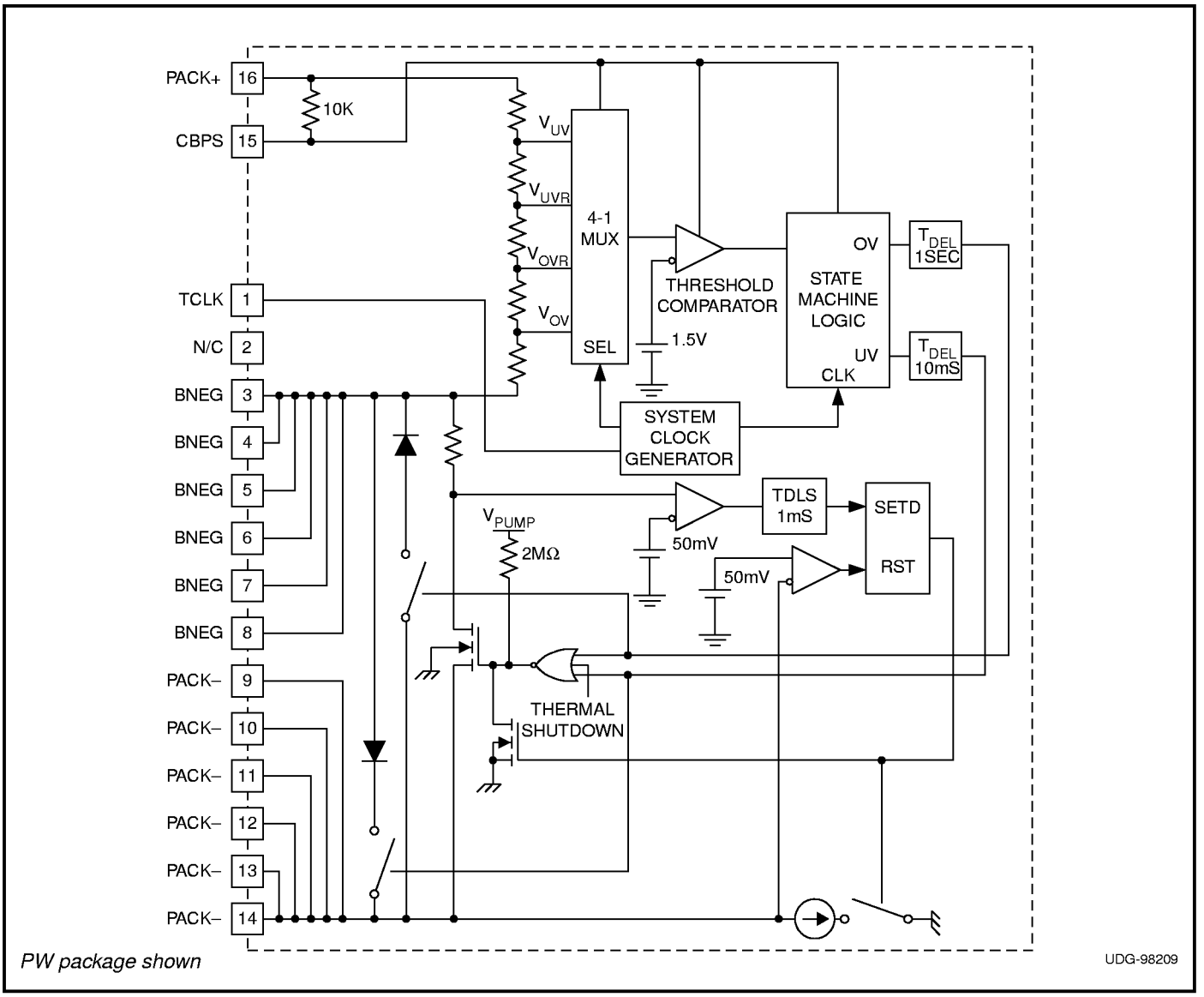


Figure 1. Detailed block diagram.

APPLICATION INFORMATION

Fig. 1 shows a detailed block diagram of the UCC3952.

Battery Voltage Monitoring

The battery cell voltage is sampled every 8ms by connecting a resistor divider across it and comparing the resulting voltage to a precision internal reference voltage. Under normal conditions (cell voltage is below Over Voltage threshold and above Under Voltage threshold), the UCC3952 consumes less than 10µA of current and the internal MOSFET is fully turned on with the aid of a charge pump.

When the cell voltage falls below the Under Voltage threshold for two consecutive samples, the IC disconnects the load from the battery pack and enters a super low power mode. The pack will remain in this state until it detects the application of a charger, at which point charging is enabled. The requirement of two consecutive readings below the UV threshold filters out momentary drops in cell voltage due to load transients, preventing nuisance trips.

If the cell voltage exceeds the Over Voltage threshold for 1sec, charging is disabled, however discharge current is still allowed. This feature of the IC is explained further in the section on Controlled Charge/Discharge Mode.

APPLICATION INFORMATION (cont.)

Over Current Monitoring and Protection

Discharge current is continuously monitored via an internal sense resistor. In the event of excessive current, an Over Current condition is declared if the high current (over 3A) persists for over 1ms. This delay allows for charging of the system bypass capacitors without tripping the overcurrent. A 0.1µF capacitor on the CBPS pin provides momentary holdup for the IC to assure proper operation in the event that a hard short suddenly pulls the cell voltage below the minimum operating voltage.

Once an Over Current condition has been declared, the internal MOSFET turns off. The only way to return the pack to normal operation is to remove the load by unplugging the pack from the system. The overcurrent is reset when an internal pull down brings PACK(–) to within 50mV of BNEG. At this point, the pack returns to its normal state of operation.

Controlled Charge/Discharge Mode

When the chip senses an over-voltage condition, it prevents any additional charging, but allows discharge. This is accomplished by activating a linear control loop which controls the gate of the MOSFET based on the differential voltage across its drain to source terminals. The linear loop attempts to regulate the differential voltage across the MOSFET to 100mV. When a light load is applied to the part, the loop adjusts the impedance of the MOSFET to maintain 100mV across it. As the load increases, the impedance of the MOSFET is decreased to maintain the 100mV control. At heavy loads (still below "over-current" limit level), the loop will not maintain regulation and will drive the gate of the MOSFET to the battery voltage (not the charge-pump output voltage). The MOSFET $R_{DS(on)}$ in the over-voltage state will be higher than $R_{DS(on)}$ during normal operation. The voltage drop (and associated power loss) across the internal MOSFET in this mode of operation is still significantly lower than the typical solution of two external back-to-back MOSFETs, where the body diode is conducting.

When the chip senses an under-voltage condition, it disconnects the load from the battery pack and shuts itself down to minimize current drain from the battery. Several circuits remain powered and will detect placement of the battery pack into a charger. Once the charger presence is detected, the linear loop is activated and the chip allows charging current into the battery. This linear control mode of operation is in effect until the battery voltage reaches a level of V_{UVR}, at which time normal operation is resumed.

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