UCN-5890A/B AND UCN-5891A/B BiMOS II 8-BIT, SERIAL-INPUT, LATCHED SOURCE DRIVERS

FEATURES

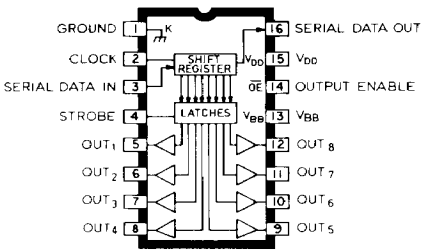
- 50 V or 80 V Source Outputs
- Output Current to −500 mA
- Output Transient-Suppression Diodes
- 3.3 MHz Minimum Data-Input Rate
- Low-Power CMOS Logic and Latches

PRIMARILY DESIGNED for use with thermal or electromagnetic printers, the UCN-5890A/B and UCN-5891A/B BiMOS II serial-input, latched drivers combine an 8-bit CMOS register, associated latches, and control circuitry (strobe and output enable) with Darlington sourcing outputs. They may also be used with relays or multiplexed LED displays within their output limitation of −500 mA per driver.

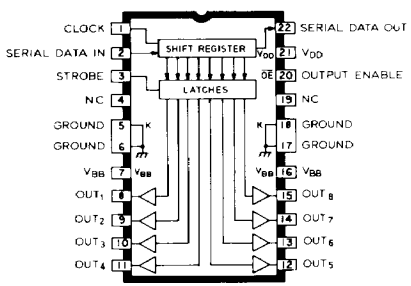
Suffix "A" devices are supplied in a standard 16-pin dual in-line plastic package. Complementary, 8-bit serial-input latched sink drivers are in Series UCN-5820A, described in Engineering Bulletin 26185.12. Suffix "B" devices are furnished in a 22-pin dual in-line package with heat-sink contact tabs that allows increased package power dissipation.

Electrical ratings for the four devices are identical except for allowable load voltage ratings. UCN-5890A and UCN-5890B are rated for operation with supply voltages of 20 V to 80 V and a minimum output sustaining voltage of 50 V. For applications using supply voltages of 20 V to 50 V (35 V sustaining), lower-cost UCN-5890A-2 and UCN-5890B-2 are recommended. The UCN-5891A and UCN-5891B are optimized for operation with supply voltages of 5 V to 50 V (35 V sustaining). A similar driver (featuring reduced output-saturation voltage), the UCN-5895A, is described in Engineering Bulletin 26182.14.

BiMOS II devices have much higher data-input rates than the original BiMOS circuits. With a 5 V supply, they will typically operate above 5 MHz. At 12 V, significantly higher speeds are obtained.



UCN-5890A
UCN-5891A



UCN-5890B
UCN-5891B

The CMOS inputs provide for minimum loading and are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors to ensure a proper input-logic high. A CMOS serial data output allows cascading these devices in multiple drive-line applications required by many dot matrix, alphanumeric, and bar graph displays.

All devices are rated for continuous operation over the temperature range of −20°C to +85°C. Because of limitations on package power dissipation, the simultaneous operation of all output drivers may require a reduction in duty cycle.

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

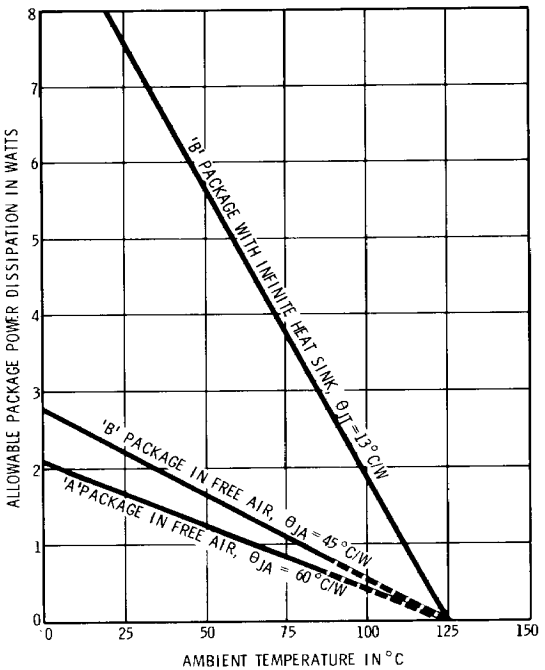
Output Voltage, V_{OUT} (UCN-5890A/B) . . . . . 80 V
(UCN-5890A/B-2) . . . . . 50 V
(UCN-5891A/B) . . . . . 50 V
Logic Supply Voltage Range, V_{DD} . . . . . 4.5 V to 15 V
Driver Supply Voltage Range, V_{BB}
(UCN-5890A/B) . . . . . 20 V to 80 V
(UCN-5890A/B-2) . . . . . 20 V to 50 V
(UCN-5891A/B) . . . . . 5.0 to 50 V
Input Voltage Range, V_{IN} . . . . . −0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT} . . . . . −500 mA
Allowable Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +125°C

Caution: Sprague Electric CMOS devices have input static protection, but are susceptible to damage when exposed to extremely high static electrical charges.

Number of Outputs ON at I_{OUT} = −200 mA	Max. Allowable Duty Cycle at T_A of					
	50°C	60°C	70°C	50°C	60°C	70°C
	Package "A"			Package "B"		
8	40%	34%	28%	53%	46%	39%
7	45%	39%	33%	60%	52%	44%
6	53%	46%	39%	70%	61%	51%
5	63%	55%	46%	84%	73%	62%
4	79%	68%	58%	100%	91%	77%
3	100%	91%	77%	100%	100%	100%
2	100%	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%	100%

Also see Allowable Output Current graphs

ALLOWABLE AVERAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



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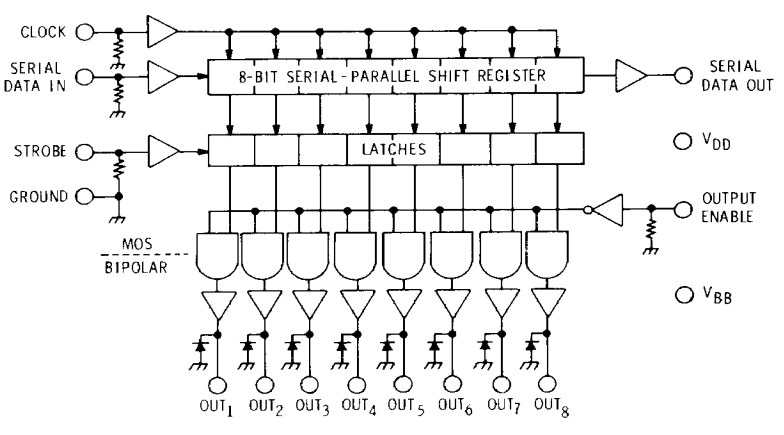
FUNCTIONAL BLOCK DIAGRAM



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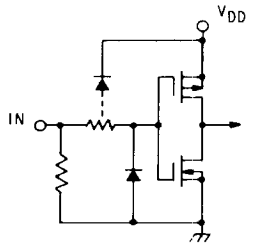
TYPICAL INPUT CIRCUIT



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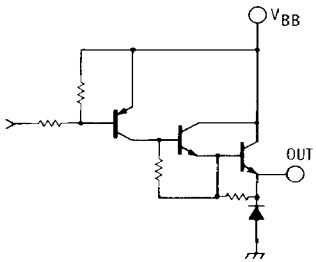
TYPICAL OUTPUT DRIVER



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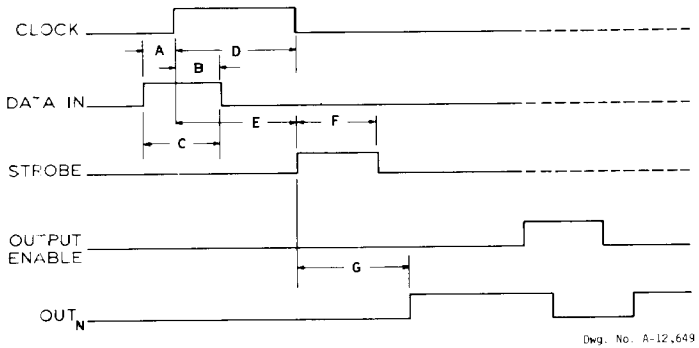
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 80 V (UCN-5890A/B) or 50 V (UCN-5890A/B-2 & UCN-5891A/B), V_{DD} = 5 V to 12 V (unless otherwise noted)

Characteristic	Symbol	V_{BB}	Test Conditions	Limits		
				Min.	Max.	Units
Output Leakage Current	I_{CEX}	Max.	T_A = +25°C	—	−50	µA
			T_A = +70°C	—	−100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	50 V	I_{OUT} = −100 mA	—	1.8	V
			I_{OUT} = −225 mA	—	1.9	V
			I_{OUT} = −350 mA	—	2.0	V
Output Sustaining Voltage	$V_{CE(sus)}$	Max.	I_{OUT} = −350 mA, L = 2 mH, UCN-5890A/B-2 & UCN-5891A/B	35	—	V
			I_{OUT} = −350 mA, L = 2 mH, UCN-5890A & UCN-5890B only	50	—	V
Input Voltage	$V_{IN(1)}$	50 V	V_{DD} = 5.0 V	3.5	5.3	V
			V_{DD} = 12 V	10.5	12.3	V
	$V_{IN(0)}$	50 V	V_{DD} = 5 V to 12 V	−0.3	+0.8	V
Input Current	$I_{IN(1)}$	50 V	V_{DD} = V_{IN} = 5.0 V	—	50	µA
			V_{DD} = V_{IN} = 12 V	—	240	µA
Input Impedance	Z_{IN}	50 V	V_{DD} = 5.0 V	100	—	kΩ
			V_{DD} = 12 V	50	—	kΩ
Clock Frequency	f_c	50 V		3.3	—	MHz
Serial Data Output Resistance	R_{OUT}	50 V	V_{DD} = 5.0 V	—	20	kΩ
			V_{DD} = 12 V	—	6.0	kΩ
Turn-ON Delay	t_{PLH}	50 V	Output Enable to Output, I_{OUT} = −350 mA	—	2.0	µs
Turn-OFF Delay	t_{PHL}	50 V	Output Enable to Output, I_{OUT} = −350 mA	—	10	µs
Supply Current	I_{BB}	50 V	All outputs ON, All outputs open	—	10	mA
			All outputs OFF	—	200	µA
	I_{DD}	50 V	V_{DD} = 5 V, All outputs OFF, Inputs = 0 V	—	100	µA
			V_{DD} = 12 V, All outputs OFF, Inputs = 0 V	—	200	µA
			V_{DD} = 5 V, One output ON, All inputs = 0 V	—	1.0	mA
			V_{DD} = 12 V, One output ON, All inputs = 0 V	—	3.0	mA
Diode Leakage Current	I_R	Max.	T_A = +25°C	—	50	µA
			T_A = +70°C	—	100	µA
Diode Forward Voltage	V_F	Open	I_F = 350 mA	—	2.0	V

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.



TIMING CONDITIONS

(V_{DD} = 5.0 V, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) . . . . . 75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) . . . . . 75 ns
C. Minimum Data Pulse Width . . . . . 150 ns
D. Minimum Clock Pulse Width . . . . . 150 ns
E. Minimum Time Between Clock Activation and Strobe . . . . . 300 ns
F. Minimum Strobe Pulse Width . . . . . 100 ns
G. Typical Time Between Strobe Activation and Output Transition . . . . . 1.0 µs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

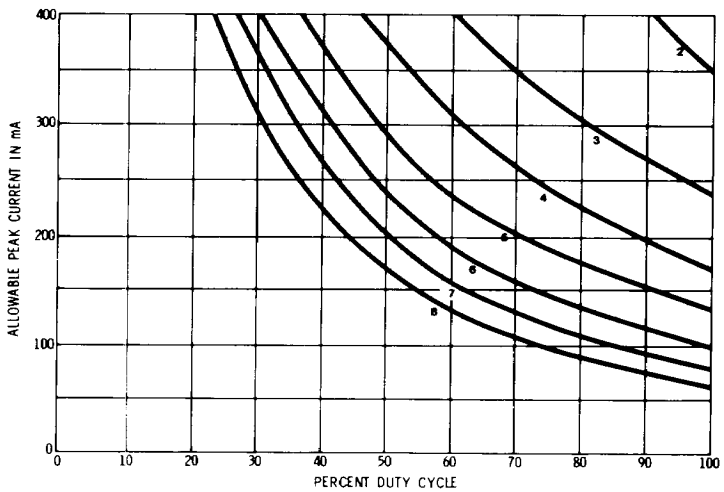
TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Output Enable	Output Contents
		I_1 I_2 I_3 . . . I_{N-1} I_N			I_1 I_2 I_3 . . . I_{N-1} I_N		I_1 I_2 I_3 . . . I_{N-1} I_N
H	⎍	H R_1 R_2 . . . R_{N-2} R_{N-1}	R_{N-1}				
L	⎍	L R_1 R_2 . . . R_{N-2} R_{N-1}	R_{N-1}				
X	⎎	R_1 R_2 R_3 . . . R_{N-1} R_N	R_N				
		X X X . . . X X	X	L	R_1 R_2 R_3 . . . R_{N-1} R_N		
		P_1 P_2 P_3 . . . P_{N-1} P_N	P_N	H	P_1 P_2 P_3 . . . P_{N-1} P_N	L	P_1 P_2 P_3 . . . P_{N-1} P_N
					X X X . . . X X	H	L L L . . . L L

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE at +25°C Free-Air Temperature

UCN-5890A AND UCN-5891A



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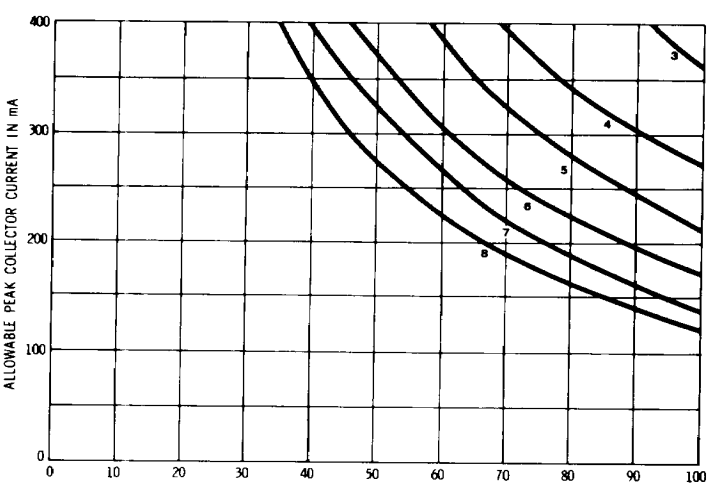
UCN-5890B AND UCN-5891B



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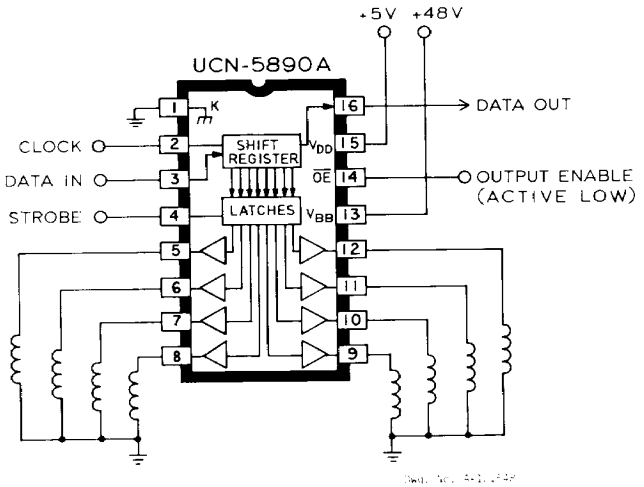
TYPICAL APPLICATIONS

SOLENOID OR RELAY DRIVER



MULTIPLEXED INCANDESCENT LAMP DRIVER