MATRA
DESIGN SEMICONDUCTOR

preliminary data sheet

UNIVERSAL LOGIC CIRCUIT (ULC)(tm) DEVICES

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FEATURES

- Factory-customized pin- and function-compatible replacements for field-programmable PAL(tm), GAL(tm), FPLA, and FPLS devices, and other PLDs

- Completely turnkey conversion to ULC devices using ABEL(tm) design files and two samples of the field-programmed PLD
  - MDS completes conversion and develops test vectors using automatic tools
  - Factory-customized ULC devices shipped fully marked and tested

- 25-50% cost-reduction from ULC devices compared to field-programmable devices
  - Highly compacted dice due to efficient architecture and sub-micron technology
  - Up to 25% cost-reduction for slower (15ns) PAL/GAL/FPLA/FPLS devices
  - Up to 50% and even higher cost-reduction high-speed (10/12ns) PAL/GAL devices and larger PLDs

- Quality improvement
  - Each ULC device tested for functional, DC and AC specifications
  - Target PPM level of 100 compared to 5,000-10,000 PPM for one-time field programmable devices
  - Saves time on expensive board rework possibly needed with partially tested field-programmable devices
  - Eliminates need for sockets used in production boards to make above rework easy

- Power consumption reduction
  - ULC device power consumption roughly 5-15mA
  - Cuts power to 5-10% of bipolar field-programmable devices and 10-15% of CMOS devices

- Simpler manufacturing
  - Eliminates need for in-house programming, testing or labeling, saving an additional 20-25%
  - Reduces manufacturing costs and leadtime

Disclaimer

This specification is subject to change without notice. Matra Design Semiconductor (MDS) assumes no responsibility for any errors contained herein.

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1. OVERVIEW

Programmable logic is an excellent tool for design development. In production, where cost, quality, power consumption, and programming overhead are important considerations, Matra Design Semiconductor (MDS) offers ULC (tm) devices as a preferable alternative to PAL(R) devices, GAL(R) devices, FPLAs, FPLSs, and other PLDs.

ULC (Universal Logic Circuit) devices are factory-customized circuits that implement pin- and function-compatible replacements for field-programmable logic devices. Devices that can be replaced on a completely turnkey basis without customer engineering involvement are listed in Section 5. Other PLDs can also be supported, but may require customer engineering support. Among PAL and GAL devices, FPLAs and FPLSs, MDS focuses on 10 and 15ns devices.

2. BENEFITS OF ULC DEVICES

2.1 Cost Reduction

With highly compacted dice, a high-yielding manufacturing technology, and sub-micron feature sizes, ULC devices use significantly less silicon per gate than field-programmable devices. The resulting cost-reduction, including mask- and prototype-making costs, ranges between 25% for slower (15ns) PAL devices to 50% and even higher for high-speed (12/10ns) PAL devices and larger PLDs.

2.2 Quality Improvement

One-time field-programmable devices are tested only partially since complete verification requires programming. As a result, one-time field-programmable devices exhibit high ppm levels in the range of 5,000-10,000 ppm.

MDS ULC devices are built to meet 100 ppm levels. They are 100% tested at the wafer and package levels at the factory. See section 6 on 'Testing'.

Further, most field-programmable devices are typically tested after programming only for correct programming (fuse map verification), which does not necessarily guarantee correct operation. Any functional testing performed is typically basic due to (i) the limited testing capability of the programming environments, and (ii) the limited number of test patterns typically generated to perform the tests. Limited testing of the nature described above makes boards manufactured with these devices susceptible to failure at final test. This reduces manufacturing yield of the board or system, and raises product cost, or requires extra time, money, labor and materials for rework. This also reduces manufacturing thruput.

MDS ULC devices are tested with more extensive tests generated with automatic test vector generation software. (See section 3 for design flow.) The software develops patterns to achieve a high degree of test coverage, or in other words, ensures that the circuit is substantially exercised in the testing process. Coupled with the fact that each device is tested at least twice before leaving the MDS factory, this reduces failure rates to less than 1 in 10,000 (100 ppm).

This difference is significant to systems manufacturers for improving system yields, manufacturing cost and manufacturing thruput - factors that are especially important in volume markets.

2.3 Power Consumption Reduction

The power consumption for bipolar PAL

devices is rated around 150-200mA, and for CMOS PAL/GAL devices around 75-100mA. ULC power consumption, although a strong function of device clock rates, typically lies between 5-15mA. This cuts power by a factor of 10-15 compared to bipolar field-programmable devices, and by a factor of 5-10 compared to CMOS field-programmable devices. Further, this is accomplished without putting the device in a standby mode, and thus without the latencies and extra logic associated with standby operation.

2.4 Simpler Manufacturing

Elimination of need for in-house programming, testing or labeling, reduces cost by an additional 20-25%. Elimination of sockets in environments where the field-programmed devices are not tested prior to placement on the board, can save another 5-10%.

3. DESIGN FLOW

MDS uses the ABEL(tm) PLD design language as its preferred input format. MDS uses proprietary software to perform logic reduction and translation, and for functional and timing verification of the translated database. The verified final database is used to generate the factory-programmed parts and the test programs for manufacturing test. The logic translation and test generation are done automatically by MDS engineers, eliminating the need for the customer to spend any engineering effort in most cases. This reduces the customer effort needed for the conversion to the same as that needed for working with the local programming and test service bureau, distributor, or in-house production programming organization. At the same time, the cost, quality, and power consumption of ULC devices is superior to the field-programmed alternatives.

Figure 3-1 on the next page shows the steps executed in the conversion process. The steps are described in further detail below.

3.1 Boolean Equation Conversion

ABEL-format equations are converted to the programming database using automatic conversion software.

3.2 Test Program Generation and Verification

The converted database is used to generate the test vectors. These test vectors are verified for correctness by running them against one or two programmed samples of the field-programmed device. This process also indirectly verifies the correctness of the conversion.

3.3 Programmed Device Generation

With the converted design verified, MDS processes the programming data to build the factory-programmed devices.

3.4 Testing of Programmed Devices

The programmed devices are tested for functional, DC and AC specifications at the wafer sort and final test level. See section on Testing.

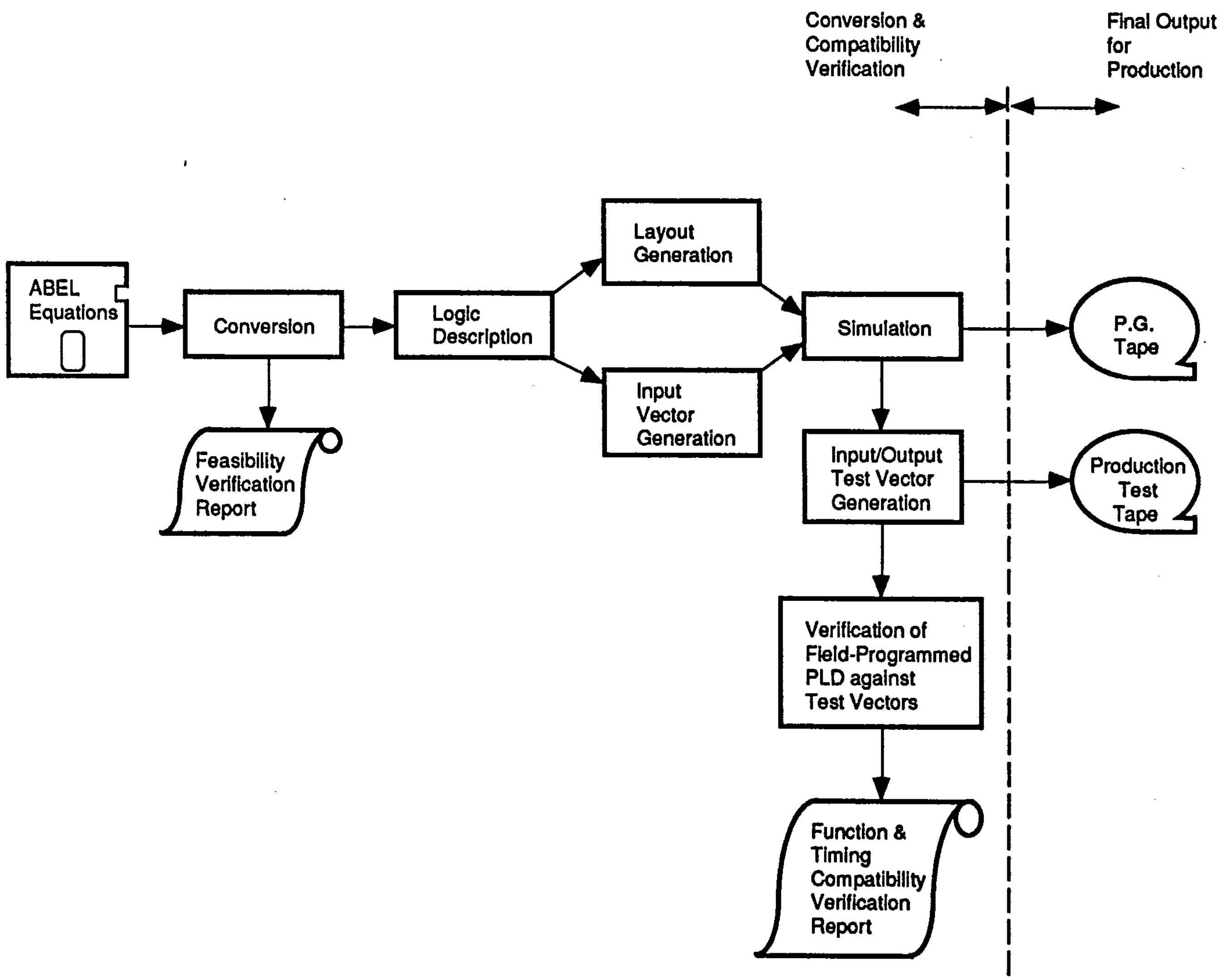

Figure 3-1: Automatic PAL/GAL/FPLS/FPLA/PLD Device Replacement Flow

4. TECHNOLOGY

MDS uses advanced sub-micron CMOS technology in its ULC devices. The n-transistor channel lengths are sized at 0.8-microns (drawn). This technology offers toggle rates in excess of 200 MHz and system clock rates in excess of 125MHz. The technology is also designed for cost-effective volume production, and thus offers state-of-the-art performance combined with highly predictable and cost-effective manufacturability. ULC devices using this technology has been in production since late 1988.

5. FIELD PROGRAMMABLE DEVICES SUPPORTED

5.1 Architectures

The following chart shows the PAL/PLD devices MDS can replace with ULC devices on a completely turnkey basis:

ULC20 Devices	ULC24 Devices	ULC28 Devices	ULC40 Devices
GAL16V8	GAL20V8	PLS100	PAL32R16
PAL18P8	GAL39V18	PLS101	EP900
PAL16P8	PAL29M16	PLS103	EP910
PAL16L8	PAL32VX10	PLS105	EP1200
PAL10L8	PAL22V10	PLUS405	
PAL12L6	PAL22RX8		
PAL14L4	PAL20RS10		
PAL16L2	PAL20RS8		
PAL23S8	PA20RS4		
PAL16RP8	PAL20X10		
PALRP6	PAL20X8		
PAL16RP4	PAL20X4		
PAL16R8	PAL20RP10		
PAL16R6	PAL20RP8		
PAL16R4	PAL20RP6		
PLS151	PAL20RP4		
PLC153	PAL20R8		
PLS153	PAL20R6		
PLHS153	PAL20R4		
PLUS153	PLS161		
PLS155	PLS162		
PLS157	PLS163		
PLS159	PLS167		
EP310	PLS168		
EP320	PLS173		
	PLS179		
	PLS473		
	PLHS473		
	PLUS173		

5.2 Speeds

The following table shows the standard speed versions of various PLDs supported:

PLD	Speed Versions Supported
PAL Devices	10ns, 12ns, 15ns, 25ns
GAL Devices	10ns, 12ns, 15ns, 20ns, 25ns
FPLAs/ FPLSs	12ns, 15ns, 20ns, 22ns, 25ns
Other PLDs	All speeds

MDS can also support other speeds not available as standard selections in field-programmable devices, at a slightly higher cost. For example, 10-ns 22V10s can be supported, even though field programmable versions that run as fast are not available.

7.5ns ULC devices are expected to be available in Q1 '90.

5.3 Packages

MDS provides the ULC devices in packages compatible and equivalent to those used for the field-programmable devices. This includes plastic DIPs, skinny DIPs, PLCCs, quad flatpaks, and ceramic DIP/CERDIP equivalents as available. Windowed packages are substituted by windowless equivalents.

6. TESTING ULC DEVICES

Each ULC device is tested twice after it has been programmed, before it is shipped to a customer. The first set of tests, consisting of DC and functional tests, are done on each device after programming and prior to packaging. The second and final set, consisting of functional, DC and AC tests, are done on each device after packaging. Re-testing, consisting of functional, DC and AC tests, is also done for quality assurance on a lot sampling basis.

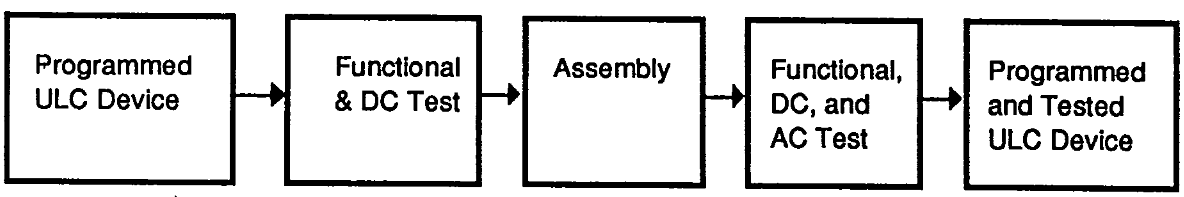

Figure 6-1: Flow diagram for testing customized ULC devices

7. ELECTRICAL SPECIFICATIONS

7.1 Maximum Ratings

V_{DD} level with reference to V_{SS}	-0.5 to +6.5V
Minimum voltage on any other pin	-0.5V
Maximum voltage on any other pin	VCC + 0.5V
Storage temperature	-65 deg C to +110 deg C.
Static discharge voltage (per Mil Std 883 Method 3015)	>2000V

7.2.1 Operating Limits (0 to 70 deg C, 5V ± 10%)

7.3 D.C. Characteristics

Parameter	Description	Min	Max	Unit	Test Conditions
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = -24mA
V_{OL}	Output LOW Voltage		0.5	V	I_{OL} = 24mA
V_{IH}	Input HIGH Voltage	2.0		V	
V_{IL}	Input LOW Voltage		0.8	V	
I_{IX}	Input Leakage Current	-10	+10	uA	$V_{SS}<V_{IN}<V_{CC}$
I_{OZ}	Output Leakage Current	-40	+40	uA	$V_{SS}<V_{OUT}<V_{CC}$
I_{CSB}	Standby Current		5	mA	V_{CC} = Max; V_{IN} = GND; Outputs open
I_{CC}	Power Supply Current		6	mA	V_{CC} = Max; V_{IN} = GND; Outputs Open; F_{op} = 1MHz (1)

Note
1. Measured at F_{op} = 1MHz.

7.2.2 A.C. Characteristics (T_{CASE} = 0 deg C to +70 deg C; V_{CC} = 5V + 5%)

All A.C. parameters are guaranteed to be equal to or better than the field-programmable devices being replaced.

8. ORDERING INFORMATION

8.1 Part Number

ULCXX	/	XXXXXXXXXXXXXXXXXXXX
Mask-Programmed Universal Logic Device		Complete Part Number of Field-Programmable Device, including Manufacturer prefix, device, part number, speed, package, and temperature range

For an example, see figure 8-1 below. If you use more than one vendor manufacturer of the field programmable device, please specify the manufacturer offering the more stringent specification, if there is a difference. If there is no difference, vendor identification is optional.

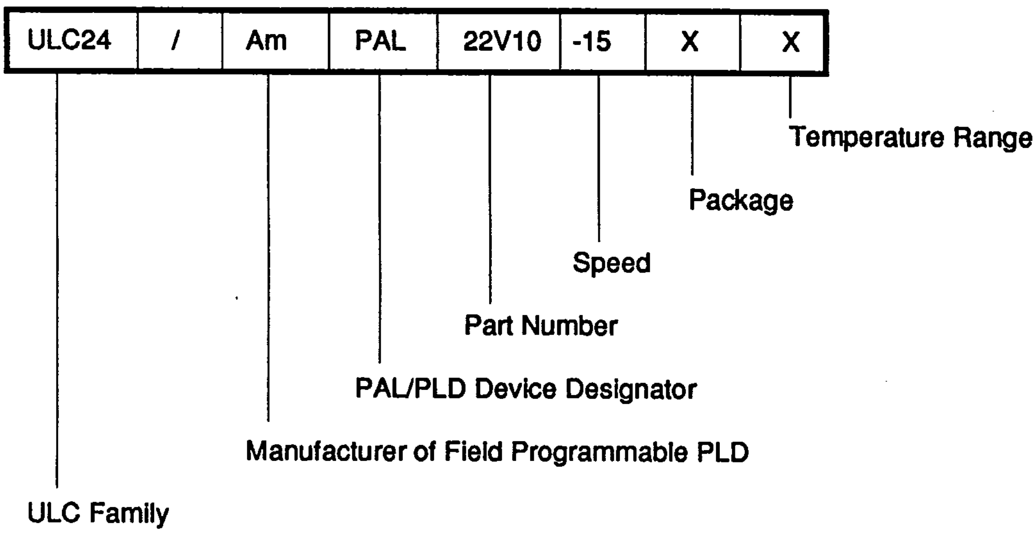

Figure 8-1: Example part number for replacement of a 15ns 22V10 in a 24-pin PDIP

8.2 Leadtimes

From the time that a customer provides the ABEL boolean equations describing the field-programmable device configuration, along with 2-3 programmed samples, MDS uses automatic software to convert the equations to the ULC device configuration and test data, and delivers fully compatible samples six weeks later. Small pre-production quantities can also be delivered at the same time. First production parts are available four weeks later.

8.3 How to Order

To submit a code and place an order, contact your local MDS representative or MDS headquarters at 800-338-GATE.