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MATRA
DESIGN SEMICONDUCTOR

UNIVERSAL LOGIC CIRCUIT (ULC)(tm) DEVICES

preliminary data sheet

September 1991

FEATURES

- Mask Programmed pin- and function-compatible replacements for field-programmable PAL(tm), GAL(tm), FPGA devices and other PLDs
- Turnkey conversion to ULC devices
- 25-50% cost-reduction with ULC devices compared to field-programmable devices
  - Highly compacted dice due to efficient architecture and sub-micron technology
- PAL & GAL speeds supported
  - 7.5, 10 and 15 ns
- Quality improvement
  - Each ULC device tested for functional, DC and AC specifications
  - Target PPM level of 250 compared to 5,000-10,000 PPM for one-time field-programmable devices
- Reduces power consumption by 90-95% of bipolar devices and 85-90% of CMOS devices
  - ULC device power consumption approximatly 5-15mA
- Simpler manufacturing
  - Eliminates need for in-house programming, testing or labeling
  - Reduces manufacturing costs and leadtime

1. OVERVIEW

Programmable logic is an excellent tool for design development. In production, where cost, quality, power consumption, and programming overhead are important considerations, Matra Design Semiconductor (MDS) offers ULC(tm) devices as a preferable alternative to PAL(R) devices, GAL(R) devices, FPGAs and other PLDs.

ULC (Universal Logic Circuit) devices are factory-customized circuits that implement pin- and function-programmable logic devices. MDS has configured computer-aided tools around a proprietary design flow which enable ULC conversions to be completed on a turnkey basis in most cases. Replacements for PAL, GAL and simple PLD devices are implemented without requiring any customer engineering involvement. For large PLDs, some assistance from the system designer is needed for thorough design verification.

A representative list of devices supported by MDS is shown in Section 2. This list is not exhaustive. Additional devices not shown in this list are also supported. Among PAL and GAL devices, MDS focuses on 7.5, 10 and 15ns devices.

Oder No.: dsULC/r1.2

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Disclaimer

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1. TECHNOLOGY

MDS uses advanced sub-micron CMOS technology in its ULC devices. The n-transistor channel lengths are sized at 0.8-microns (drawn). This technology offers toggle rates in excess of 200 MHz and system clock rates in excess of 125 MHz. The technology is also designed for cost-effective volume production, and thus offers state-of-the-art performance combined with highly predictable and cost-effective manufacturability. ULC devices using this technology have been in production since late 1988.

2. FIELD PROGRAMMABLE DEVICES SUPPORTED

2.1 Architectures

The device listed in Table 1 are representative of PAL/PLD devices that can be replaced with ULC devices. This list is not exhaustive. For a device not included in this list, please check with an MDS salesperson. Among various PLDs supported, nearly all 20-, 24- and 28-pin devices are converted automatically without any customer involvement. Many larger PLDs are also converted automatically.

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Table 1: Summary List of ULC Devices

ULC 20 Devices	ULC 24 Devices	ULC 28 Devices	ULC 68 Devices
GAL16V8	GAL20V8	85C508	PLHS502
PAL16P8	PAL22V10	PAL22V10	PLHS601
PAL18P8	PAL22RX8	85C509	EPM5128
PAL16L8	PAL20RS10	85C960	EP1830
PAL10L8	PAL20RS8	PLS100	EP1810
PAL12L6	PAL20RS4	PLS101	ACT1010
PAL14L4	PAL20X10	PLS103	ACT1020
PAL16L2	PAL20X8	PLS105	XC2064
PAL16RP8	PAL20X4	PLUS405	XC2018
PALRP6	PAL20RP10	EPM5032	XC3020
PAL16RP4	PAL20RP8		XC3030
PAL16R8	PAL20RP6	**ULC 40 Devices**	XC3042
PAL16R6	PAL20RP4		MACH120
PAL16R4	PAL20R8	5C090	MACH220
PLS151	PAL20R6	5AC324	5C180
PLC153	PAL20R4	PAL32R16	
PLS153	PLS161	EP900	**ULC 84 Devices**
PLHS153	PLS162	EP910	
PLUS153	PLS163	EP1200	ACT1010
PLS155	PLS167	ATV2500	ACT1020
PLS157	PLS168	85C090	EPM5192
PLS159	PLS173		MACH130
EP310	PLS 179	**ULC 44 Devices**	MACH230
EP320	PLS473		XC2018
EP330	PLHS473	EPM5064	XC3064
EPM5016	PLUS173	5AC324	XC3090
85C220	EP610	85C090	XC4005
5C032	EP630	ACT1010	
PEEL18CV8	ATV750	ACT1020	**ULC 100 Devices**
	85C060	MACH110	
	5C060	MACH210	EPM5130
	SAC312		XC3020
	PEEL22CV10	**ULC 52 Devices**	XC3030
			XC3042
		PLHS501	ACT1225

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3. BENEFITS OF ULC DEVICES

3.1 Cost Reduction

With highly compacted dice, a high-yielding manufacturing technology, and sub-micron feature sizes, ULC devices use significantly less silicon per gate than field-programmable devices. The resulting cost-reduction, including mask and prototype costs, ranges between 25% for slower (15ns) PAL devices to 50% and even higher for higher-speed (10/7.5ns) PAL devices and larger PLDs.

3.2 Quality Improvement

One-time field-programmable devices are tested only partially by the manufacturer since complete verification requires programming. As a result, one-time field-programmable devices exhibit high ppm defect levels in the range of 5,000-10,000 ppm.

MDS ULC devices are built to meet 250 ppm levels. They are 100% tested at the wafer and package levels at the factory. See section 5.4 on 'Testing'.

Further, most field-programmable devices are typically tested after programming only for correct programming (fuse map verification), which does not necessarily guarantee correct operation. Any functional testing performed is typically basic due to (i) the limited testing capability of the programming environments, and (ii) the limited number of test patterns typically generated to perform the tests. Limited testing of the nature described above makes boards manufactured with these devices susceptible to failure at final test. This reduces manufacturing yield of the board or system, and raises product cost, or requires extra time, money, labor and materials for rework. This also reduces manufacturing throughput.

MDS ULC devices are tested with extensive tests generated by automatic test vector generation software. (See section 5 for design flow.) The software develops patterns to achieve a high degree of test coverage, or in other words, ensures that the circuit is substantially exercised in the testing process. Coupled with the fact that each device is tested at least twice before leaving the MDS factory, this reduces failure rates to less than 1 in 10,000 (100 ppm).

This difference is significant to systems manufacturers for improving system yields, manufacturing cost and manufacturing thoroughput factors that are especially important in volume markets.

3.3 Power Consumption Reduction

The power comsumption for bipolar PAL devices is rated around 150-200mA, and for CMOS PAL/GAL devices around 75-100mA. ULC power consumption, although a strong function of device clock rates, typically lies between 5-15mA. This cuts power by a factor of 10-15 compared to bipolar field-programmable devices, and by a factor of 5-10 compared to CMOS field-programmable devices. Further, this is accomplished without putting the device in a standby mode, and thus without the latencies and extra logic associated with standby operation.

3.4 Simpler Manufacturing

Elimination of need for in-house programming, testing and labeling, reduces cost by an additional 20-25%. Elimination of sockets in environments where the field-programmed devices are not tested prior to placement on the board, can save another 5-10%.

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4. ELECTRICAL SPECIFICATIONS

4.1 Maximum Ratings

V_{DD} level with reference to V_{SS}	-0.5 to +6.5V
Minimum voltage on any other pin	-0.5V
Maximum voltage on any other pin	V_{DD} + 0.5V
Storage temperature	-65°C to +125°C
Static discharge voltage (per Mil Std 883 Method 3015)	>2000V

4.2 Operating Limits (T_{CASE} = 0° to 70°C, V_{DD} = 5V ± 5%)

4.3 D.C. Characteristics

Parameter	Description	Min	Max	Unit	Test Conditions
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = -12mA
V_{OL}	Output LOW Voltage		0.5	V	I_{OL} = 24mA
V_{IH}	Input HIGH Voltage	2.0		V	
V_{IL}	Input LOW Voltage		0.8	V	
I_{IX}	Input Leakage Current	-10	+10	uA	$V_{SS}<V_{IN}<V_{DD}$
I_{OZ}	Output Leakage Current	-40	+40	uA	$V_{SS}<V_{OUT}<V_{DD}$
I_{CSB}	Standby Current		8-20 (1)	mA	V_{DD} = 5.25V; V_{IN} = GND; Outputs open
I_{DD}	Power Supply Current		See Section 4.5	mA	V_{DD} = 5.25V; V_{IN} = GND; Outputs Open; F_{op} = 1MHz (Note)
C_{IN}	Input		5	pF	V_{DD} = 5.0V; V_{SN} = 2.0V
C_{OUT}	Output		4	pF	V_{OUT} =2.0V

Note: Measure at F_{op} = 1 MHz

(1) This parameter is device and pin count dependent.

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4.4 AC Characteristics

All A C parameters are guaranteed to be equal to or better then field-programmable devices being replaced.

ULC 20 / 16XX					
	-25	-15	-10	-7	-5
t_{pd}	25	15	10	7/7.5[1]	
t_{co}	15	12	8	6.5	
t_{su}	25	15	10	7	
t_{en}	25	15	10	10	
t_{dis}	25	15	10	10	

ULC 24 / 20XX					
	-25	-15	-10	-7	-5
t_{pd}	25	15	10	7/7.5 [1]	
t_{co}	15	12	8	6.5	
t_{su}	25	15	10	7	
t_{en}	25	15	10	10	
t_{dis}	25	15	10	10	

ULC 24 / 22XX					
	-25	-15	-10	-7	
t_{pd}	25	15	10	7.5	
t_{co}	15	10	7	6	
t_{su}	15	12	10	3	
t_{en}	25	15	10	7.5	
t_{dis}	25	15	10	7.5	

Notes:

1) 7.0 ns with one output switching, 7.5 with more than 1 output switches.

2) Setup, enable and disable times are not 100% tested but are guaranteed by design and from characterization data.

t_{pd} = Input or Feedback to Combinational Output

t_{co} = Clock to Output

t_{su} = Setup time from Input or Feedback to Clock

t_{en} = Input to Output Enable

t_{dis} = Input to Output disable

4.5 Static and Dynamic Power Consumption for CMOS ULC

Assumptions :

a. Static power dissipation due to the internal backbias generator pump can be considered negligible (typically around 2mA*5V=10mW)

b. The output buffers are driving TTL logic, i.e. sinking 24 mA and sourcing a few hundred uA.

There are 3 main factors to consider:

1. Static power dissipation in I/O buffers (24mA across VOL=0.4V):

   P1(in mW)=24mA*0.4V*No = 9.6*No
   where: No=Number of 24mA outputs

   Example: With twelve 24mA outputs, we get: P1=9.6*12=115.2mW

2. Dynamic power dissipation for the internal gates (5uA/MHz/Gate):
   P2 (in mW)=5V*0.005mA*Ni*Fi
   =0.025*Ni*Fi
   where: Ni=average number of internal gates toggling
   Fi=Clocking frequency of internal logic in MHz

   Note: A usual rule of thumb is to assume that 1/2 of the used gates are toggling at the same time.

   Example: With 100 used gates and 40 MHz internal clock,
   we get: P2=0.025*50*40=50mW

3. Dynamic power dissipation for 24mA output switching (0.02mA/MHz/Output/pf):

   P3 (in mW)=5V*Nos*Fos*(0.02*C)
   =0.1*Nos*Fos*C
   where: Nos=number of outputs switching simultaneously
   Fos=Output clocking frequency in MHz
   C=Output load capacitance in pF

Example: With 8 outputs switching simultaneously at 20 MHz and loaded with 50 pF

we get: P3=0.1*8*20*50=800mW

Global Formula:
With:

Ni=number of internal toggling gates (usual rule of thumb is 1/2 of total used gates)
Fi=Clocking frequency in MHz for the internal logic
No=Number of 24mA Outputs
Nos=Number of output switching simultaneously
Fos=Clocking frequency for the output switching simultaneously
C=Output load capacitance in pf (C≥50 pF)

we get:

Wcp (in mW)=P1+P2+P3
=(10*No)+(0.025*Ni*Fi)+(0.1*Nos*Fos*C)

Note: Wcp= Worst case power

5. DESIGN FLOW

MDS uses ABEL(tm) PLD design language as its preferred input format. Most other PLD design languages are also supported. MDS uses proprietary software to perform logic reduction and

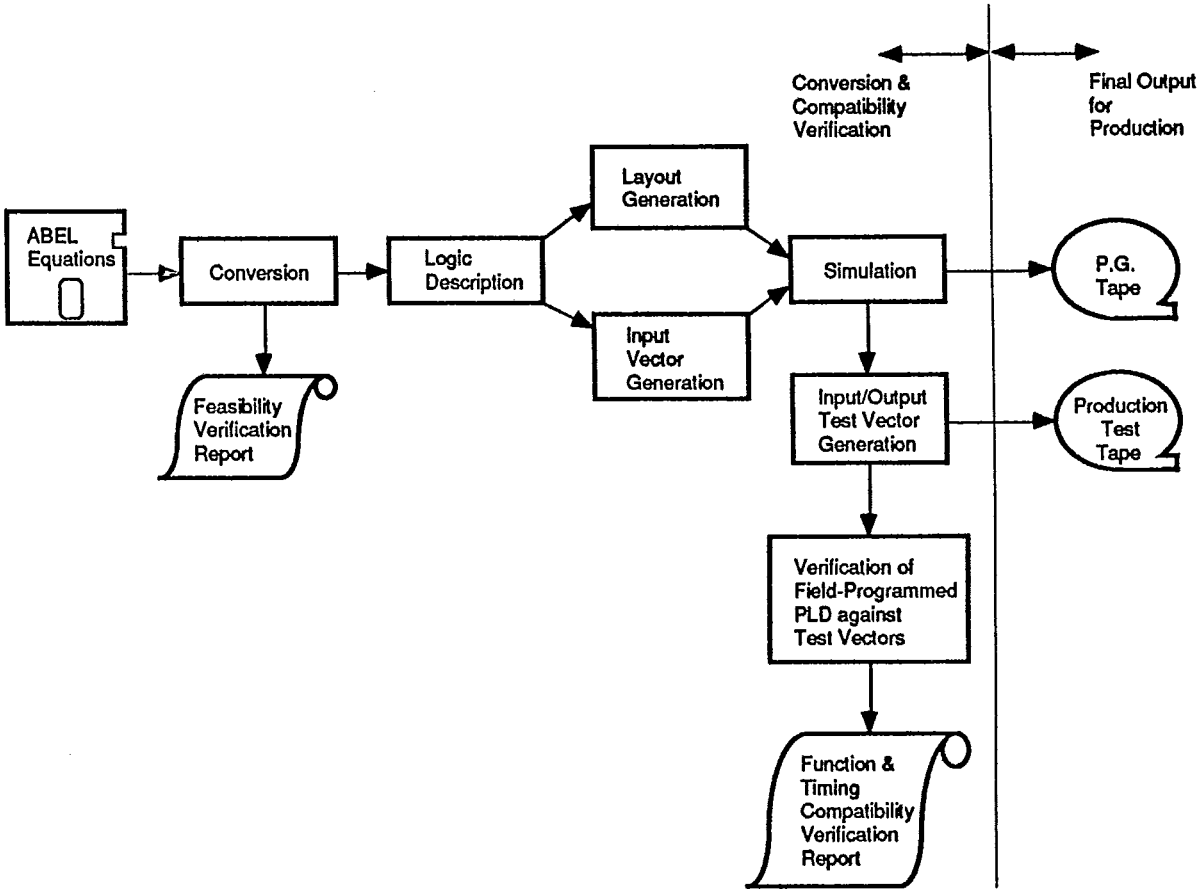

Figure 5-1: Automatic PAL/GAL/FPLS/FPLA/PLD Device Replacement Flow (Patent Pending)

translation, and for functional and timing verification of the translated database. The verified final database is used to generate the factory-programmed parts and the test programs for manufacturing test. The logic translation and test generation are done automatically by MDS, eliminating the need for the customer to spend any engineering effort in most cases. This reduces the customer effort needed for the conversion to the same as that needed for working with the local programming and test service bureau, distributor, or in-house production programming organization. At the same time, the cost, quality, and power consumption of ULC devices is superior to the field-programmed alternatives.

Figure 5-1 on previous page shows the steps executed in the conversion process. The steps are described in further detail.

5.1 Boolean Equation Conversion

ABEL-format equations are converted to the programming database using automatic conversion software.

5.2 Test Program Generation and Verification

The converted database is used to generate the test vectors. These test vectors are verified for correctness by running them against one or two programmed samples of the field-programmed device. This process also indirectly verifies the correctness of the conversion.

5.3 Programmed Device Generation

With the converted design verified, MDS processes the programming data to build the factory-programmed devices.

5.4 Testing of ULC devices

Each ULC device is fully tested, before being shipped to a customer. These tests consist of functional, DC and AC parametric tests, and are performed on each device after packaging. Automatic test Vector generation (ATVG) tools are used to generate the functional test in order to ensure very high fault covrerage within the device. Re-testing, consisting of functional, DC and AC parametric tests, is also done for quality assurance on a lot sampling basis. See Fig 5-2.

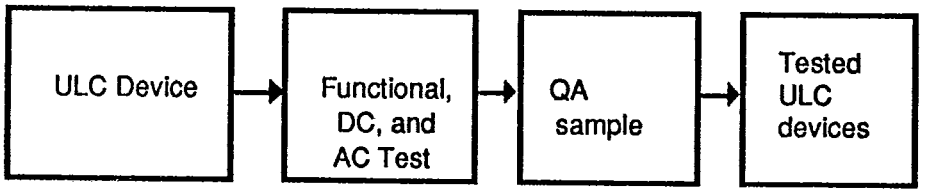

Figure 5-2: Flow diagram for testing customized ULC devices

6. Packages

MDS provides the ULC devices in packages compatible and equivalent to those used for the field-programmable devices. This includes plastic DIPs, skinny DIPs, PLCCs and quad flatpacks.

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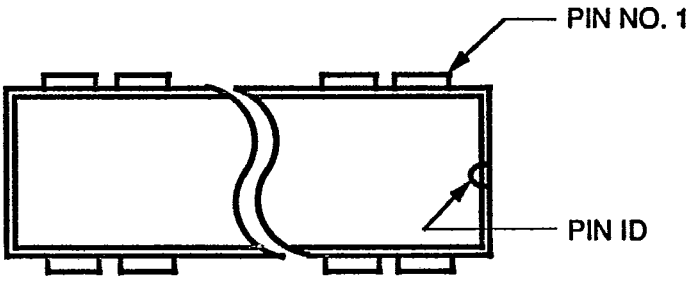
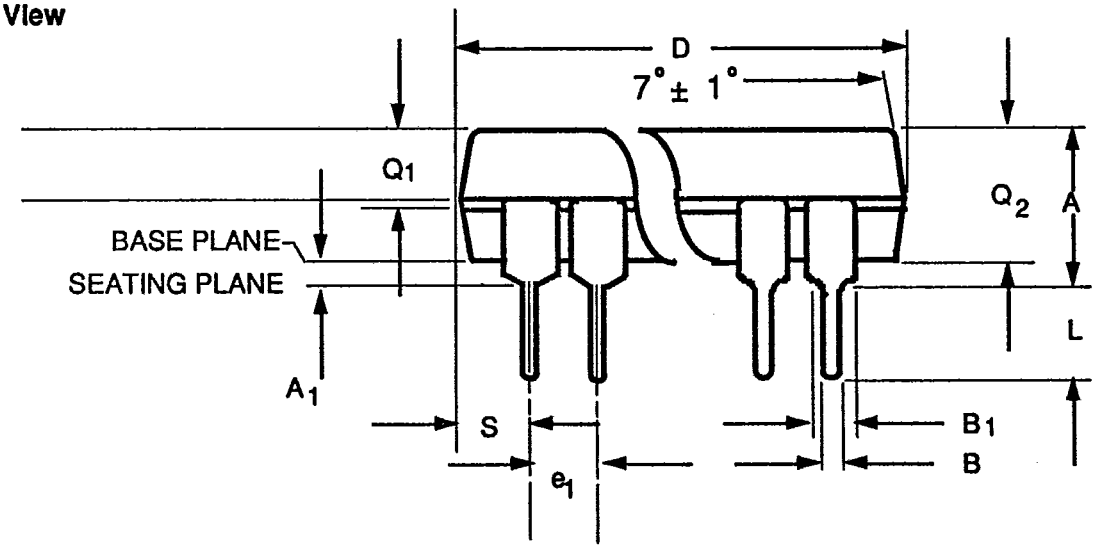
6.1 20/24-Lead Plastics DIP/Skinny DIP Package Diagrams

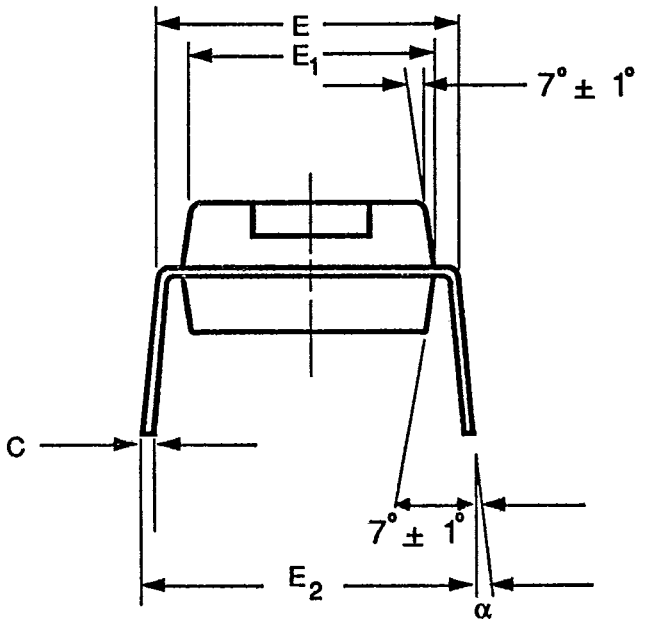
Top View



Front View



End View



6.1 20/24-Lead Plastics DIP/Skinny DIP Package Diagrams (Continued)

Sym	20-Lead Plastic-DIP		24-Lead Skinny Dip	
	Inches		Inches	
	Min	Max	Min	Max
A	0.145	0.155	----	0.200
A_1	0.020	----	----	----
B	0.018	0.020	0.014	0.023
B_1	0.058	0.082	0.038	0.065
C	0.008	0.012	0.008	0.015
D	1.028	1.032	----	1.280
E	0.298	0.302	0.220	0.310
E_1	0.248	0.252	0.290	0.320
E_2	0.335	0.355	----	----
e_1	------	------	0.100	
a_1	0.100 REF.		----	----
α	0°	16°	0°	15°
N	20		----	----
O	0.035 REF.		----	----
Q	----	----	0.015	0.060
Q_1	0.059	0.061	----	----
Q_2	0.128	0.132	----	----
S	0.063	0.067	----	0.098
L	0.128	0.132	0.125	0.200

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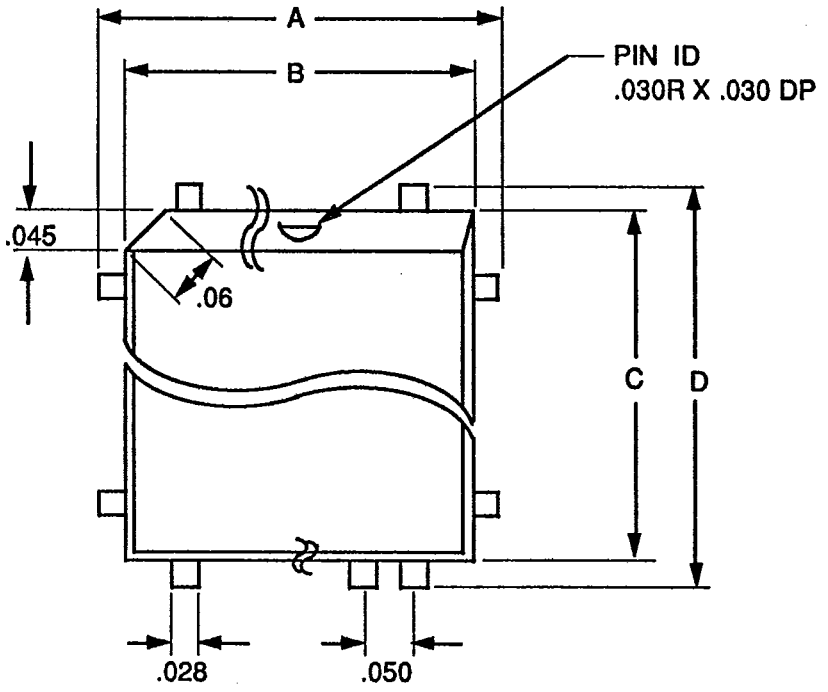
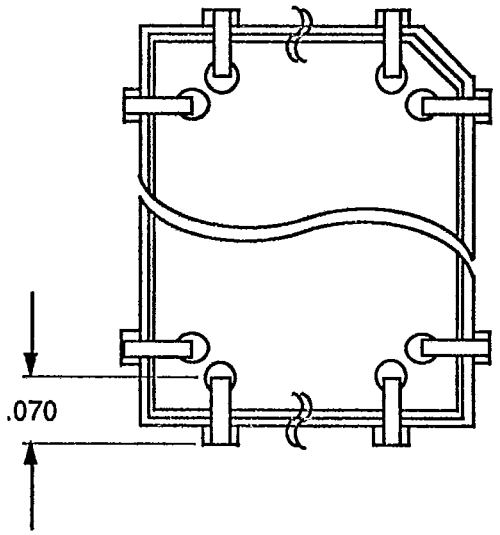
6.2 20/28-Lead PLCC Package Diagrams

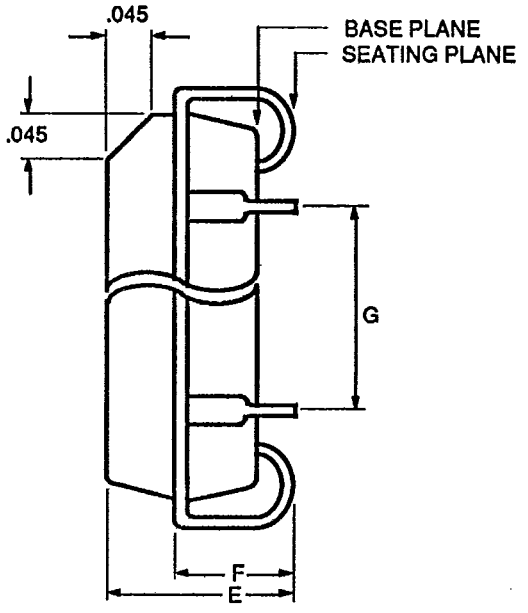
Top View



Bottom View



Right Side View



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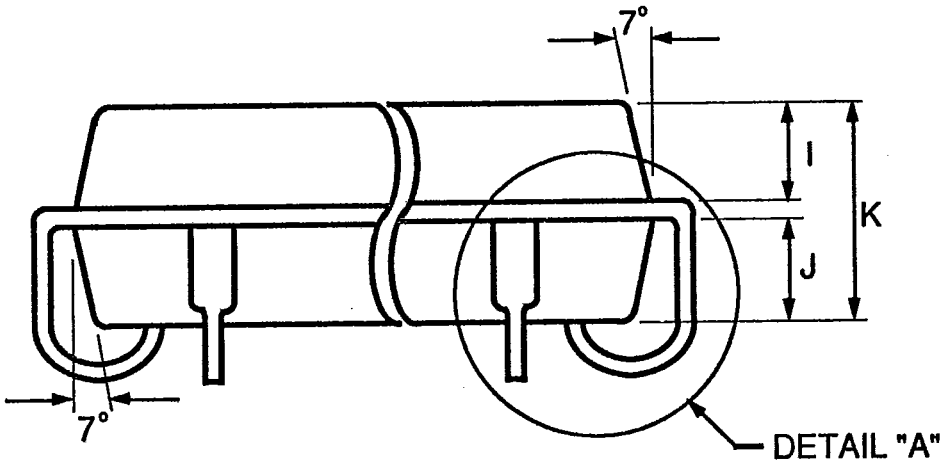
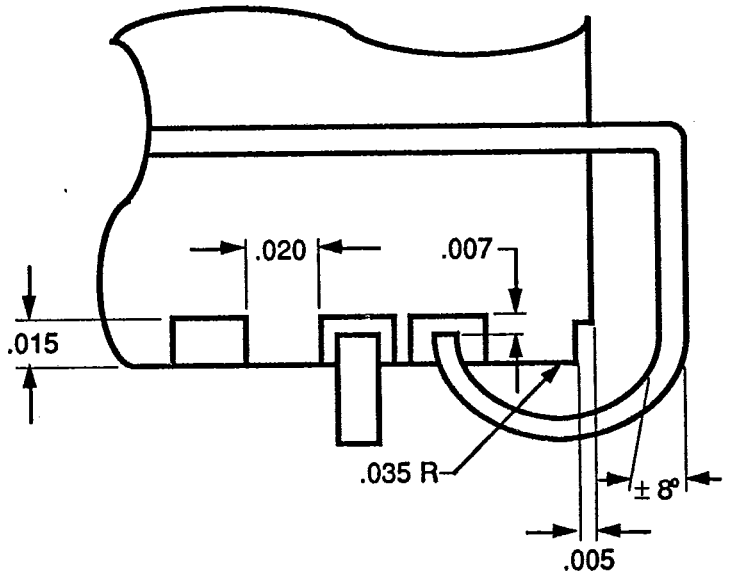
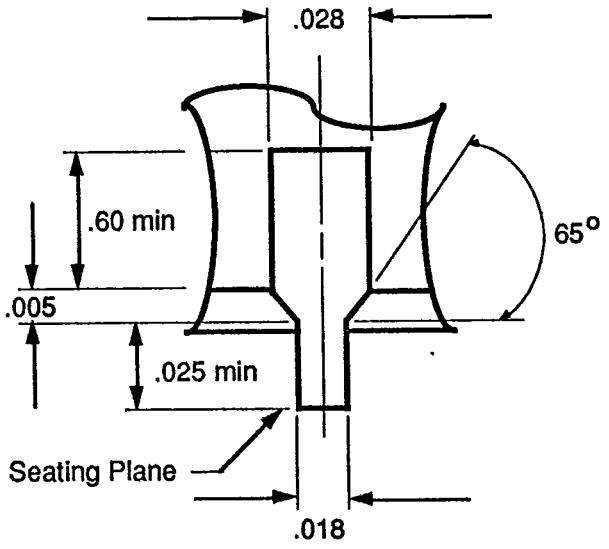
6.2 20/28-Lead PLCC Package Diagrams (Continued)

Front View



DETAIL A





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6.2 20/28-Lead PLCC Package Diagrams (Continued)

Symbol	20-Lead PLCC		28-Lead PLCC	
	Inches		Inches	
	Min	Max	Min	Max
A	0.385	0.395	0.485	0.495
B	0.300	0.320	0.452	0.456
C	0.300	0.320	0.452	0.456
D	0.385	0.395	0.485	0.495
E	0.168	0.172	0.170	0.180
F	0.168	0.172	0.100	-----
G	0.200 REF.		0.300 REF.	
I	0.068	0.072	0.070	0.072
J	0.058	0.062	0.070	0.072
K	0.143	0.147	0.148	0.152

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7. ORDERING INFORMATION

7.1 Part Number

ULCXX / XXXXXXXXXXXX

Mask-Programmed Universal Logic Circuit	Complete Part Number of Field-Programmable Device, including speed and temperature range (optional)

For an example, see figure 7-1 below.

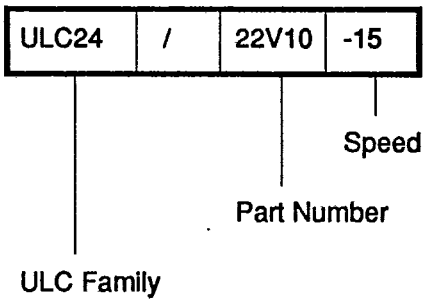

Figure 7-1: Example part number for replacement of a 15ns 22V10

7.3 How to Order

To submit a code and place an order, contact your local MDS representative or MDS headquarters at 800-338-GATE.

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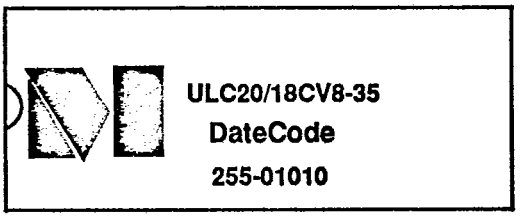
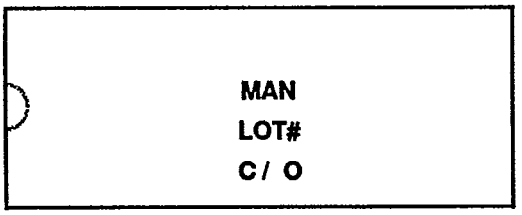
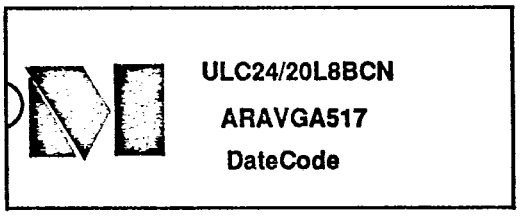
8. MARKING INFORMATION

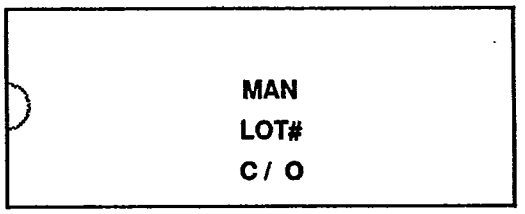
8.1 20/24 Pin PDIP



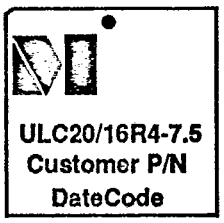


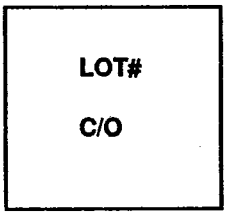
8.2 24 Pin Skinny Dip





8.3 20 Pin PLCC





8.4 28 Pin PLCC