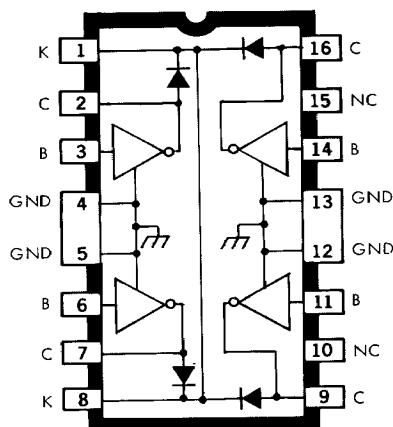


IECQ MFG.
APPROVALDESCLINE
CERTIFICATION

1.5 A DARLINGTON SWITCHES

ULN2064B



DWG. NO. A-9765A

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature for Any One Driver (unless other noted)

Output Voltage, V_{CEX} See Guide
Output SustainingVoltage, $V_{CE(SUS)}$ See GuideOutput Current, I_{OUT} (Note 1) 1.75 AInput Voltage, V_{IN} (Note 2) See GuideInput Current, I_B (Note 3) 25 mASupply Voltage, V_S (ULN2068/69B/LB) . 10 V

Total Package Power

Dissipation See Graph

Operating Temperature

Range, T_A -20°C to +85°C

Storage Temperature

Range, T_S -55°C to -150°C

1. Allowable combinations of output current, number of outputs conducting, and duty cycle are shown on following pages.
2. Input voltage is referenced to the substrate (no connection to other pins) for the ULN2061/62L/M and ULN2074/75B/LB, reference is ground for all other types.
3. Input current may be limited by maximum allowable input voltage.

High-voltage, high-current Darlington arrays ULN2061L/M through ULN2075B/LB are designed for interface between low-level logic and a variety of peripheral loads such as relays, solenoids, dc and stepper motors, multiplexed LED and incandescent displays, heaters, and similar loads. Output OFF voltage ratings of 50 V and 80 V are available. In the DIP, the quad drivers can drive resistive loads to 480 watts (1.5 A x 80 V, 26% duty cycle). For inductive loads, sustaining voltages of 35 V and 50 V at 100 mA are specified.

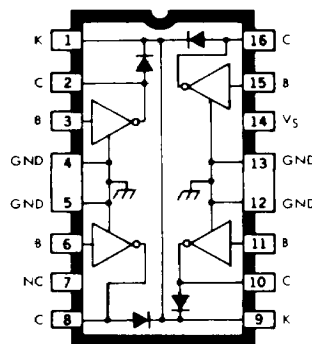
Dual-driver arrays ULN2061L/M and the higher-voltage ULN2062L/M are used for common-emitter (externally connected) or emitter-follower applications. They are supplied in 8-pin plastic mini-DIPs (suffix M) and surface-mountable SOICs (suffix L).

Quad drivers ULN2064B/LB, ULN2065B/LB, ULN2068B/LB, and ULN2069B/LB are intended for use with TTL, low-speed TTL, and 5 V MOS logic. The ULN2065B/LB and ULN2069B/LB are selected for the 80 V minimum output breakdown specification. The ULN2068B/LB and ULN2069B/LB have pre-driver stages and are recommended for applications requiring high gain (low input-current loading). Isolated Darlington arrays ULN2074B/LB and ULN2075B/LB are identical to the ULN2064B/LB and ULN2065NB/LB except for the isolated Darlington pinout and the deletion of suppression diodes. These switches are for emitter-follower applications. Quad-driver arrays are supplied with heat-sink contact tabs in 16-pin plastic DIPs (suffix B) and 20-lead surface-mountable wide-body SOICs (suffix LB).

FEATURES

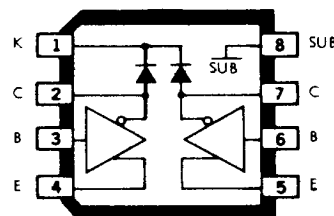
- TTL, DTL, MOS, CMOS Compatible Inputs
- Transient-Protected Outputs
- Loads to 480 Watts
- Heat-Sink Contact Tabs on Quad Arrays

ULN2068/69B



Dwg. No. A-10,310

ULN2061/62L



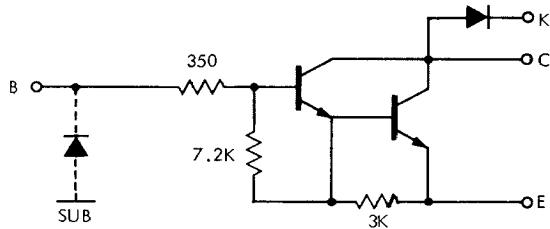
SPRAGUE

SEMICONDUCTOR GROUP

SERIES ULN2061L/M THROUGH ULN2075B/LB

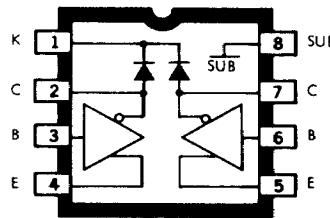
1.5 A DARLINGTON SWITCHES

PARTIAL SCHEMATIC



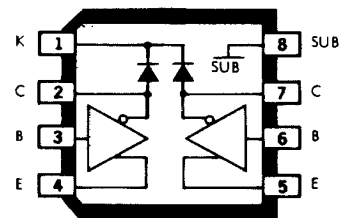
Dwg. No. A-10,352B

ULN2061/62M



Dwg. No. A-10,230A

ULN2061/62L



ELECTRICAL CHARACTERISTICS AT +25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices*	Test Conditions	Limits		
					Min.	Max.	Units
Output Leakage Current	I_{CEX}	1	ULN2061	$V_{CE} = 50 \text{ V}$	—	100	μA
				$V_{CE} = 50 \text{ V}, T_A = 70^\circ\text{C}$	—	500	μA
			ULN2062	$V_{CE} = 80 \text{ V}$	—	100	μA
				$V_{CE} = 80 \text{ V}, T_A = 70^\circ\text{C}$	—	500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	ULN2061	$I_C = 100 \text{ mA}, V_{IN} = 0.4 \text{ V}$	35	—	V
			ULN2062	$I_C = 100 \text{ mA}, V_{IN} = 0.4 \text{ V}$	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	Both	$I_C = 500 \text{ mA}, I_B = 625 \mu\text{A}$	—	1.1	V
				$I_C = 750 \text{ mA}, I_B = 935 \mu\text{A}$	—	1.2	V
				$I_C = 1.0 \text{ A}, I_B = 1.25 \mu\text{A}$	—	1.3	V
				$I_C = 1.25 \text{ A}^{**}, I_B = 2.0 \text{ mA}$	—	1.4	V
			ULN2062	$I_C = 1.5 \text{ A}^{**}, I_B = 2.25 \text{ mA}$	—	1.5	V
Input Current	$I_{IN(ON)}$	4	Both	$V_{IN} = 2.4 \text{ V}$	1.4	4.3	mA
				$V_{IN} = 3.75 \text{ V}$	3.3	9.6	mA
Input Voltage	$V_{IN(ON)}$	5	Both	$V_{CE} = 2.0 \text{ V}, I_C = 1.0 \text{ A}$	—	2.0	V
			ULN2061	$V_{CE} = 2.0 \text{ V}, I_C = 1.25 \text{ A}^{**}$	—	2.5	V
			ULN2062	$V_{CE} = 2.0 \text{ V}, I_C = 1.5 \text{ A}^{**}$	—	2.5	V
Turn-On Delay	t_{PLH}	—	Both	$0.5 E_{in} \text{ to } 0.5 E_{out}$	—	1.0	μs
Turn-Off Delay	t_{PHL}	—	Both	$0.5 E_{in} \text{ to } 0.5 E_{out}$	—	1.5	μs
Clamp Diode Leakage Current	I_R	6	ULN2061	$V_R = 50 \text{ V}$	—	50	μA
				$V_R = 50 \text{ V}, T_A = 70^\circ\text{C}$	—	100	μA
			ULN2062	$V_R = 80 \text{ V}$	—	50	μA
				$V_R = 80 \text{ V}, T_A = 70^\circ\text{C}$	—	100	μA
Clamp Diode Forward Voltage	V_F	7	Both	$I_F = 1.0 \text{ A}$	—	1.75	V
				$I_F = 1.5 \text{ A}$	—	2.0	V

** Pulse-Test

* Complete part number includes suffix to identify package style: L — SOIC, M — 8-pin mini-DIP.

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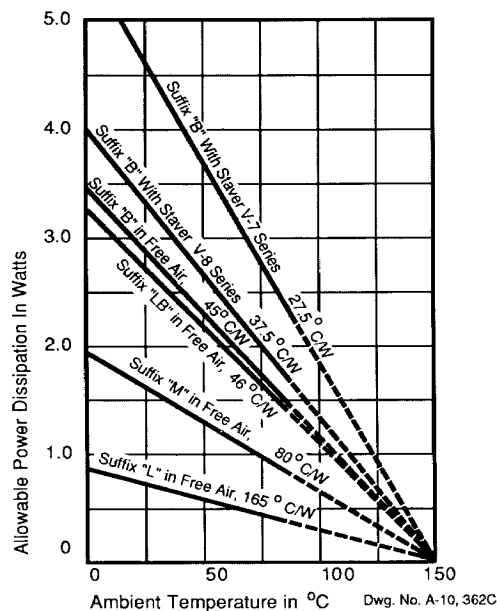
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Worcester, Massachusetts 01615-0036 (508) 853-5000
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SERIES ULN2061L/M THROUGH ULN2075B/LB 1.5 A DARLINGTON SWITCHES

SELECTION GUIDE

Part Number*	Max. V_{CEX}	Min. $V_{CE(SUS)}$	Max. V_{IN}	Application
ULN2061L/M ULN2062L/M	50 V 80 V	35 V 50 V	30 V 60 V	TTL, DTL, Schottky TTL, and 5 V CMOS
ULN2064B/LB ULN2065B/LB	50 V 80 V	35 V 50 V	15 V 15 V	TTL, DTL, Schottky TTL, and 5 V CMOS
ULN2068B/LB ULN2069B/LB	50 V 80 V	35 V 50 V	15 V 15 V	TTL, DTL, Schottky TTL, and 5 V CMOS
ULN2074B/LB ULN2075B/LB	50 V 80 V	35 V 50 V	30 V 60 V	General Purpose

*Suffixes 'L' and 'LB' are SOICs, 'B' and 'M' are DIPs.



TEST FIGURES

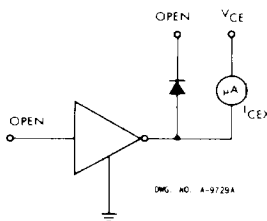


FIGURE 1

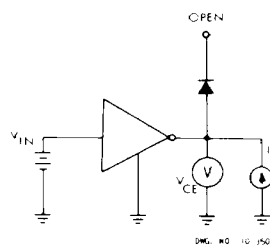


FIGURE 2

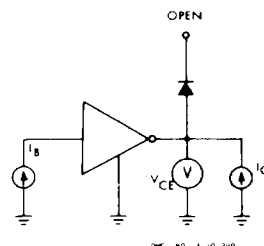


FIGURE 3

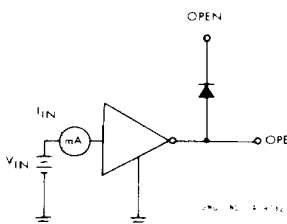


FIGURE 4

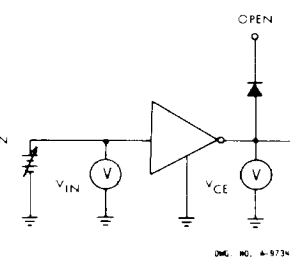


FIGURE 5

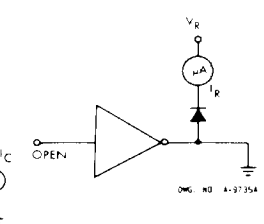


FIGURE 6

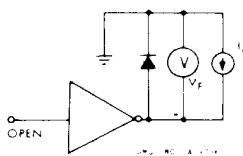


FIGURE 7

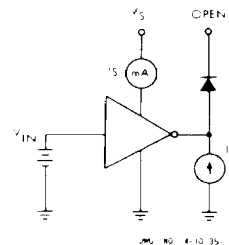
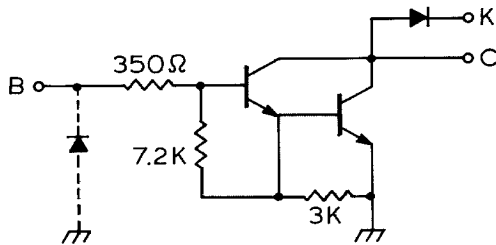


FIGURE 8

SEMICONDUCTOR GROUP

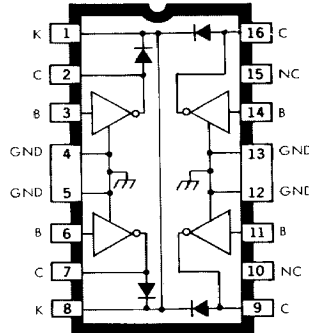
SERIES ULN2061L/M THROUGH ULN2075B/LB 1.5 A DARLINGTON SWITCHES

PARTIAL SCHEMATIC



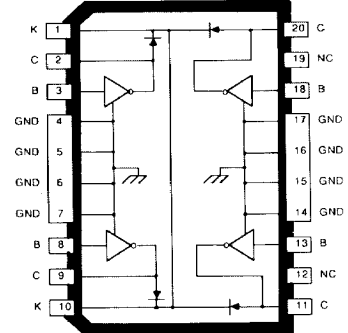
Dwg. No. A 10,353C

ULN 2064/65B



DWG. NO. A-9765A

ULN 2064/65LB



ELECTRICAL CHARACTERISTICS AT $\pm 25^{\circ}\text{C}$ (unless otherwise noted)

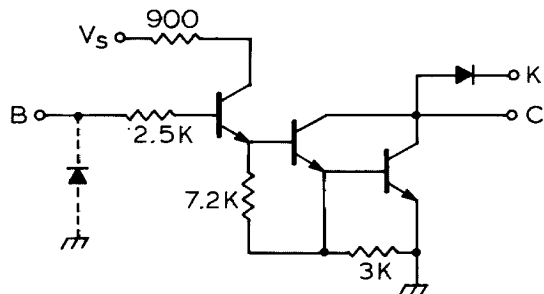
Characteristic	Symbol	Test Fig.	Applicable Devices*	Test Conditions	Limits		
					Min.	Max.	Units
Output Leakage Current	I_{CEX}	1	ULN2064	$V_{CE} = 50\text{ V}$	—	100	μA
				$V_{CE} = 50\text{ V}, T_A = 70^{\circ}\text{C}$	—	500	μA
			ULN2065	$V_{CE} = 80\text{ V}$	—	100	μA
				$V_{CE} = 80\text{ V}, T_A = 70^{\circ}\text{C}$	—	500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	ULN2064	$I_C = 100\text{ mA}, V_{IN} = 0.4\text{ V}$	35	—	V
			ULN2065	$I_C = 100\text{ mA}, V_{IN} = 0.4\text{ V}$	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	Both	$I_C = 500\text{ mA}, I_B = 625\text{ }\mu\text{A}$	—	1.1	V
				$I_C = 750\text{ mA}, I_B = 935\text{ }\mu\text{A}$	—	1.2	V
				$I_C = 1.0\text{ A}, I_B = 1.25\text{ }\mu\text{A}$	—	1.3	V
				$I_C = 1.25\text{ A}, I_B = 2.0\text{ mA}$	—	1.4	V
			ULN2065	$I_C = 1.5\text{ A}, I_B = 2.25\text{ mA}$	—	1.5	V
Input Current	$I_{IN(ON)}$	4	Both	$V_{IN} = 2.4\text{ V}$	1.4	4.3	mA
				$V_{IN} = 3.75\text{ V}$	3.3	9.6	mA
Input Voltage	$V_{IN(ON)}$	5	Both	$V_{CE} = 2.0\text{ V}, I_C = 1.0\text{ A}$	—	2.0	V
			ULN2064	$V_{CE} = 2.0\text{ V}, I_C = 1.25\text{ A}$	—	2.5	V
			ULN2065	$V_{CE} = 2.0\text{ V}, I_C = 1.5\text{ A}$	—	2.5	V
Turn-On Delay	t_{PLH}	—	Both	$0.5 E_{in}$ to $0.5 E_{out}$	—	1.0	μs
Turn-Off Delay	t_{PHL}	—	Both	$0.5 E_{in}$ to $0.5 E_{out}$	—	1.5	μs
Clamp Diode Leakage Current	I_R	6	ULN2064	$V_R = 50\text{ V}$	—	50	μA
				$V_R = 50\text{ V}, T_A = 70^{\circ}\text{C}$	—	100	μA
			ULN2065	$V_R = 80\text{ V}$	—	50	μA
				$V_R = 80\text{ V}, T_A = 70^{\circ}\text{C}$	—	100	μA
Clamp Diode Forward Voltage	V_F	7	Both	$I_F = 1.0\text{ A}$	—	1.75	V
				$I_F = 1.5\text{ A}$	—	2.0	V

*Complete part number includes suffix to identify package style: B = DIP with heat sink tabs, LB = SOIC with heat sink tabs.

SPRAGUE

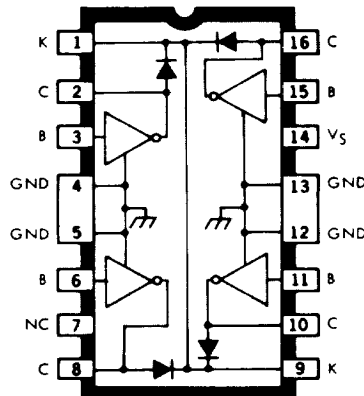
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

PARTIAL SCHEMATIC



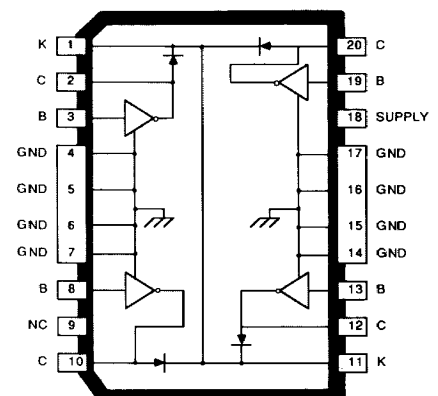
Dwg. No. A-10,354C

ULN2068/69B



Dwg. No. A-10,310

ULN2068 69LB



ELECTRICAL CHARACTERISTICS AT +25°C, $V_S = 50V$ (unless otherwise noted)

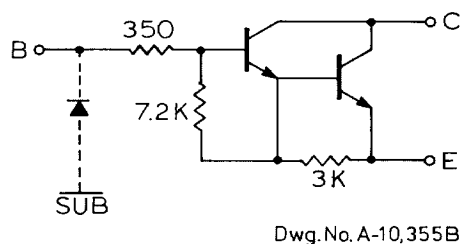
Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits		
					Min.	Max.	Units
Output Leakage Current	I_{CEX}	1	ULN2068	$V_{CE} = 50V$	—	100	μA
				$V_{CE} = 50V, T_A = 70^\circ C$	—	500	μA
			ULN2069	$V_{CE} = 80V$	—	100	μA
				$V_{CE} = 80V, T_A = 70^\circ C$	—	500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	ULN2068	$I_C = 100mA, V_{IN} = 0.4V$	35	—	V
			ULN2069	$I_C = 100mA, V_{IN} = 0.4V$	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	Both	$I_C = 500mA, I_{IN} = 2.75V$	—	1.1	V
				$I_C = 750mA, I_{IN} = 2.75V$	—	1.2	V
				$I_C = 1.0A, I_{IN} = 2.75V$	—	1.3	V
				$I_C = 1.25A, I_{IN} = 2.75V$	—	1.4	V
			ULN2069	$I_C = 1.5A, I_{IN} = 2.75V$	—	1.5	V
Input Current	$I_{IN(ON)}$	4	Both	$V_{IN} = 2.75V$	—	550	μA
				$V_{IN} = 3.75V$	—	1000	μA
Input Voltage	$V_{IN(ON)}$	5	ULN2068	$V_{CE} = 2.0V, I_C = 1.25A$	—	2.75	V
			ULN2069	$V_{CE} = 2.0V, I_C = 1.5A$	—	2.75	V
Supply Current	I_S	8	Both	$I_C = 500mA, V_{IN} = 2.75V$	—	6.0	mA
Turn-On Delay	t_{PLH}	—	Both	$0.5E_{in}$ to $0.5E_{out}$	—	1.0	μs
Turn-Off Delay	t_{PHL}	—	Both	$0.5E_{in}$ to $0.5E_{out}, I_C = 1.25A$	—	1.5	μs
Clamp Diode Leakage Current	I_R	6	ULN2068	$V_R = 50V$	—	50	μA
				$V_R = 50V, T_A = 70^\circ C$	—	100	μA
			ULN2069	$V_R = 80V$	—	50	μA
				$V_R = 80V, T_A = 70^\circ C$	—	100	μA
Clamp Diode Forward Voltage	V_F	7	Both	$I_F = 1.0A$	—	1.75	V
				$I_F = 1.5A$	—	2.0	V

*Complete part number includes suffix to identify package style: B = DIP with heat sink tabs, LB = SOIC with heat sink tabs.

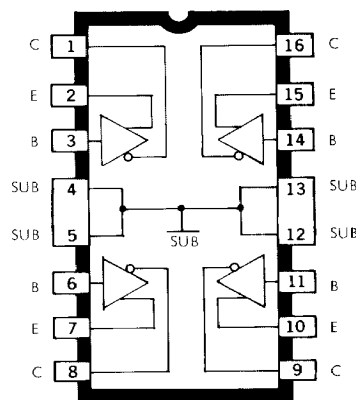
SEMICONDUCTOR GROUP

SERIES ULN2061L/M THROUGH ULN2075B/LB 1.5 A DARLINGTON SWITCHES

PARTIAL SCHEMATIC

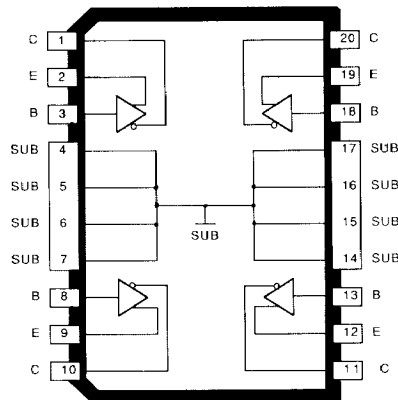


ULN2074/75B



DWG. NO. A-9766A

ULN2074/75LB



ELECTRICAL CHARACTERISTICS AT +25°C (unless otherwise noted)

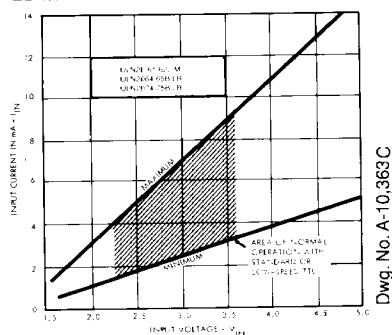
Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits		
					Min.	Max.	Units
Output Leakage Current	I_{CEX}	1	ULN2074	$V_{CE} = 50 \text{ V}$	—	100	μA
				$V_{CE} = 50 \text{ V}, T_A = 70^\circ\text{C}$	—	500	μA
			ULN2075	$V_{CE} = 80 \text{ V}$	—	100	μA
				$V_{CE} = 80 \text{ V}, T_A = 70^\circ\text{C}$	—	500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	ULN2074	$I_C = 100 \text{ mA}, V_{IN} = 0.4 \text{ V}$	35	—	V
			ULN2075	$I_C = 100 \text{ mA}, V_{IN} = 0.4 \text{ V}$	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	Both	$I_C = 500 \text{ mA}, I_B = 625 \mu\text{A}$	—	1.1	V
				$I_C = 750 \text{ mA}, I_B = 935 \mu\text{A}$	—	1.2	V
				$I_C = 1.0 \text{ A}, I_B = 1.25 \text{ mA}$	—	1.3	V
				$I_C = 1.25 \text{ A}, I_B = 2.0 \text{ mA}$	—	1.4	V
			ULN2075	$I_C = 1.5 \text{ A}, I_B = 2.25 \text{ mA}$	—	1.5	V
Input Current	$I_{IN(ON)}$	4	Both	$V_{IN} = 2.4 \text{ V}$	1.4	4.3	mA
				$V_{IN} = 3.75 \text{ V}$	3.3	9.6	mA
Input Voltage	$V_{IN(ON)}$	5	Both	$V_{CE} = 2.0 \text{ V}, I_C = 1.0 \text{ A}$	—	2.0	V
			ULN2074	$V_{CE} = 2.0 \text{ V}, I_C = 1.25 \text{ A}$	—	2.5	V
			ULN2075	$V_{CE} = 2.0 \text{ V}, I_C = 1.5 \text{ A}$	—	2.5	V
Turn-On Delay	t_{PLH}	—	Both	$0.5 E_{in}$ to $0.5 E_{out}$	—	1.0	μs
Turn-Off Delay	t_{PHL}	—	Both	$0.5 E_{in}$ to $0.5 E_{out}$	—	1.5	μs

*Complete part number includes suffix to identify package style: B DIP with heat sink tabs, LB SOIC with heat sink tabs.

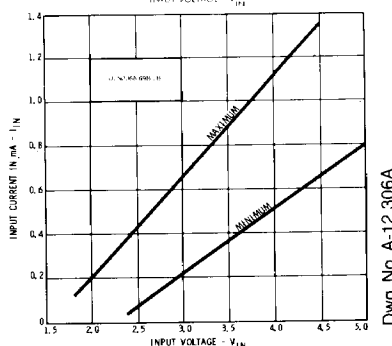
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Worcester, Massachusetts 01615-0036 (508) 853-5000

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE AT +25°C

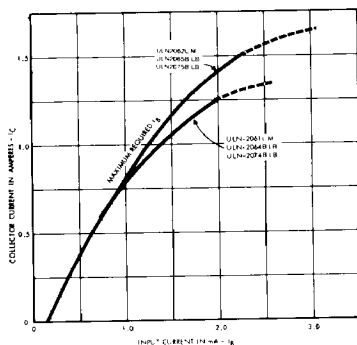


Dwg. No. A-10,363C

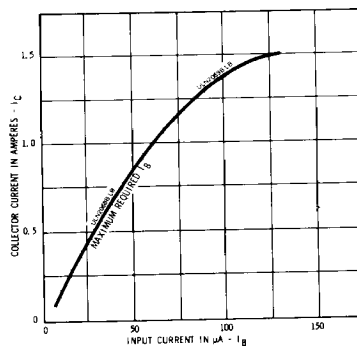


Dwg. No. A-12,306A

COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT AT +25°C

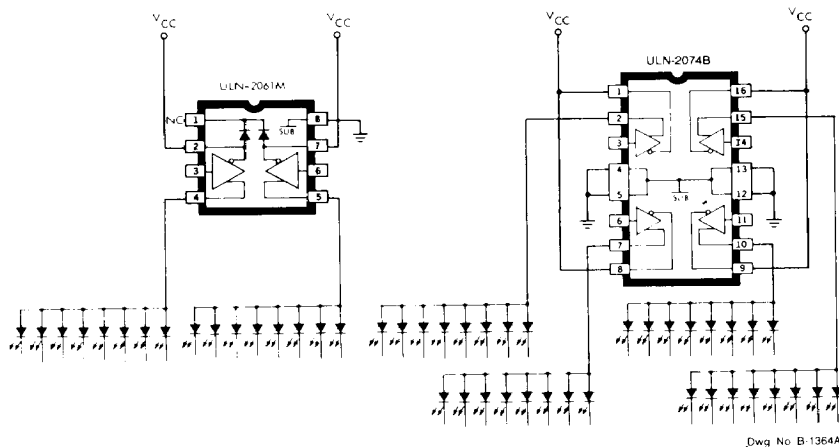


Dwg. No. A-10,358C



Dwg. No. A-12,306A

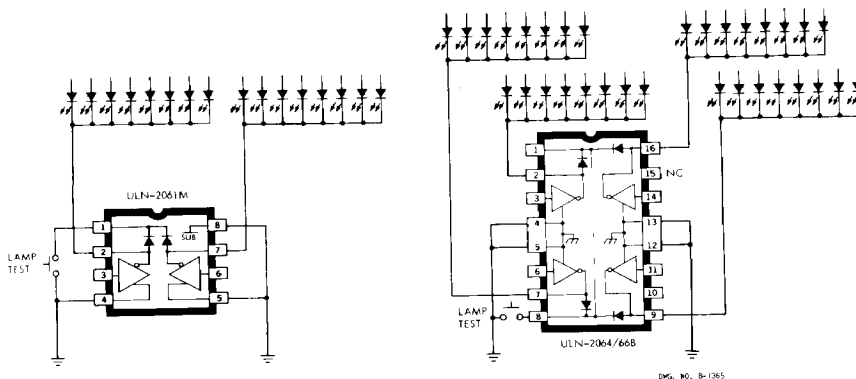
TYPICAL APPLICATIONS



Dwg. No. B-1364A

COMMON-ANODE LED DRIVERS

(Series UD2980A/EP/LW devices can be used in similar applications at currents of up to 500 mA)

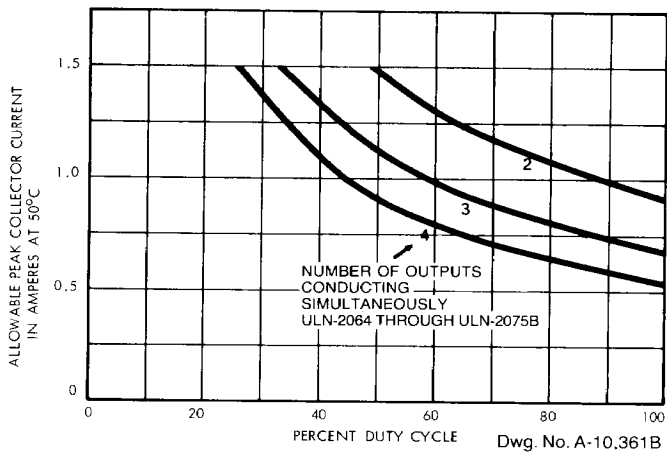
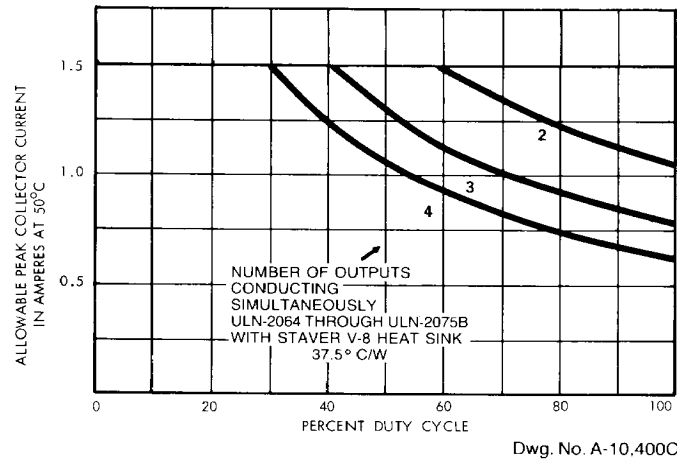
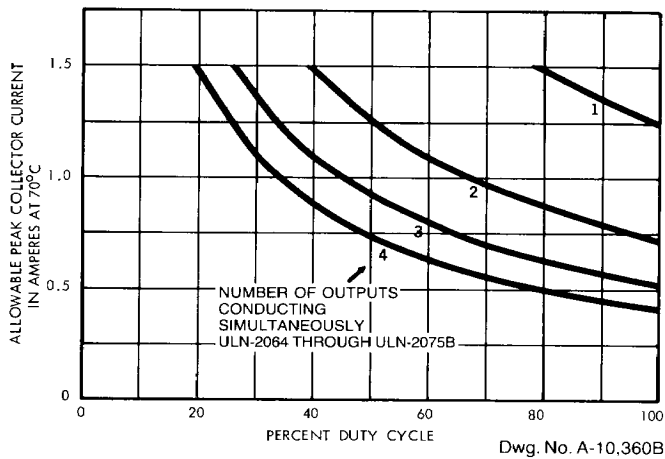
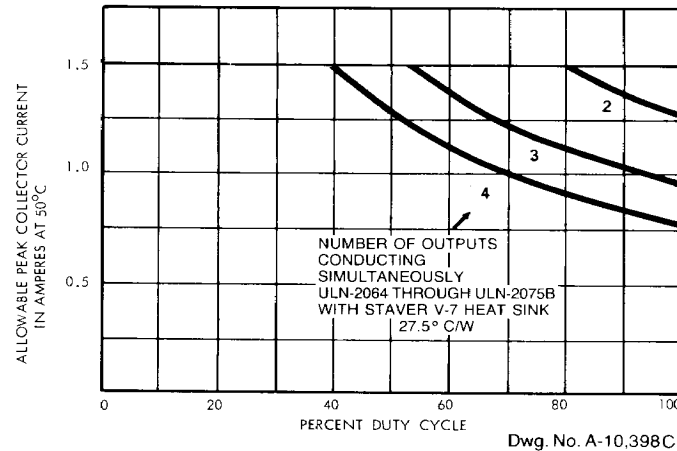
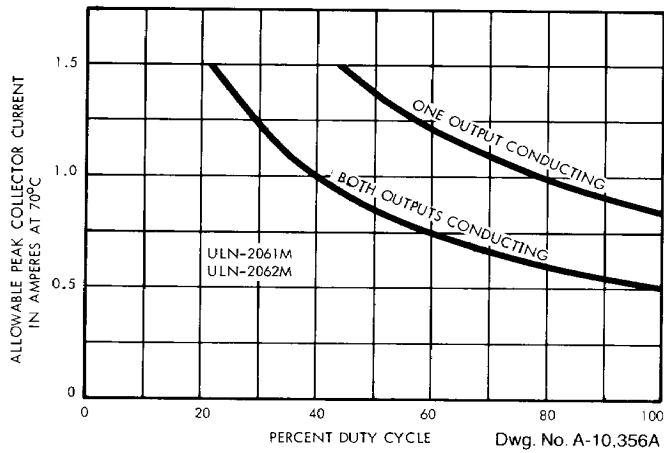


Dwg. No. B-1365

COMMON-CATHODE LED DRIVERS

(Type ULN2068B/LB is also applicable)

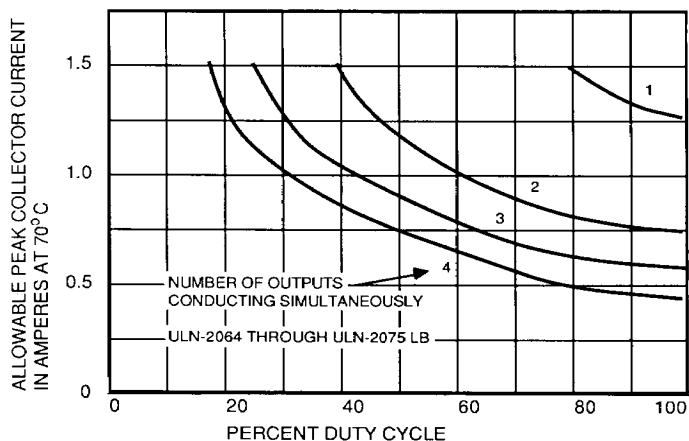
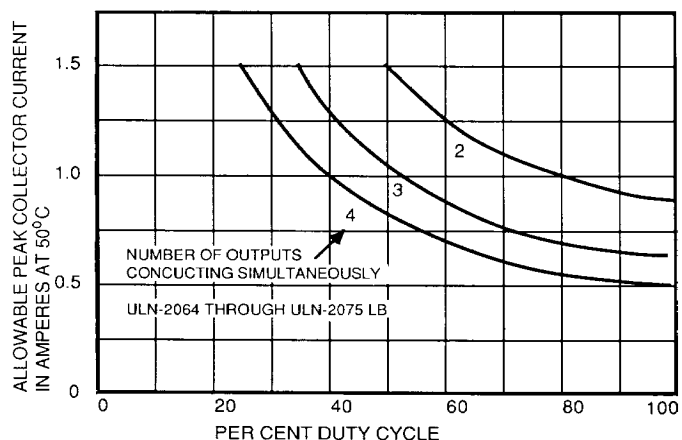
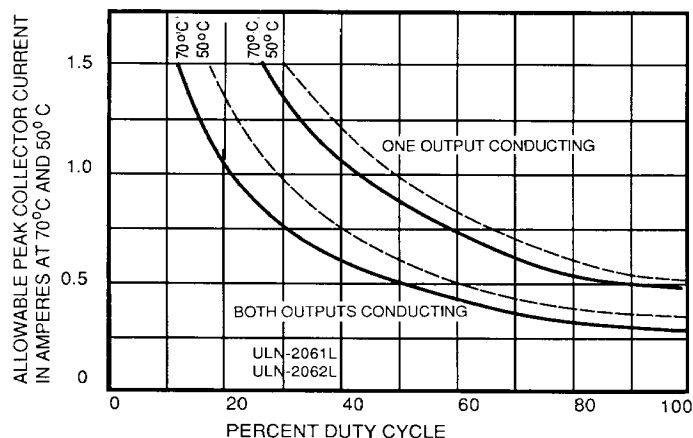
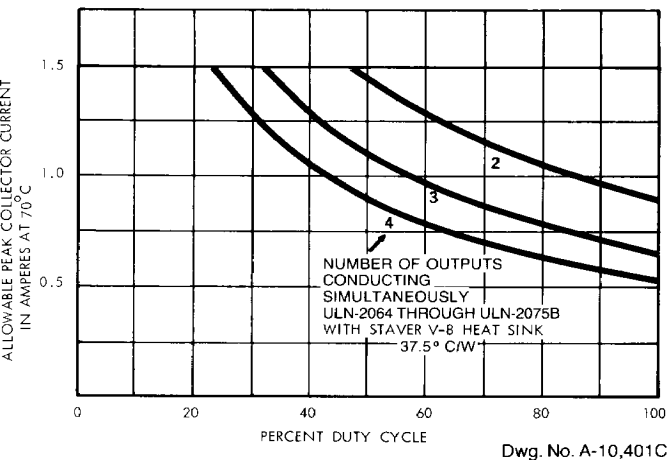
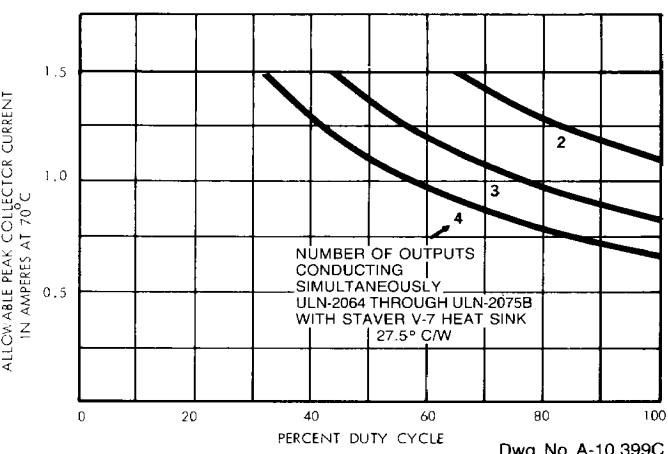
PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE (Dual In-Line Packaged Devices)



SEMICONDUCTOR GROUP

SERIES ULN2061L/M THROUGH ULN2075B/LB 1.5 A DARLINGTON SWITCHES

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE (Small Outline Packaged Devices)



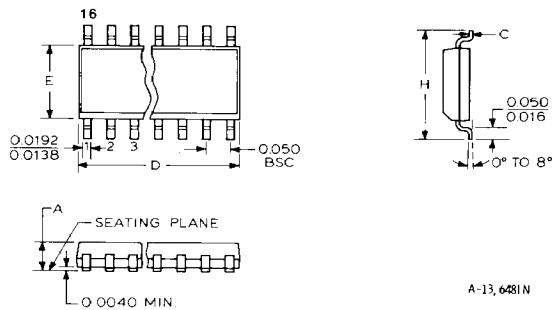
SEMICONDUCTOR GROUP

SERIES ULN2061L/M THROUGH ULN2075B/LB

1.5 A DARLINGTON SWITCHES

PLASTIC SOIC

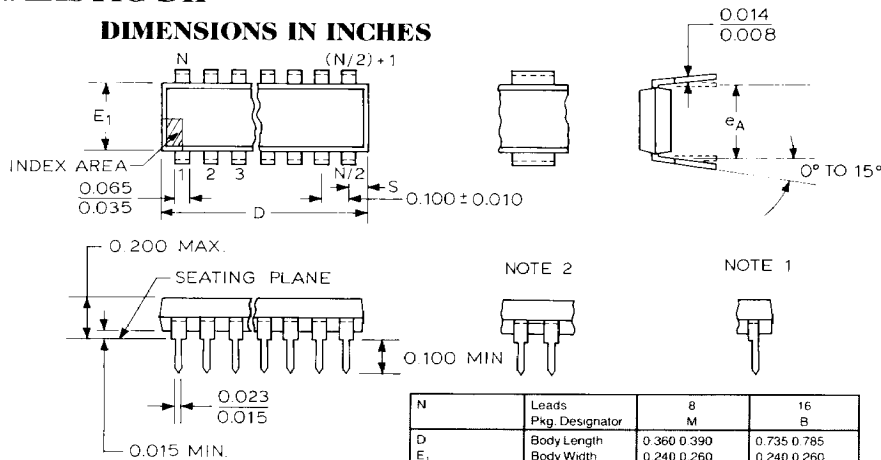
DIMENSIONS IN INCHES (BASED ON 1 mm = 0.03937")



N	Leads Pkg. Designator	8 L	20 LB
A	Seated Height	0.0532 0.0688	0.0926 0.1043
C	Lead Thickness	0.0075 0.0098	0.0091 0.0125
D	Body Length	0.1890 0.1968	0.4961 0.5118
E	Body Width	0.1497 0.1574	0.2914 0.2992
H	Overall Width	0.2284 0.2440	0.394 0.419
Notes	(Leads Affected)	2 (4.7-14-17)	

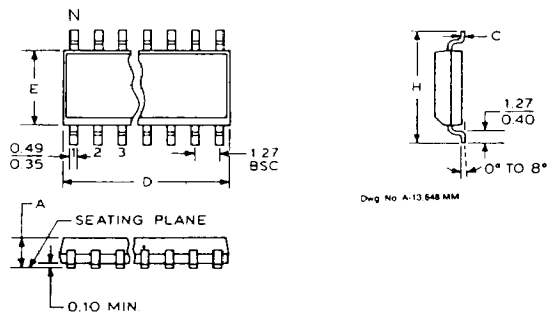
PLASTIC DIP

DIMENSIONS IN INCHES



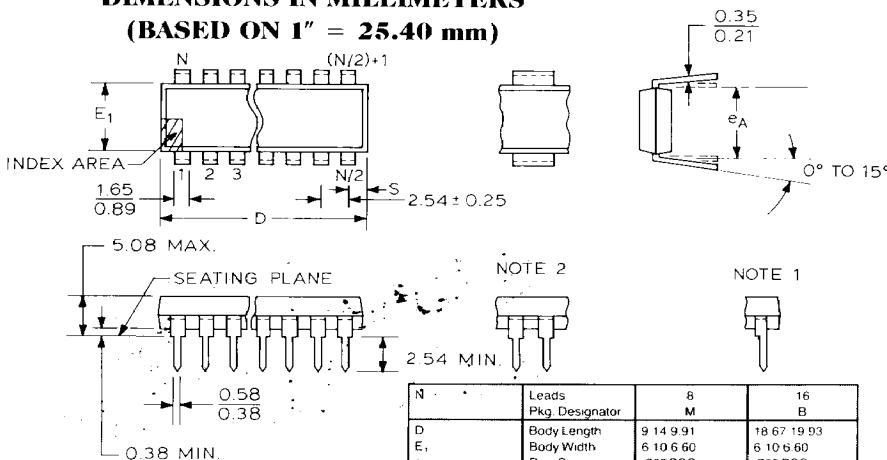
N	Leads Pkg. Designator	8 M	16 B
D	Body Length	0.360 0.390	0.735 0.785
E1	Body Width	0.240 0.260	0.240 0.260
eA	Row Spacing	0.300 BSC	0.300 BSC
S	Lead CL to End	0.040 REF	0.025 REF
Notes	(Leads Affected)	1 (1.4.5.8)	1 (1.8.9.16) 2 (4.5.12.13)

DIMENSIONS IN MILLIMETERS



N	Leads Pkg. Designator	8 L	20 LB
A	Seated Height	1.35 1.75	2.35 2.65
C	Lead Thickness	0.19 0.25	0.23 0.32
D	Body Length	4.80 5.00	12.60 13.00
E	Body Width	3.80 4.00	7.40 7.60
H	Overall Width	5.80 6.20	10.0 10.65
Notes	(Leads Affected)	2 (4.7-14-17)	

DIMENSIONS IN MILLIMETERS (BASED ON 1" = 25.40 mm)



N	Leads Pkg. Designator	8 M	16 B
D	Body Length	9.14 9.91	18.67 19.93
E1	Body Width	6.10 6.60	6.10 6.60
eA	Row Spacing	7.62 BSC	7.62 BSC
S	Lead CL to End	1.02 REF	0.64 REF
Notes	(Leads Affected)	1 (1.4.5.8)	1 (1.8.9.16) 2 (4.5.12.13)

1. Leads 1, N/2, (N/2) + 1, and N may be half-leads at vendor's option.
2. Webbed lead frame. Leads indicated are internally one piece.

In the construction of the components described, the full intent of the specification will be met. The Sprague Electric Company, however, reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the design of its products. Components made under military approvals will be in accordance with the approval requirements.

The information included herein is believed to be accurate and reliable. However, the Sprague Electric Company assumes no responsibility for its use; nor for any infringements of patents or other rights of third parties which may result from its use.

- A. Dimensions shown as ____/____ are Min./Max.
- B. Lead thickness is measured at seating plane or below.
- C. Lead spacing tolerance is non-cumulative.
- D. Exact body and lead configuration at vendor's option within limits shown.
- E. Leads missing from their designated positions shall also be counted when numbering leads.
- F. Lead gauge plane is 0.030" (7.62 mm) max. below seating plane.

SPRAGUE

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