PRELIMINARY ISSUE
(Specifications Subject to Change Without Notice) October 26, 1988

Integrated Circuits

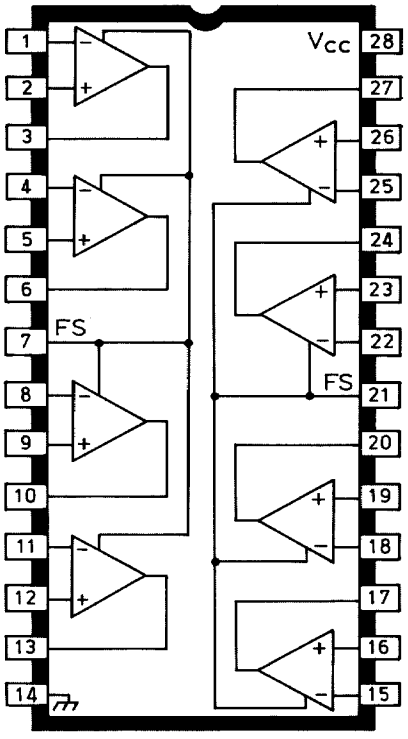
ULN8510A/EP/R
ULN8511A/EP/R

Data Sheet 27445

IECQ MFG. APPROVAL

OCTAL LOW-SPEED EIA RECEIVERS

ULN8510A/R
ULN8511A/R



Dwg. PS-005

Each containing eight differential line receivers, the ULN8510A/EP/R and ULN8511A/EP/R are designed for cost-effective data communications meeting the requirements of RS-232C, RS-423A and CCITT recommendations V.10, V.11, and V.28 for low-speed applications without external components. The receivers include failsafing for protection against certain input fault conditions, Schottky TTL output stages, and output current limiting. The ULN8510A/EP/R includes internal low-pass filtering for data transmission rates up to 200 kb/s and meets the low-speed applications of RS-422A. The ULN8511A/EP/R is for use with increased data rates up to 10 Mb/s. Except for the internal low-pass filtering, the ULN8510x and ULN8511x are pin-compatible and completely interchangeable.

The ULN8510A and ULN8511A are supplied in 28-pin dual in-line plastic packages with copper lead frames for improved power dissipation capabilities; devices with package suffix code 'R' are supplied in 28-pin dual in-line cer-DIP hermetic packages for operation under adverse environmental conditions; suffix code 'EP' indicates a 28-lead PLCC for minimum-area, surface-mount applications.

FEATURES

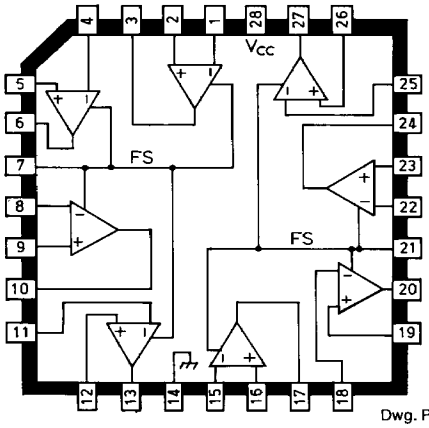
- Dual, Four-Channel, Failsafing Control
- Schottky TTL Output Stages
- Output Current Limiting
- Meets EIA RS-232C, RS-422A, and RS-423A
- Replaces NE5180/81 & UC5180/81

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... **7.0 V**
Input Common Mode Range,
V_{IC} ..... **±15 V**
Differential Input Voltage, V_{ID} ..... **±25 V**
Output Current, I_{OUT} ..... **50 mA**
Package Power Dissipation,
P_D ..... **1.2 W**
Operating Temperature Range,
T_A ..... **0°C to +70°C**
Storage Temperature Range,
T_S ..... **−55°C to +125°C**

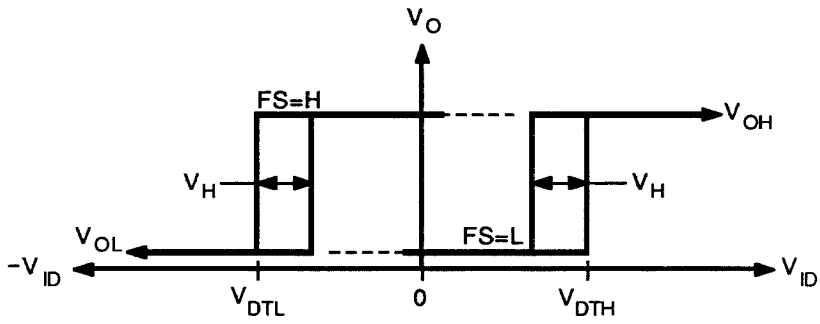
ULN8510A/EP/R AND ULN8511A/EP/R
OCTAL LOW-SPEED EIA RECEIVERS

ULN8510/11EP



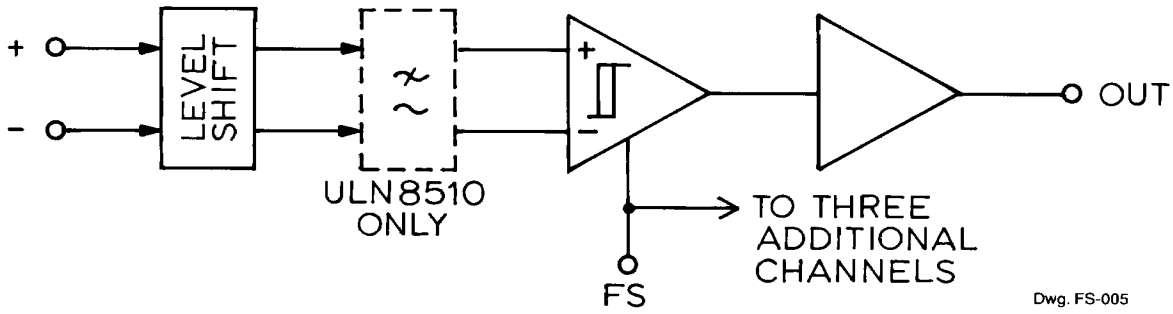
Dwg. PS-006

DEFINITIONS



Dwg. GS-007

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM
(ONE OF EIGHT CHANNELS SHOWN)



Dwg. FS-005

TRUTH TABLE

Input	Failsafe Input	Output
$V_{ID} \geq 0.2$ V	X	H
$V_{ID} \geq -0.2$ V	X	L
$V_{ID} = 0$	L	L
$V_{ID} = 0$	H	H

X = Don't Care.

SPRAGUE

115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

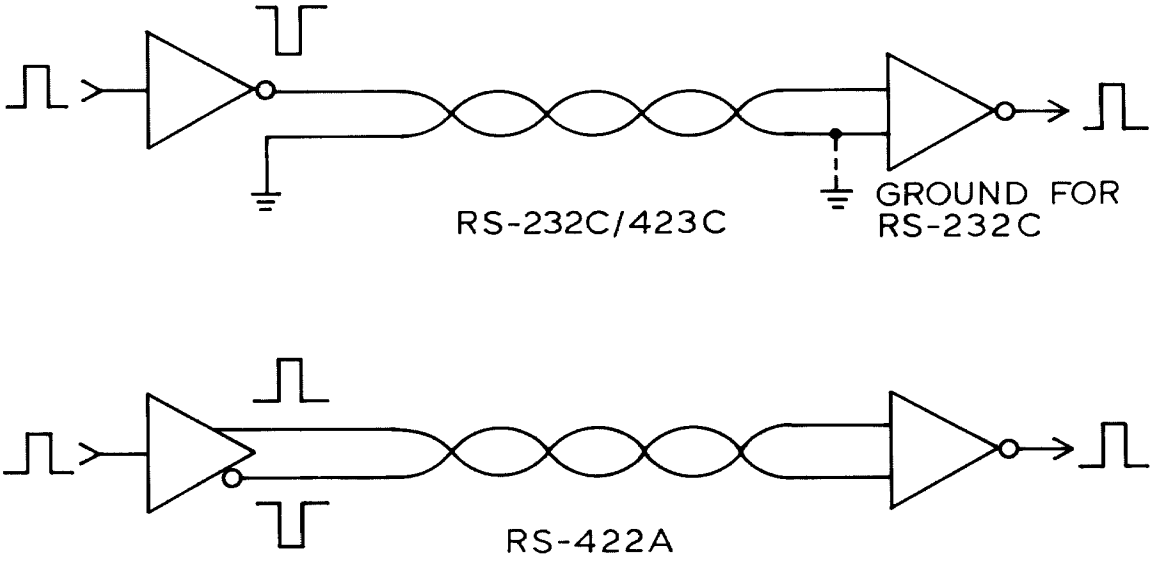
APPLICATIONS INFORMATION

Failsafing. These devices provide a failsafe operating mode to guard against input faults as defined in RS-422A and RS-423A. The receivers are programmed by connecting the appropriate failsafe input to V_{CC} or ground. A failsafe connection to V_{CC} provides a logic '1' output under fault conditions (both inputs to ground, to V_{CC}, opened, or shorted together), a failsafe connection to ground provides a logic '0' under fault conditions. Under normal operating conditions (1 V_{pp}), if either input is faulted (to ground, to V_{CC}, or opened), but not both, the system will continue to function but with reduced noise immunity.

Limited failsafing for single-ended operation (RS-232 operation) is provided by tying the unused input to ground. A failsafe connection to V_{CC} provides a logic '**1**' output under fault conditions to ground, a failsafe connection to ground provides a logic '0' output under fault conditions to ground.

Input Filtering. The ULN8510A/EP/R has input low-pass filtering for improved noise rejection. The filtering is a function of both signal level and frequency. These devices are intended for low-speed data applications to 200 kb/s.

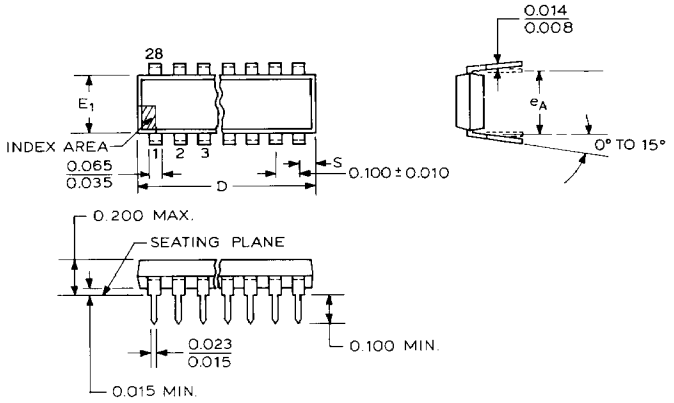
DATA COMMUNICATIONS



Dwg. OS-002

ULN8510A and ULN8511A — PLASTIC DUAL IN-LINE PACKAGE

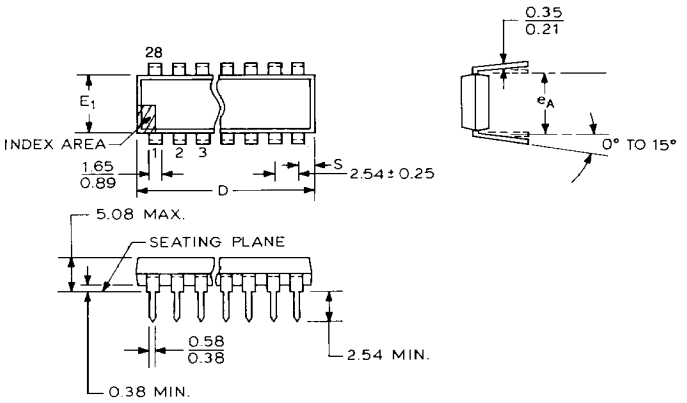
DIMENSIONS IN INCHES



Dwg. No. A-13.642 IN

D	Body Length	1.380/1.460
E_1	Body Width	0.480/0.560
e_A	Row Spacing	0.600 BSC
S	Lead CL to End	0.075 REF

DIMENSIONS IN MILLIMETERS (BASED ON 1″ = 25.40 mm)

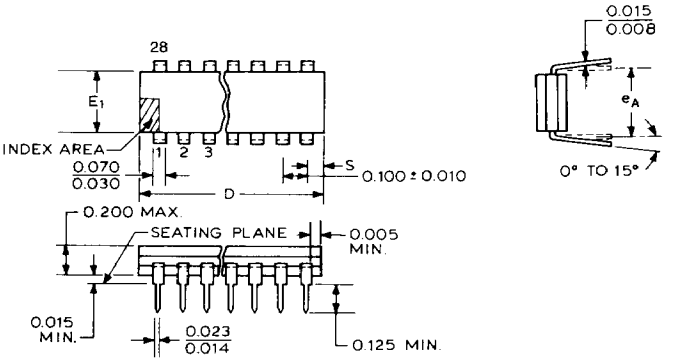


Dwg. No. A-13.642 MM

D	Body Length	35.05/37.08
E_1	Body Width	12.19/14.22
e_A	Row Spacing	15.24/BSC
S	Lead CL to End	1.90 REF

ULN8510R and ULN8511R — HERMETIC CerDIP PACKAGE

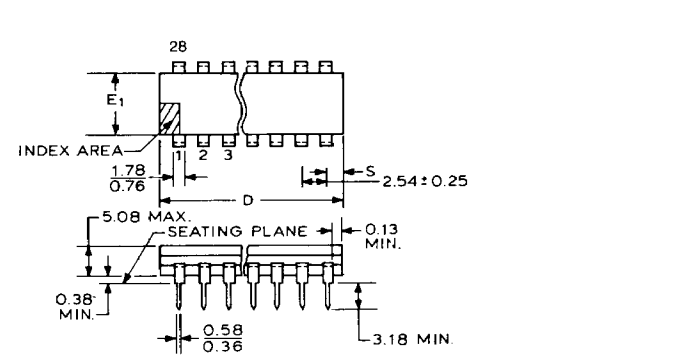
DIMENSIONS IN INCHES



Dwg. No. A-13.650 IN

D	Body Length	1.490 Max.
E_1	Body Width	0.500/0.610
e_A	Row Spacing	0.590/0.620
S	Lead CL to End	0.100 Max.
M38510H, Case Outline		D-10 Configuration 1

DIMENSIONS IN MILLIMETERS (BASED ON 1″ = 25.40 mm)



Dwg. No. A-13.650 MM

D	Body Length	37.85 Max.
E_1	Body Width	12.70/15.49
e_A	Row Spacing	14.99/15/75
S	Lead CL to End	2.54 Max.
M38510H, Case Outline		D-10 Configuration 1

A. Dimensions shown as ____ / ____ are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Lead gauge plane is 0.030″ (0.762 mm) max. below seating plane.

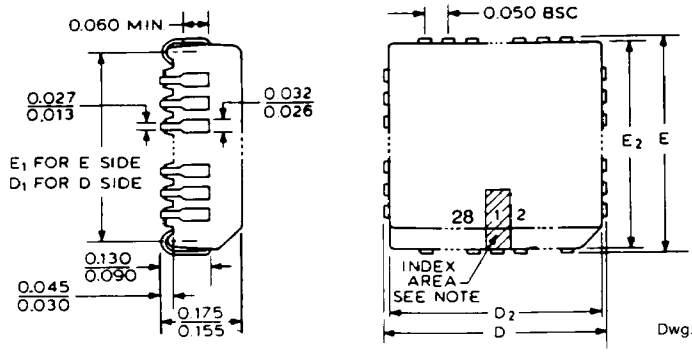
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 4.75 V to 5.25 V, V_{IC} = ±7.0 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Diff. Input Threshold Voltage	V_{DTH}	Output High	–	0.2	V
		Output High (Note 1)	–	0.4	V
	V_{DTL}	Output Low	–	−0.2	V
		Output Low (Note 1)	–	−0.4	V
Hysteresis	V_H		40	140	mV
Open-Circuit Input Voltage	V_{IOC}		–	0.5	V
Input Current	I_{IN}	V_{CC} = 5.25 V, V_{IN} = 10 V (Note 2)	–	3.25	mA
		V_{CC} = 5.25 V, V_{IN} = −10 V (Note 2)	–	−3.25	mA
Input Resistance	R_{IN}	V_{IN} = 0	4.0	7.0	kΩ
		3.0 V ≤ $\lvert V_{in} \rvert$ ≤ 25V	3.0	7.0	kΩ
Input Capacitance	C_{in}		–	100	pF
Failsafe Input Voltage	V_{IH}		4.0	–	V
	V_{IL}		–	0.5	V
Failsafe Input Current	I_{IH}	V_{IN} = 4.0 V	–	−100	µA
	I_{IL}	V_{IN} = 0.5 V	–	−500	µA
Output Voltage	V_{OH}	V_{ID} = 1.0 V, I_{OUT} = −440 µA	2.7	–	V
	V_{OL}	V_{ID} = 1.0 V, I_{OUT} = 4.0 mA	–	0.4	V
		V_{ID} = 1.0 V, I_{OUT} = 8.0 mA	–	0.5	V
Output Short-Circuit Current	I_{OS}	V_{ID} = 1.0 V (Note 3)	–	−100	mA
Propagation Delay	t_{PLH}	C_L = 50 pF, V_{in} = 1.0 V	–	500	ns
	t_{PHL}	C_L = 50 pF, V_{in} = 1.0 V	–	500	ns
Frequency Response		V_{in} = 400 mVpp, 100 kHz Square Wave	Note 4	–	–
		V_{in} = 1.0 Vpp, 5.0 MHz Square Wave	Note 5	–	–
		V_{in} = 1.0 Vpp, 5.5 MHz Square Wave	–	Note 6	–
		V_{in} = 2.0 Vpp, 12.5 MHz Square Wave	–	Note 7	–
Supply Current	I_{CC}	No Signal	–	135	mA

Notes: 1. 500 Ω resistor in series with both inputs.
2. Inputs not under test grounded.
3. Each output tested separately.
4. Presence of 100 kHz TTL output (All devices).
5. Presence of 5.0 MHz TTL output (ULN8511A/EP/R only).
6. No 5.5 MHz TTL output component present (ULN8510A/EP/R only).
7. No 12.5 MHz TTL output component present (ULN8510A/EP/R only).

ULN8510EP and ULN8511EP
PLASTIC LEADED CHIP CARRIER

DIMENSIONS IN INCHES

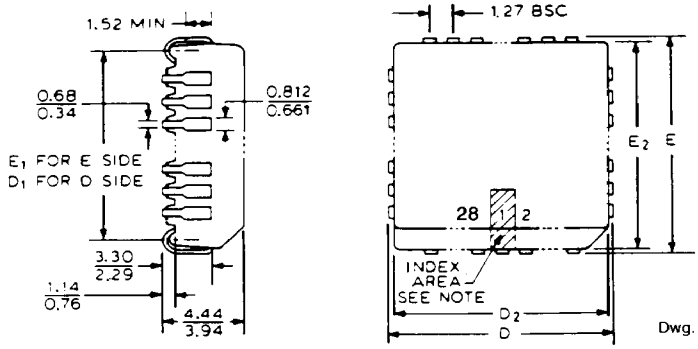


Dwg. No. A-13.644 IN

D	Overall Length	0.470/0.510
D_1	Row Spacing	0.390/0.430
D_2	Body Length	0.440/0.460
E	Overall Width	0.470/0.510
E_1	Row Spacing	0.390/0.430
E_2	Body Width	0.440/0.460
JEDEC Designation		MS-007AA

NOTE: Index is centered on "D" side.

DIMENSIONS IN MILLIMETERS
(BASED ON 1" = 25.40 mm)



Dwg. No. A-13.644 MM

D	Overall Length	11.94/12.95
D_1	Row Spacing	9.91/10.92
D_2	Body Length	11.18/11.68
E	Overall Width	11.94/12.95
E_1	Row Spacing	9.91/10.92
E_2	Body Width	11.18/11.68
JEDEC Designation		MS-007AA

NOTE: Index is centered on "D" side.

A. Dimensions shown as ____ / ____ are Min./Max.
B. Lead thickness is measured at seating plane or below.
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D. Exact body and lead configuration at vendor's option within limits shown.

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