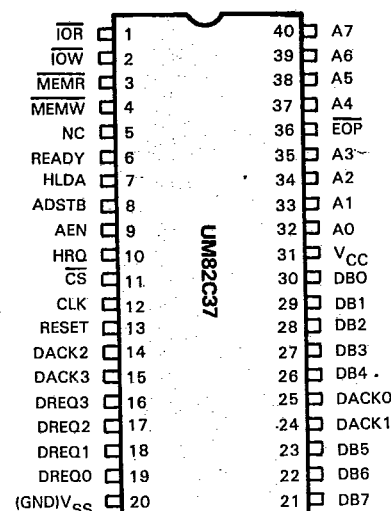# UM82C37

CMOS High Performance Programmable DMA Controller

FEATURES

- Compatible with the NMOS 8237A
- Four Independent Maskable Channels with Autoinitialization Capability
- Expandable to any Number of Channels
- Memory-to-memory Transfers
- Static CMOS Design Permits Low Power Operation
  - ICCOP = 2 mA/MHz Maximum
  - ICCSB = 10 μA Maximum
- Fully TTL/CMOS Compatible
- High Speed Data Transfers up to 4 MBytes/sec with 8 MHz Clock
- Upgraded Capabilities Allow Software Read of Internal Registers

PIN CONFIGURATION

Pin	Signal		Pin	Signal
1	$\overline{IOR}$		40	A7
2	$\overline{IOW}$		39	A6
3	$\overline{MEMR}$		38	A5
4	$\overline{MEMW}$		37	A4
5	NC		36	$\overline{EOP}$
6	READY		35	A3
7	HLDA		34	A2
8	ADSTB		33	A1
9	AEN		32	A0
10	HRQ		31	V_{CC}
11	$\overline{CS}$		30	DB0
12	CLK		29	DB1
13	RESET		28	DB2
14	DACK2		27	DB3
15	DACK3		26	DB4
16	DREQ3		25	DACK0
17	DREQ2		24	DACK1
18	DREQ1		23	DB5
19	DREQ0		22	DB6
20	(GND)V_{SS}		21	DB7

UM82C37

UM82C54/-2 CMOS Programmable Interval Timer

FEATURES

- Compatible with most Microprocessors Including 8080A, 8085A, iAPX88 and iAPX86
- Handles Inputs from DC to 10 MHz
- Six Programmable Counter Modes
- Status Read-back Command
- Three Independent 16-bit Counters
- Binary or BCD Counting
- Single +5V Supply
- iAPX88 and iAPX86 are all Trademarks of Intel Microsystem

PIN CONFIGURATION

Pin	Signal		Pin	Signal
1	D7		24	V_{CC}
2	D6		23	$\overline{WR}$
3	D5		22	$\overline{RD}$
4	D4		21	$\overline{CS}$
5	D3		20	A_1
6	D2		19	A_0
7	D1		18	CLK2
8	D0		17	OUT2
9	CLK 0		16	GATE2
10	OUT 0		15	CLK1
11	GATE 0		14	GATE1
12	GND		13	OUT1

UM82C54/-2