T-75-33-05

U M C

2400 BPS MODEM DATA PUMP

(Preliminary)

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UMC 2400 bps Modem Chip Set Oct. 1989

INTRODUCTION

The UMC 2400 bps modem chip set is a 2-wire full duplex, synchronous and asynchronous CCITT V.22 bis modem data pump. It is designed to operate over the public switched telephone network (PSTN), as well as leased lines. This chip set is used in conjunction with an external controller such as Intel 8051, to implement a 2400 bps full duplex modem. The external controller performs all modem controls and some modem functions.

The UMC modem chip set contains two chips -- UM92240 DSP chip and UM92241 AFE. The UM92240 DSP chip performs most of the receiving functions. The other chip UM92241 AFE performs most of the transmission functions and some of the receiving functions.

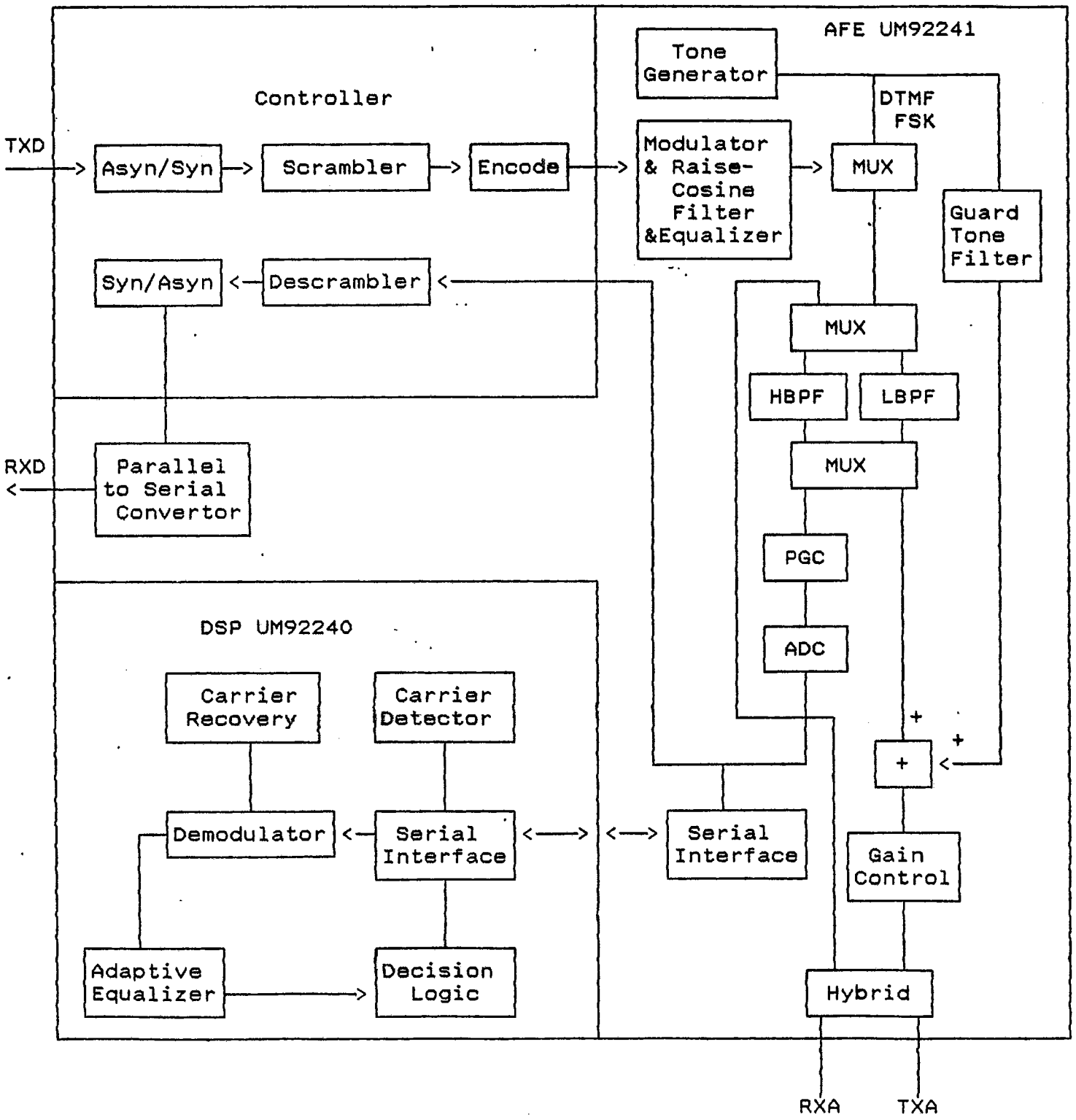
This modem chip set operates at 2400 bps QAM and 1200 bps PSK as well as 0 to 300 baud FSK modes, compatible with Bell 212A and 103 as well as CCITT V.22 bis, V.22 and V.21 standards. When used with external controller, the UMC 2400 bps modem chip set performs industry standard "AT" command set, and becomes an intelligent modem.

When used with Bus Interface chip UM92242,an internal modem will be easily implemented. The UM92242 has a built-in UART and some circuits that are usually found in interfacing with IBM compatible PC bus slot. This minimizes the component count in implementing the internal modem.

FEATURES

- Compatibility :
  - -- CCITT: V.22 bis, V.22 and V.21.
  - -- Bell: Bell 212A and 103.
- Loopback :
  - -- Analog
  - -- Digital
  - -- Remote Digital
- On chip DTMF/GUARD tone generator.
- On chip hybrid circuit.
- Easily controlled by microcontroller.
- Low power consumption :
  - -- DSP 1.5 micron CMOS technology
  - -- AFE 3.5 micron CMOS technology
- Audio interface for phone line monitoring.
- Programmable audio output level control.
- Both DSP and AFE in 28 pin DIP or PLCC packages.
- Needs only one clock source.

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

POWER-UP INITIAL CONDITION

After power up, some initialization process should be provided for this data pump. Following power up, the data in the registers of AFE chip UM92241 are undefined, and the output pins may deliver unwanted signals. Control registers of UM92241 must be properly programmed to obtain the wanted operation. The DSP chip UM92240 will be initialized and execute program from the starting address 0 after an active high pulse on RESET pin.

ACCESSIBLE REGISTERS

The operation of the UMC 2400 bps modem pump is based on a set of 4 bit accessible registers. These accessible registers contain ten write-only and two read-only registers. By writing data into the write-only registers, we can control the operation of this data pump; By reading data from the read-only registers, we can get the line status information and the received data from the data pump. These registers are listed in Table 2.

The read/write operation of this data pump is based on seven pins : write enable WRB, read enable RDB, data/address select DASEL, and address/data pin AD3 to AD0. In order to minimize the pin count, AD3-AD0 are used as dual functional pins selected by DASEL. When DASEL is low, AD3-AD0 are used as address input pins. When DASEL is high, AD3-AD0 are used as data input pins.

For example, when we want to write/read data to/from some AFE register, say register 3, the operations are as follow :

First we should point to register 3 , use AD3-AD0 as address bus:
. WRB active low, DASEL low, and AD3-AD0 = 03.
Second we then write/read data to/from register 3, use AD3-AD0 as data bus:
WRB/RDB active low, DASEL high, and AD3-AD0 are used as data input/output pins.

OPERATING MODE AND SPEED

The operating speed and mode are determined by SPEED2-0 and MODE1-0.

Operating Mode :

There are four operating modes in this data pump. Note that, the operating modes control the operations of DSP only, and have no effect on the AFE. That is, the operating modes control the operations of the receiver, not the transmitter. MODE1-0 = 00 , 01 , 10 , 11 will force the DSP chip UM92240 to operate in Modem Off, Protocol, Data, CPM detect modes respectively.

In the Modem Off mode,the UM92240 will initialize all the registers in UM92240 and idle there waiting for the operating mode to change.

In Protocol mode, the DSP uses two high-Q filters to determine if the incoming signal is 2225 Hz or 2100 Hz, and reflects the result on AFE register bits 2225Hz and 2100Hz.

In Data mode, the UM92240 performs the functions of demodulation, gain control, carrier recovery, timing recovery, and decision, according to SPEED2-0 setting, then sends the decoded data to AFE register bits RD3-0.

In CPM detect mode, the UM92240 sets the AFE register bit CD if the signal on the line exceeds the predefined threshold level. This is useful in call progress monitoring.

Operating Speed :

There are three operating speeds in this data pump : 2400 bps QAM , 1200 bps PSK, and 0 to 300 bps FSK. In 2400 and 1200 bps, there are further distinctions between the receiver adaptive equalizer turn on and off.

SPEED2-0 = 0X0 , 0X1 , 101 , 111 will set the data pump operating at 2400, 1200, 0 to 300 bps V.21, and BELL 103 respectively. In 2400 and 1200 bps, SPEED1 determines if the adaptive equalizer in UM92240 will turn on or not. Note that, SPEED1 has no influence on AFE UM92241 because the compromise equalizer in the transmitter is always on when operating at 2400 or 1200 bps.

TRANSMISSION

All the transmission functions of the data pump are performed in AFE chip UM92241. The signals which can be transmitted include QAM, PSK, FSK, DTMF tone, 2100/2225 Hz answer tone, and .550/1800 Hz guard tone. TONE2-0 determine which signal will be generated.

QAM, PSK, Guard tone :

When TONE2-0 = 000/100/101 , the QAM or PSK signal will be generated. In the case of 100/101, the 550/1800 guard tone will be generated together with QAM or PSK signal.

The QAM/PSK signal to be generated is decided by bits A/OB and TD3-0 in UM92241 registers. A/OB selects answer or originate mode (high or low band). TD3-0 select one of sixteen constellation points to be transmitted (refer to Fig. 2 and Table 1). The modulated output Z(t) is then passed to raised-cosine filter and compromise equalizer. Where Z(t) = X COS(Wct) - Y SIN(Wct).

Because the TD3-0 represents the encoded data, the functions of asynchronous to synchronous conversion(if in asynchronous mode), scrambling, and encoding should be performed by the external device.

FSK :

TONE2-0 = 010, 011 enables FSK modulation for BELL 103, V.21 . A/OB selects answer or originate mode, and TD0 selects 1 (mark) or 0 (space) to be transmitted.

DTMF tone :
Setting TONE2-0 = 001 enables the DTMF generator. The dialed digit to be transmitted is selected by DTMF H2, DTMF H1, DTMF L2, and DTMF L1. DTMF H2 and DTMF H1 select high group (column) frequencies and DTMF L2 and DTMF L1 select low group (row) frequencies. For detailed information, see registers description.

Answer Tone :
Setting TONE2-0 equal to 110, 111 enable 2225 Hz, 2100 Hz answer tone respectively.

Transmitter Gain Control :
The data pump provides three bits TG2-0 to control the transmitted signal level from 0 to -14 dB with 2 dB resolution.

RECEIVING

Most of the receiving functions of the data pump are performed in DSP chip UM92240. The AFE chip UM92241 just performs the functions of filtering, amplification (by PGC), and analog to digital conversion (by ADC).
The signals received are first passed to a band pass filter to reject the unwanted out-of-band noise. The filtered signal is then amplified by the programmable gain control circuit (PGC) with amplification factor determined by DSP. The analog output signal of PGC then passed to ADC to get 10 bits of digital data and passed to the DSP chip for further processing.

The DSP chip UM92240 performs the functions of demodulation, gain control, carrier recovery, timing recovery, decision, and decoding. The decoded data are passed to UM92241 and stored in RD3-0.

QAM/PSK :
When operating at 2400 or 1200 bps, RD3-0 are updated at baud rate (600 Hz). For 2400 bps, RD3-0 represents the 4 bits of received data. (RD3 is the first bit.) For 1200 bp only RD3-2 represents the 2 bits of received data. (RD3 is the first bit too.) In this case, RD1-0 has no meaning.
The received data RD3-0 should be further processed by external controller including descrambling, synchronous to asynchronous conversion (if in asynchronous mode). The processed data is then sent back to AFE UM92241 8 bits parallel to serial converter through ASD7-0 to shift out via RSD pin.
The parallel to serial converter uses an 8 bit buffer for buffering data from ASD7-0 and a bit EMPTY to indicate if it is ready to accept data. When the 8 bit shifter has shifted out the last bit, it will load 8 bits of data from the buffer and set the EMPTY flag automatically. The EMPTY flag informs the external controller that the converter is ready to accept another 8 bits of data. After the empty buffer has been loaded with another 8 bits of data from the external controller, the EMPTY will be cleared.
The converter uses a clock at a rate of about 2400 Hz to shift the 8 bits of data. In asynchronous normal speed transmission the clock is about 2400 Hz ; In asynchronous over-speed transmission, the clock will be a little higher ; In synchronous transmission, the clock is synchronous with SCR.

When operate in PSK, because the transmission speed is about 1200 bps, the data from external controller must be duplicated before writing into ASD7-0. For example,the 4 bits data after synchronous to asynchronous conversion are 1001, they must be duplicated into 11000011 before sending to ASD7-0.

FSK :
When operated in FSK 0 to 300 bps, only RD0 represents the received data bit, RD3-1 have no meaning. In this speed, RD0 is updated of a rate of 7200 Hz and directly connected to RSD pin.

CLOCK GENERATION

Transmit DPLL :

The TXDPLL can be synchronized on an external terminal clock tied to SCTE pin or on the receive bit rate signal SCR generated from RXDPLL. It can also run free without any phase shift.
When the internal clock is out of phase with the selected reference clock, the TXDPLL operates by adding or subtracting pulses to a 691.2 KHz internal clock every 1/600 second until the internal clock is in phase with the selected reference clock.
The TXDPLL outputs two clock signals : SCT and TBR.
The SCT is a bit rate clock. This signal is useful when DTE operates in synchronous transmission mode.

TBR :
For FSK mode when FSKC is set, the TBR is always a 4800 Hz clock that can be used by external controller to sample the 0 to 300 bps data stream from DTE.
For the QAM/PSK mode, there are some differences between asynchronous and synchronous operation. For asynchronous operation,the TBR is a 600 Hz active low pulse with 4.34 microsecond duration. Because the transmitter uses the high-go-low edge of TBR to latch TD3-0 into modulator, TBR can be used to activate the interrupt service routine in the external controller program to load other TD3-0 data into AFE. For synchronous operation, the TBR is identical to SCT, i.e. , 2400 Hz clock for QAM and 1200 Hz clcok for PSK. It can be used by external controller to sample the synchronous data stream from DTE and load TD3-0 to AFE every four (for QAM) or two (for PSK) clocks of TBR.

Receive DPLL :
The RXDPLL synchronizes the internal clock with the reference clock derived from the received signal and outputs two synchronous signals SCR and RBR. The SCR is a bit rate clock and can be used by DTE to sample the serial data stream output by RSD pin. The RBR is a 600 Hz active low pulse with 4.34 microsecond duration. Because the receiver uses the high-go-low edge of RBR to update the received data RD3-0, RBR can be used to activate the interrupt service routine in the external controller program to read RD3 from AFE.

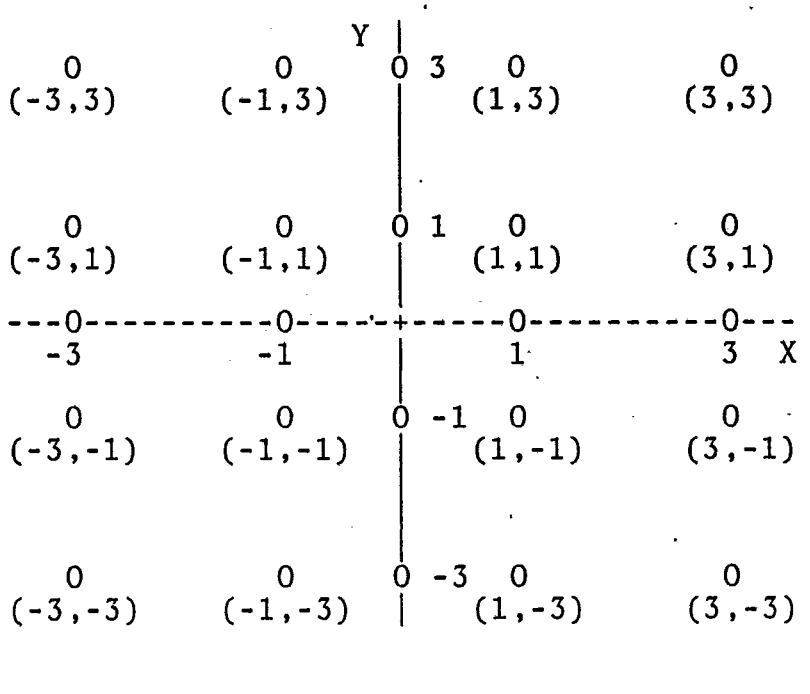


Figure 2. 16-QAM/4-PSK Constellation

TD3	TD2	TD1	TD0	(X, Y)
0	0	0	0	(+1,+1)
0	0	0	1	(+3,+1)
0	0	1	0	(+1,+3)
0	0	1	1	(+3,+3)
0	1	0	0	(+1,-1)
0	1	0	1	(+1,-3)
0	1	1	0	(+3,-1)
0	1	1	1	(+3,-3)
1	0	0	0	(-1,+1)
1	0	0	1	(-1,+3)
1	0	1	0	(-3,+1)
1	0	1	1	(-3,+3)
1	1	0	0	(-1,-1)
1	1	0	1	(-3,-1)
1	1	1	0	(-1,-3)
1	1	1	1	(-3,-3)

Table 1. TD3-0 Mapping

ACCESSIBLE REGISTER DESCRIPTION

ADDRESS	DATA				Type
	BIT3	BIT2	BIT1	BIT0	
00H	0	TONE 2	TONE 1	TONE 0	Write Only
01H	DTMF H2 / TD3	DTMF H1 / TD2	DTMF L2 / TD1	DTMF L1 / TD0	Write Only
02H	ALB	A/OB	HYBRID ON/ $\overline{\text{OFF}}$	SYNC/$\overline{\text{ASYNC}}$	Write Only
03H	$\overline{\text{SQUELCH}}$	TG2	TG1	TG0	Write Only
04H	CLOCK 1	CLOCK 0	TLAC1	TLAC0	Write Only
05H	OVERSPEED/ $\overline{\text{NORMAL}}$	SPEED2	SPEED 1	SPEED 0	Write Only
06H	Reserved	FSKC	MODE 1	MODE 0	Write Only
07H	ASD7	ASD6	ASD5	ASD4	Write Only
08H	ASD3	ASD2	ASD1	ASD0	Write Only
0BH	TEST 3	TEST 2	TEST 1	TEST 0	Write Only
0CH	RD3/2225HZ	RD2/2100HZ	RD1	RD0	Read Only
0DH	CD	S1	Reserved	EMPTY	Read Only

Table 2. Accessible Registers.

TONE 2 - TONE 0

The three bits TONE2 - TONE0 are used to select TXA output functions.

Tone2	Tone1	Tone0	Function
0	0	0	All tones disable
0	0	1	DTMF enable
0	1	0	103 FSK enable
0	1	1	V.21 FSK enable
1	0	0	Guard tone enable (550 HZ)
1	0	1	Guard tone enable (1800 HZ)
1	1	0	2225 HZ answer tone
1	1	1	2100 HZ answer tone

DTMF H2 / TD3
DTMF H1 / TD2
DTMF L2 / TD1
DTMF L1 / TD0

These four bits can be used either as DTMF selection bits or as transmit data bits.
When DTMF is enabled (TONE2-0 = 0 0 1), these four bits are DTMF selection bits; If DTMF is not enabled, these four bits are transmit data bits.

DTMF H2	DTMF H1	Tone Out	
0	0	1209 HZ	Column 1
0	1	1336 HZ	Column 2
1	0	1477 HZ	Column 3
1	1	1633 HZ	Column 4

DTMF L2	DTMF L1	Tone Out	
0	0	697 HZ	Row 1
0	1	770 HZ	Row 2
1	0	852 HZ	Row 3
1	1	941 HZ	Row 4

ALB

Analog Loop Back bit.
When this bit is enabled, the transmitter's analog output is coupled to the receiver's analog input at a point near the modem's telephone line interface, and both the transmitter and receiver operate at the same band selected by A/OB bit.

A/$\overline{O}$

Answer mode or Originate mode selection bit.
When this bit is high,modem transmits at high band and receives at low band ; When this bit is low, modem transmits at low band and receives at high band.

HYBRID ON/$\overline{\text{OFF}}$

When this bit is on, internal hybrid circuit will be on; When it is off, internal hybrid circuitry will be off, and user should provide hybrid circuit externally.

SYNC/$\overline{\text{ASYNC}}$

When this bit is a 1, synchronous mode is selected; When 0, asynchronous mode is selected.

$\overline{\text{SQUELCH}}$

When this bit is a 0, squelch is enabled : Transmitter doesn't output any signal, but the receiver still works as in normal operation.

TG2, TG1, TG0

Transmitter output gain control.

TG2	TG1	TG0	Transmitter gain
1	1	1	0 dB
1	1	0	-2 dB
1	0	1	-4 dB
1	0	0	-6 dB
0	1	1	-8 dB
0	1	0	-10 dB
0	0	1	-12 dB
0	0	0	-14 dB

CLOCK1, CLOCK0

These two bits select transmitter clock source.

Clock1	Clock0	TX clock source
0	0	Internal SCT
0	1	Not used
1	0	External SCTE
1	1	Slave to SCR

ALAC1, ALAC0

Audio Level Attenuation Control.

ALAC1	ALAC0	Audio level attenuation
0	0	audio off
0	1	-12 dB
1	0	-6 dB
1	1	0 dB

(continued)

OVERSPEED/$\overline{\text{NORMAL}}$	This bit selects the modem operating at overspeed mode or normal speed mode. According to CCITT V.22bis,when the intercharacter signaling rate provided by the DTE on transmitted data is 2400 or 1200 bit/s +1 % , -2.5 % , normal speed operation is selected ; When signaling rate is 2400 or 1200 bit/s +2.3 % , -2.5 % , overspeed speed mode should be selected.
SPEED2, SPEED1, SPEED0	These three bits select modem operating speeds. Speed2 Speed1 Speed0 Function 0 0 0 V.22 bis 2400 bps with Adaptive Equalizer OFF 0 0 1 V.22 bis/V.22 1200 bps with Adaptive Equalizer OFF 0 1 0 V.22 bis 2400 bps with Adaptive Equalizer ON 0 1 1 Bell 212 1200 bps, or V.22 1200 bps With Adaptive Equalizer ON 1 0 0 Not Used 1 0 1 V.21 1 1 0 Not used 1 1 1 Bell 103
MODE1 , MODE0	These two bits select DSP program operating modes. Mode1 Mode0 Function 0 0 Modem OFF 0 1 Protocol Mode 1 0 Data Mode 1 1 CPM Mode
ASD7 - ASD0	These 8 bits store the received data after descrambler, and synchronous to asynchronous converter (if asynchronous mode is selected). These 8 bits of data will be serially shifted out via the RSD pin.
TEST3 - TEST0	Reserved for factory testing only. Should be loaded by 0 in normal operation.

(continued)

RD3 / 2225 HZ RD2 / 2100 HZ RD1 RD0	1.When in data mode (MODE1=1, MODE0=0), these four bits represent the received data after demodulation and decoding. In FSK mode, only RD0 represents the received data after demodulation; The other three bits don't have any meaning. At 1200 bps speed, only RD3, RD2 represent the the received data after demodulation; RD1, RD0 has no any meaning. At 2400 bps speed, all four bits represent the received data. These data need further processing (except FSK mode) -- descrambler, and optional synchronous to asynchronous conversion (if operating in asynchronous transmission) - before loading back to AFE ASD7-0. 2.When in protocol mode (MODE1=0, MODE0=1), BIT3 and BIT2 indicates a 2225 Hz or a 2100 Hz tone has been detected. BIT1 and BIT0 has no meaning.
CD	When this bit is on, it represents valid carrier signal (energy above -43 dBm , and the recommended band) has been detected.
S1	When this bit is on, it means that the unscrambled binary 1 of handshaking has been detected.
EMPTY	This bit indicates if the parallel to serial data conversion buffer is empty, and can be loaded with another 8 bits of data.

TECHNICAL SPECIFICATIONS

DTMF, GUARD TONE, ANSWER TONE GENERATORS

a). For Frequency:

Parameter	Nominal Frequency	Allowable Error
Row 1	697 HZ	+ - 1 %
Row 2	770 HZ	+ - 1 %
Row 3	852 HZ	+ - 1 %
Row 4	941 HZ	+ - 1 %
Column 1	1209 HZ	+ - 1 %
Column 2	1336 HZ	+ - 1 %
Column 3	1477 HZ	+ - 1 %
Column 4	1633 HZ	+ - 1 %
Guard Tones	550 HZ	+ - 20 HZ
	1800 HZ	+ - 20 HZ
Answer Tones	2100 HZ	+ - 15 HZ
	2225 HZ	+ - 10 HZ

b). For Level:

Parameter		Min.	TYP.	Max.	Unit
Second Harmonic Distortion			-40		dB
Row Output Level			0		dBm
Column Output Level			2		dBm
Transmit level measured at TXA	Normal operation:		0		dBm
	Squelched operation:		-50		dBm
550 HZ Guard Tone			-3		dB (Note 2)
1800 HZ Guard Tone			-6		dB (Note 2)
2100 HZ Answer Tone			0		dB

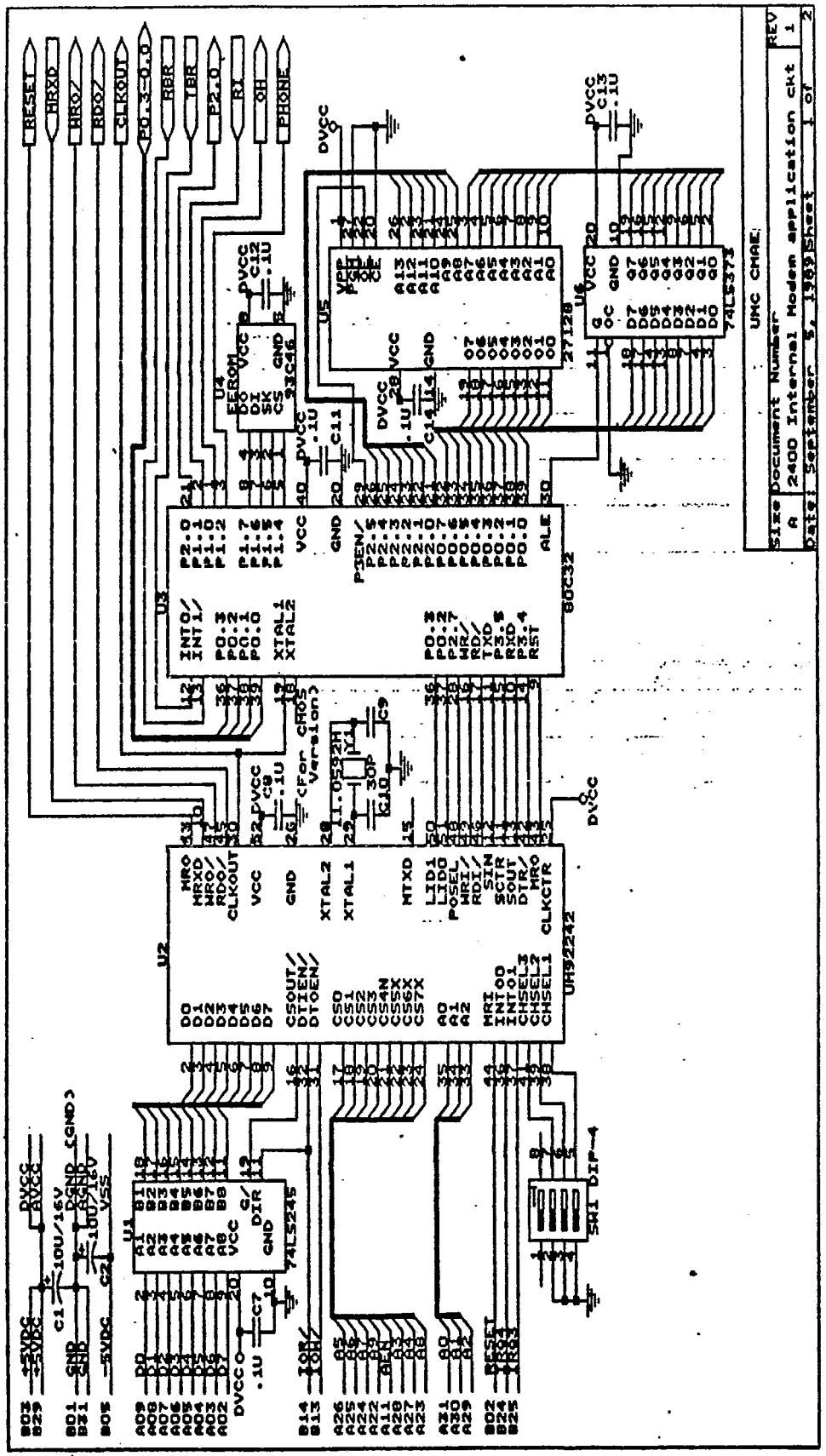
Note: 1. Condition:
VDD= +5V, VSS= -5V, GND= 0V ; TG2=TG1=TG0=0
Measured at TXA pin.
2. These levels are referenced to the TXA real signal level. When guard tones are added, the TXA real signal level is adjusted to maintain a constant level on the line.
For 1800 HZ, the adjustment is -0.97dB;
For 550 HZ, the adjustment is -1.76dB.

TRANSMITTER SIGNAL AND DATA RATE

Operating Mode	Signaling Rate(Baud)	Data Rate
V.22 bis	600 + - 0.01 %	2400 or 1200 bps + - 0.01 %
V.22	600 + - 0.01 %	1200 bps + - 0.01 %
Bell 212A	600 + - 0.01 %	1200 bps + - 0.01 %
V.21 or Bell 103	0 to 300	0 to 300 bps

TRANSMITTER CARRIER FREQUENCY

Operating Mode	Carrier Frequency	Allowable Error
V.22 bis or V.22 or Bell 212A	2400 HZ (High Band)	+ - 1 HZ
	1200 HZ (Low Band)	+ - 0.5 HZ
V.21	Answer Mark: 1650 HZ	+ - 6 HZ
	Answer Space: 1850 HZ	+ - 6 HZ
	Originate Mark: 980 HZ	+ - 6 HZ
	Originate Space: 1180 HZ	+ - 6 HZ
Bell 103	Answer Mark: 2225 HZ	+ - 6 HZ
	Answer Space: 2025 HZ	+ - 6 HZ
	Originate Mark: 1270 HZ	+ - 6 HZ
	Originate Space: 1070 HZ	+ - 6 HZ



PLICATION INFORMATION