Frequency synthesizer for cellular radio communication UMA1014T

FEATURES

- Single chip synthesizer solution;
- Compatible with Philips Cellular Radio chipset;
- Fully programmable RF divider;
- IIC two-line serial bus interface;
- On chip crystal oscillator\TCXO buffer from 3 to 16 MHz;
- 16 reference division ratios allowing 5 to 100 kHz channel spacing;
- Crystal frequency divide-by-8 output;
- On chip out-of-lock indication ;
- Two VCO control outputs;
- Latched synthesizer alarm output;
- Status register including out-of-lock indication and power failure;
- Power down mode.

QUICK REFERENCE DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC & VCP	Supply voltage range	4.5	5.0	5.5	V
ICC + ICP	Supply current	-	13	-	mA
ICCpd	ICC in power down	-	2.5	-	mA
FREF	Phase comparator reference frequency	5	-	100	KHz
RFin	RF frequency input	50	-	1100	MHz
Tamb	Operating temperature range	-40	-	85	°C

APPLICATIONS

- Cellular mobile radio (NMT, AMPS, TACS)
- Private Mobile Radio (PMR)
- Cordless telephones

GENERAL DESCRIPTION

The UMA1014T is a low power universal synthesizer which has been designed for use in channelized radio communications. The IC is manufactured in bipolar technology and is designed to operate from 5 to 100 kHz channel spacing with an RF input of 50 to 1100 MHz. The channel is programmed via the standard IIC bus. A low power sensitive RF divider is integrated as well as a dead zone eliminated tri-state phase comparator. A low noise charge pump delivers 1 mA or 1/2 mA output current enabling better compromise between fast switching and loop bandwidth. A power down circuit allows the synthesizer to be idled.

ORDERING AND PACKAGE INFORMATION

Extended Type number	Package			
	Pins	Pin Position	Material	Code
UMA1014T	16	SO16	plastic	SOT109A
UMA1014M	20	SSOP20	plastic	SOT266A

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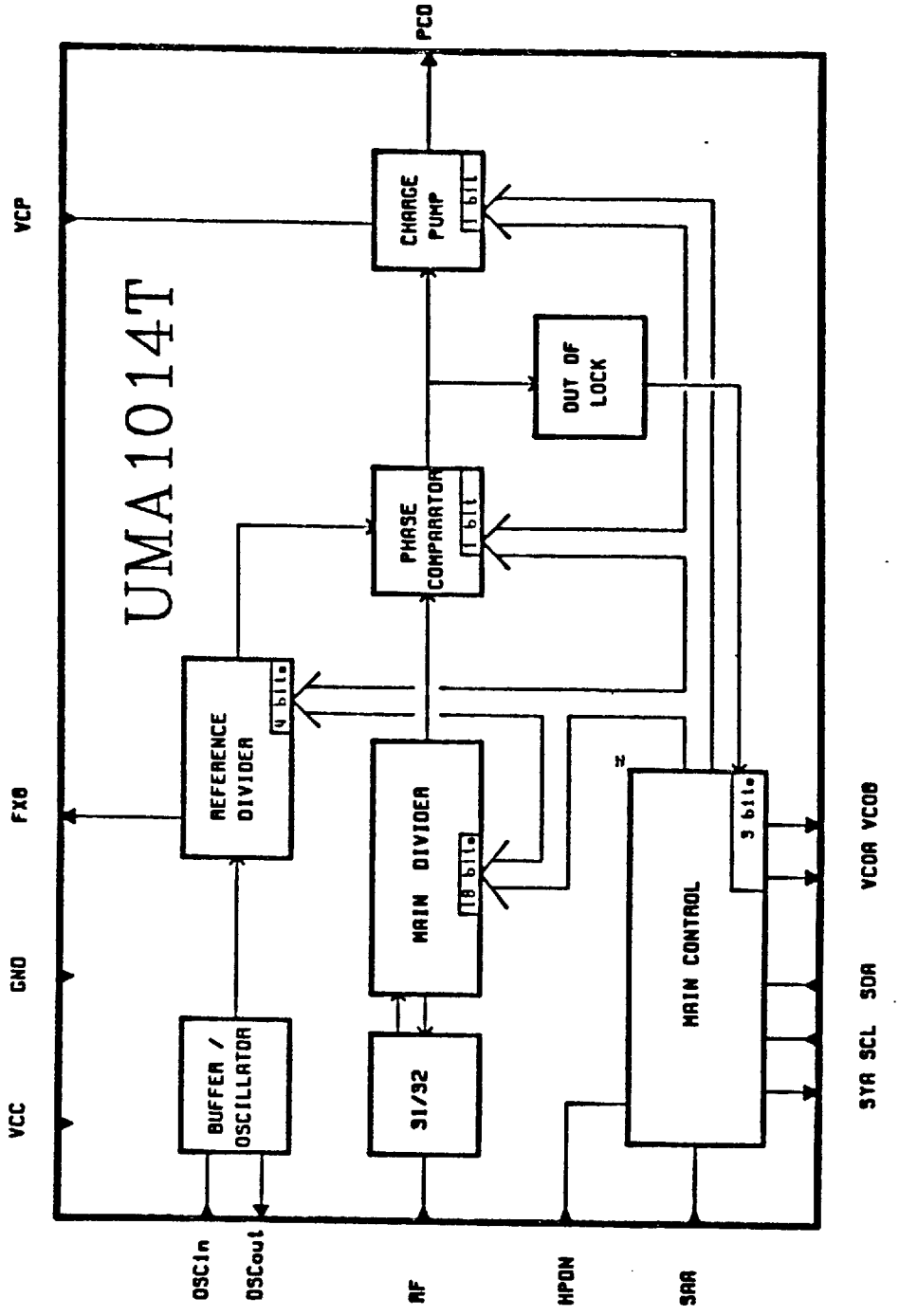
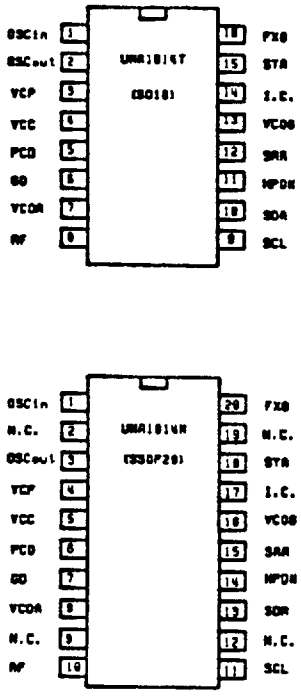


FIG. 1 Block diagram

FIG 2 PIN CONFIGURATION



PINNING

Symbol	Pin		Description
	SO16	SSOP20	
OSCin	1	1	Oscillator input or TCXO input
OSCout	2	3	Oscillator output
VCP	3	4	Charge pump 5 Volts supply
VCC	4	5	5 Volts supply
PCD	5	6	Charge pump output
GD	6	7	Ground
VCOA	7	8	VCO buffer switch output A (including out-of-lock)
RF	8	10	RF input
SCL	9	11	Serial clock line input
SDA	10	13	Serial data line input/output
HPDN	11	14	Hardware power down (low active)
SAA	12	15	Slave address select input A
VCOB	13	16	VCO buffer switch output B
I.C.	14	17	Internally connected (for test purpose only)
SYA	15	18	Synthesizer alarm output
FX8	16	20	1/8 crystal frequency output
N.C. = not connected			

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

Symbol	Parameter	Min	Max	Unit
VCC	Supply voltage range	-0.3	7	V
Vi	Voltage range at pin i to ground	0	Vcc	V
Tstg	Storage temperature range	-55	+125	°C
Tamb	Operating ambient temperature range	-40	85	°C

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class A (method 3015-2). Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling Integrated Circuits.

FUNCTIONAL DESCRIPTION

The UMA1014T is a low power frequency synthesizer for radio communications which operates in the 50 to 1100 MHz range. The device includes an oscillator\buffer circuit, a reference divider, an RF main divider, a tri-state phase comparator, a charge pump and a control circuit which transfers the serial data into the four internal 8 bit-registers. The VCC supply feeds the logic part while VCP feeds the charge-pump only. Both supplies are +5 Volts (+/- 10%). The power down facility puts the synthesizer in the idle mode (all current supplies are switched off except in the control part). Any IIC transfer is permitted during this mode and all information in the registers is retained allowing fast power-up.

MAIN DIVIDER.

The main divider is a fully programmable pulse swallow type counter. After a sensitive input amplifier (50 mV, -13 dBm), the RF signal is applied to a 31/32 dual-modulus counter. The output is then used as the clock for the 5-bit swallow counter R= (MD4,..., MD0) and the 13 bit main counter N= (MD17, ..., MD5). The ratio is sent via the IIC bus into the registers B, C and D. It is then buffered in a 18-bit latch. The ratio in the divider chain is updated with this new information only after the least significant bit (D0) is received. This update is synchronized to the output of the divider in order to limit the phase error during small jumps of the synthesized frequency.

MAIN COUNTER								SWALLOW COUNTER		
:N								:R		
MD17	MD16	MD15		MD8	MD7		MD5	MD4		MD0
B1	B0	C7	...	C0	D7	...	D5	D4	...	D0
MSB										LSB

Division ratio in the main divider

The main divider can be programmed to any value between 2048 and 262143 (i.e. 2^{18}-1). If a ratio X, which is less than 2048, is sent to the divider, the ratio (X+2048) will be programmed. For switching between adjacent channels it is possible to program only register D allowing shorter IIC programming time.

OSCILLATOR.

The oscillator is a common collector Colpitts type with external capacitive feedback. It has been designed to function also as a buffer when a TCXO or any clock is used. The oscillator has very small temperature drift and high voltage supply rejection. When acting as a buffer, no additional external components will be necessary.

REFERENCE DIVIDER.

The reference divider is semi-programmable with 16 division ratios which are selected via the IIC bus. The programming uses bits A3 to A0 of register A as shown below. These ratios can be used with crystal frequencies from 3 to 16 MHz. All popular channel spacings can be obtained from a single crystal / TCXO frequency of 9.6 MHz.

A3	A2	A1	A0	reference division ratio	Channel spacing for 9.6 MHz at OSCin
RD3	RD2	RD1	RD0		
0	0	0	0	128	75 kHz
0	0	0	1	160	60 kHz
0	0	1	0	192	50 kHz
0	0	1	1	240	40 kHz
0	1	0	0	256	37.5 kHz
0	1	0	1	320	30 kHz
0	1	1	0	384	25 kHz
0	1	1	1	480	20 kHz
1	0	0	0	512	18.75 kHz
1	0	0	1	640	15 kHz
1	0	1	0	768	12.5 kHz
1	0	1	1	960	10 kHz
1	1	0	0	1024	9.375 kHz
1	1	0	1	1280	7.5 kHz
1	1	1	0	1536	6.25 kHz
1	1	1	1	1920	5 kHz

reference divider programming

PHASE COMPARATOR AND CHARGE PUMP.

The block diagram of the phase comparator and charge pump is shown below. The phase comparator is both a phase and frequency detector. It comprises dual flip-flops together with logic circuitry which eliminates the dead zone. When a phase error is detected, the UP or DOWN signal becomes high . It switches on the corresponding current generator which sources or sinks current as appropriate into the loop filter. When no phase error is detected, PCD goes tristate. The final tuning voltage of the VCO is provided by the loop filter. The charge pump current is programmable via the IIC bus. When bit IPCD (bit A5) is set to logic 1, the charge pump will deliver 1 mA. When IPCD is logic 0, the charge pump will deliver 0.5 mA.

The phase comparator has a phase inverter logic input (PHI). This allows the use of inverted or non-inverted loop filter configurations. It is thus possible to use a passive loop filter which can offer high performance without an operational amplifier. The function of the phase comparator and charge pump is given in the table below and a typical transfer curve is shown overleaf.

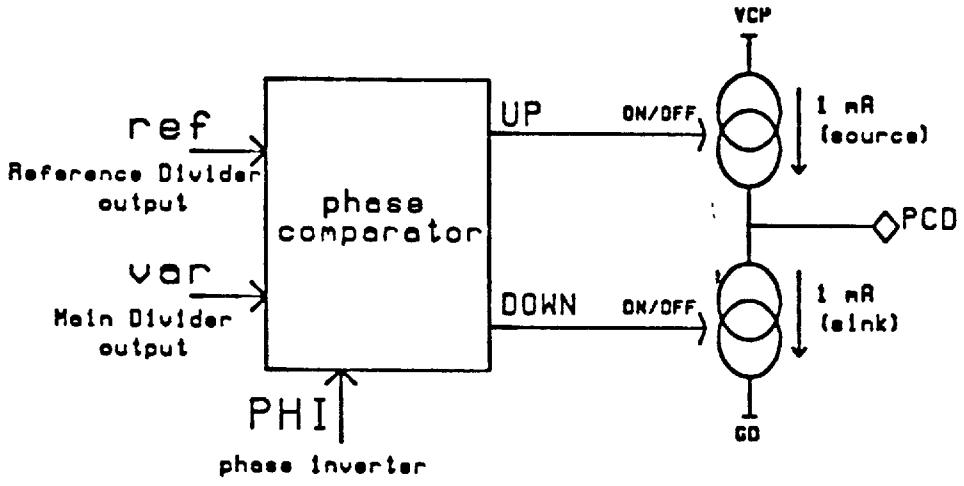


FIG. 3 Phase comparator and charge pump

	PHI = 0 (Passive loop filter)			PHI = 1 (Active loop filter)		
	Fref<Fvar	Fref>Fvar	Fref=Fvar	Fref<Fvar	Fref>Fvar	Fref=Fvar
UP	0	1	0	1	0	0
DOWN	1	0	0	0	1	0
Ipcd	- 1 mA	1 mA	< +/- 5 nA	1 mA	- 1 mA	< +/- 5 nA

Operation of the phase comparator

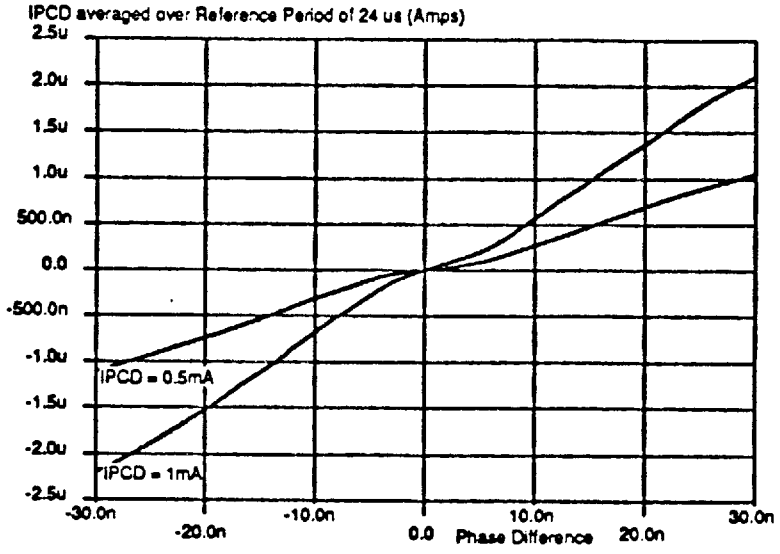


FIG. 4 Gain of phase detector and charge pump

OUT-OF-LOCK DETECTOR.

An out-of-lock detector using the UP and DOWN signals from the phase comparator is included on chip. Pin VCOA is an open collector output which is forced low during out-of-lock. This information is also available via the IIC bus in the status register. When the phase error (measured at the phase comparator) is greater than approximately 200 ns, an out-of-lock condition is immediately flagged. The flag is only released after 6 reference cycles of phase error less than 200 ns.

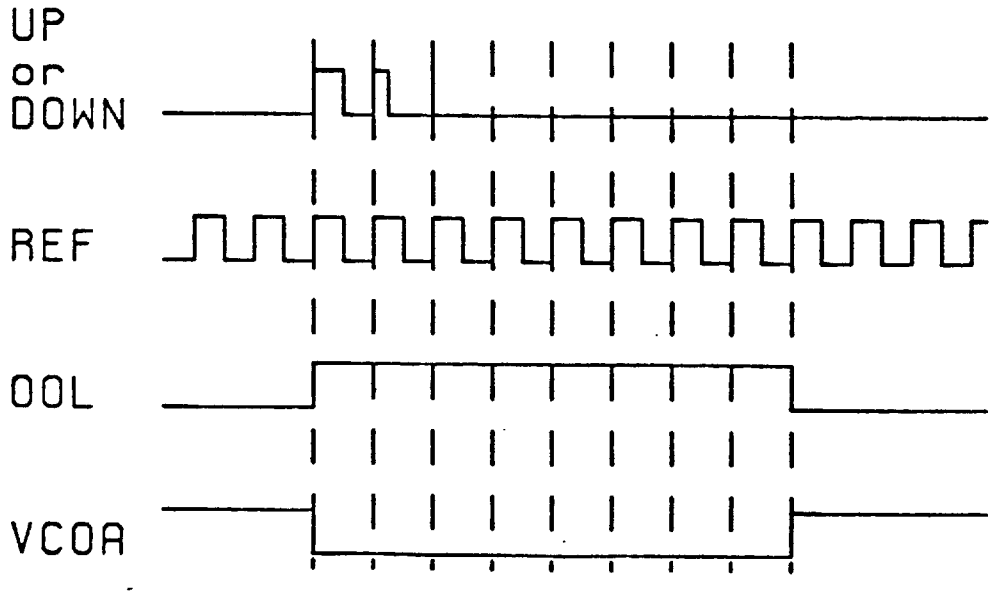


FIG. 5 Out-of-lock function

MAIN CONTROL

The control part consists mainly of the IIC control interface and a set of four registers, A, B, C and D. The serial input data (SDA) is converted to 8 bit parallel words and stored in the appropriate registers. The data transmission to the synthesizer is executed in the burst mode with the following format:

//slave addr./subaddr./data1/data2/.../datan// ; n up to 4.

Data byte 1 is written in the register indicated by the subaddress. An auto-increment circuit if enabled (AVI=1) then provides the correct addressing for the following data bytes. Since the length of the data burst is not fixed, it is possible to program the whole set of registers or just one. The registers are structured in such a way so that the burst, for normal operation, is kept as short as possible. The bits that are only programmed during the set-up (reference division ratio, power down, phase inversion and current on PCD) are stored in registers A and B.

In the slave address, six bits are fixed. The remaining two bits depend on the application.

1	1	0	0	0	1	SAAN	R/WN

Slave address

SAAN is the slave address select not. When SAA (pin 12) is high, then SAAN = 0, and when pin 12 goes low SAAN = 1. This allows the use of two UMA1014Ts on the same IIC bus with a different address. R/WN (read/write not) should be set to 0 when writing to the synthesizer or set to 1 when reading the status register.

The subaddress includes the register pointer, and sets the flags related to the auto-increment (AVI) and the alarm disable (DI) :

x	x	x	DI	AVI	x	SB1	SB0

Subaddress

DI (Disable Interrupt); DI=1 disables SYA alarm
DI=0 allows SYA alarm
AVI (Auto Value Increment); AVI=1 enables auto-increment
AVI=0 disables auto-increment
SB1/SB0 point to the register where DATA1 will be written. (see table attached)
x means not used.

SB1	SB0	register pointed
0	0	A
0	1	B
1	0	C
1	1	D

Pointer of the registers

MAIN CONTROL (continued)

When the auto-increment is disabled (AVI=0) , the subaddress pointer will maintain the same value during the IIC bus transfer. All the databytes will then be written consecutively in the same register pointed to by the subaddress.

STATUS REGISTER and synthesizer alarm.

When an out-of-lock condition or a power dip occurs, open collector output SYA (pin 15) is forced low and latched. The pin SYA will be only released after the status register is read via the IIC bus.

The status register contains information as shown below:

0	0	0	OOL	0	LOOL	LPD	DI

where : OOL momentary out-of-lock

LOOL latched out-of-lock

LPD latched power dip

DI disable interrupt (of the last write cycle)

The IIC bus protocol to read this internal register is a single byte without subaddressing:

//slave address (R/WN=1)/status register (read)//

MAIN CONTROL (continued)

BIT ALLOCATION :

BIT ALLOCATION										
register.	pointer.	7	6	5	4	3	2	1	0	preset
A	00	PD	X	IPCD	X	RD3	RD2	RD1	RD0	00001110
B	01	1	0	1	PHI	VCOB	VCOA	MD17	MD16	10100101
C	10	MD15	MD14	MD13	MD12	MD11	MD10	MD9	MD8	00111000
D	11	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	10000000

X means not used

register name	bit name	function		preset value
A	PD	power down	PD=0 normal operation	0
	IPCD	programmable current in PCD	IPCD=1 : 1mA IPCD=0 : 1/2mA	0
	RD3...RD0	reference ratio	see table	1110; r=1536
B	PHI	phase inverter	PHI=0 passive loop filter	0
	VCOA	VCO switch A	set the pin 7	1
	VCOB	VCO switch B	set the pin 13	0
	MD17 MD16	bits 17 and 16	MSB of main divider ratio	0 1
C	MD15 ... MD8	bits 15 ... 8	main divider ratio	00111000
	MD7 ... MD0	bits 7 ... 0	main divider ratio	10000000 r=80000

Registers in UMA1014T

CHARACTERISTICS

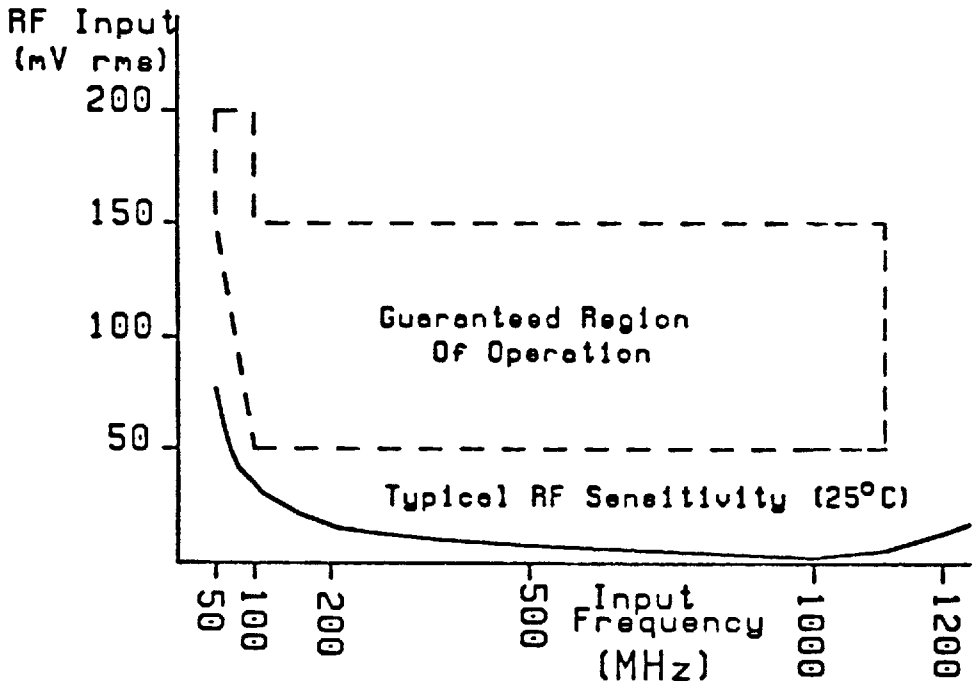
Vcc = 4.5 to 5.5V ; 25 deg; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit.
Supply (pins VCC & VCP).						
VCC	Supply voltage range		4.5	-	5.5	V
ICC	Supply current		-	11.5	-	mA
ICCpd	Supply current	power down	-	2.5	-	mA
VCP	Supply voltage of the charge pump		4.5	-	5.5	V
ICP	Supply current C-P	IPCD=0.5mA	-	1.4	-	mA
ICPpd	Supply current C-P	power down	-	0.01	-	mA
RF dividers (pin RF)						
F_{RF}	Frequency range		50	-	1100	MHz
V_{RFrms}	input voltage level	50 to 100 MHz	150	-	200	mV
		100 to 1100 MHz	50	-	150	mV
Rin	Input resistance	at 1 GHz	-	200	-	Ω
		at 100 MHz	-	600	-	Ω
Cin	Input Capacitance*		-	2	-	pF
R_{RF}	Division ratios		2048	-	262143	-
* Note: Cin in parallel with Rin						
Oscillator and reference divider (pins OSCin, OSCout)						
FOSC	Oscillator frequency range		3	-	16	MHz
VOSC(rms)	Input level sine wave		0.1	-	VCC + 2.8	Vrms
VOSC(p-p)	Input level square wave		0.3	-	VCC	Vpp
Z_{OSCout}	output impedance at OSCout pin		-	-	2	KΩ
R_{REF}	Reference division ratio	see table	128	-	1920	-
F_o	Output frequency range		5	-	100	KHz

CHARACTERISTICS (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit.
1/8 crystal frequency open collector output (pin FX8)						
I_{OL}	Current output low	$V_{OL} \geq 0.6$ V	1	-	-	mA
Phase comparator (pin PCD)						
F_{PCD}	Frequency range		5		100	KHz
I_{PCD}	Output current V_{PCD} = 2.5 V	Bit IPCD = 1	0.8	1	1.3	mA
		Bit IPCD = 0	0.4	0.5	0.7	mA
I_{PCDlk}	Output leakage current		-5	+/- 1	5	nA
V_{PCD}	Output voltage		0.4		V_{CP} -0.5	V
Serial clock input, serial data input (pins SDA, SCL)						
Fclk	clock frequency		0	-	100	KHz
VIH	input voltage high		3	-	-	V
VIL	input voltage low		-	-	1.5	V
IIH	input current high		-	3	10	µA
IIL	input current low		-10	-5	-	µA
CI	input capacitance		-	-	10	pF
IOL	SDA sink current	VOL = 0.4 V	-	-	3	mA
Slave address select input (pin SAA) hardware power down input (pin HPDN)						
VIH	input voltage high		3	-	-	V
VIL	input voltage low		-	-	0.4	V
IIH	input current high		-	-	0.1	µA
IIL	input current low		-10	-	-	µA
VCO output switches (pins VCOA, VCOB), synthesizer alarm (pin SYA)						
VOL	output voltage low	note 1	-	-	0.4	V
IOL	sink current low		400	-	-	µA

Note : 1. The pin VCOA is forced to zero state during out-of-lock



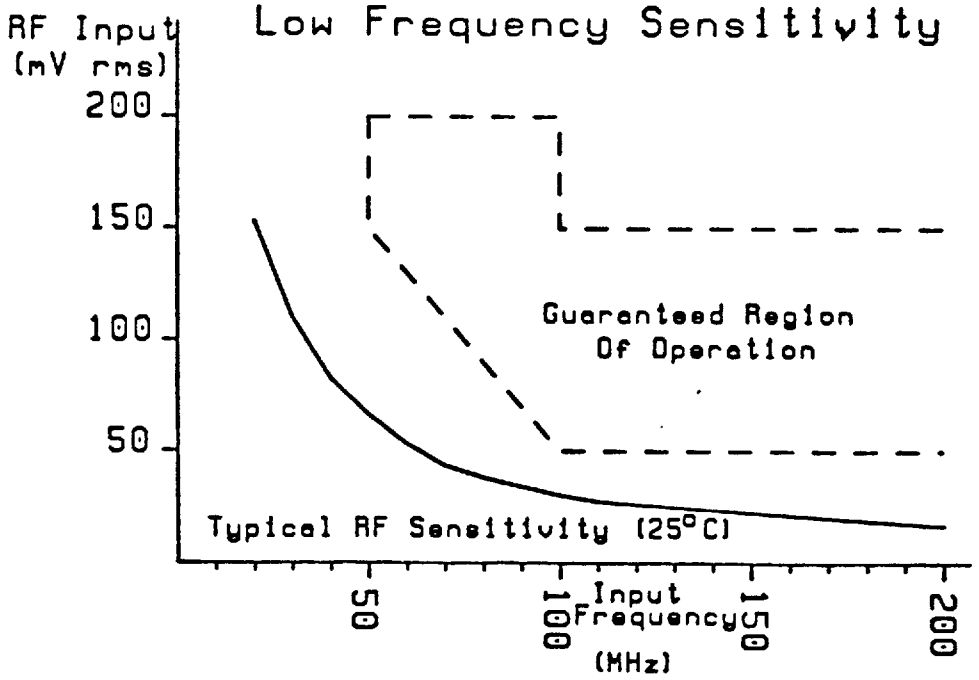
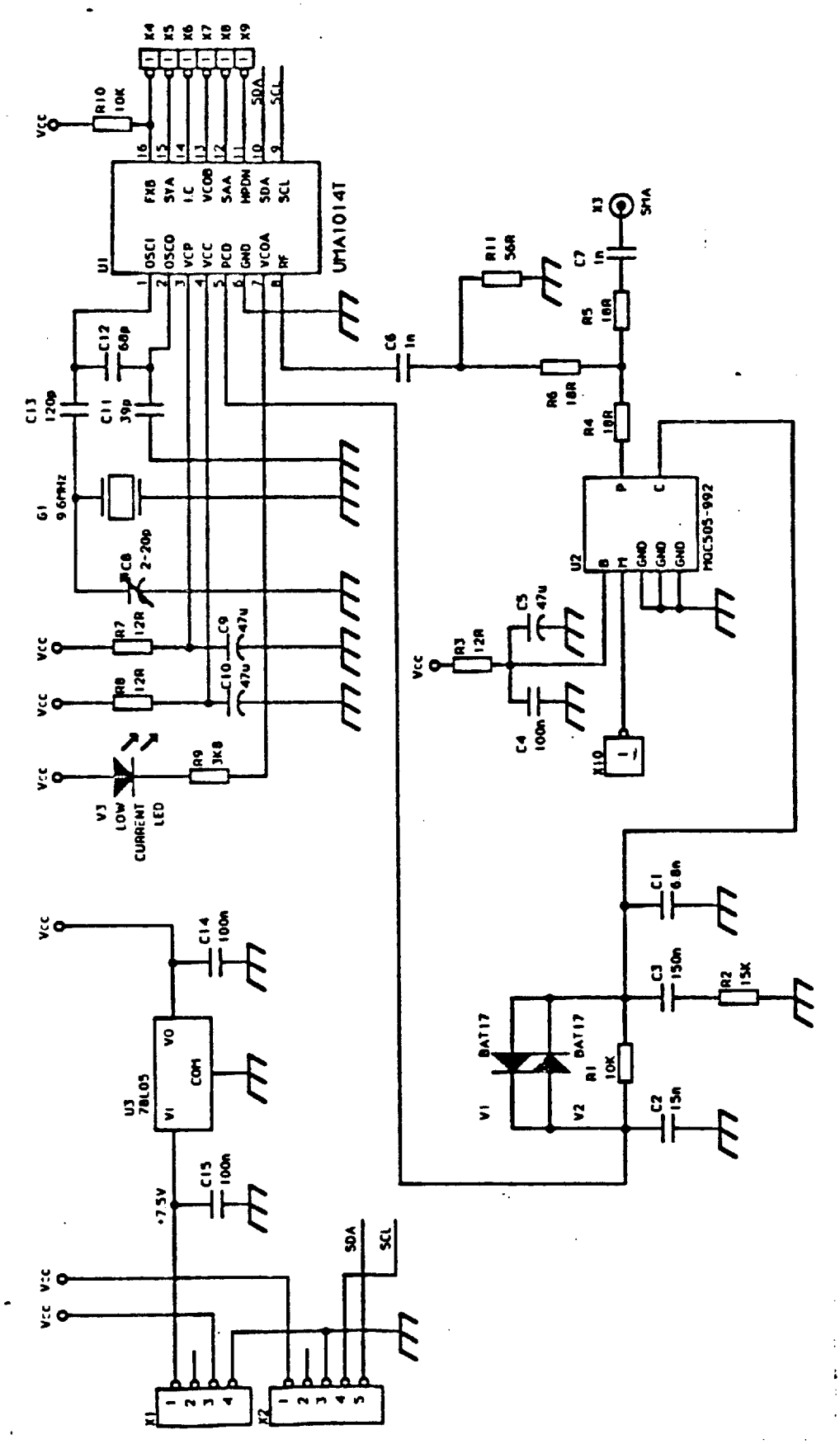


FIG. 6 RF Input Sensitivity


UMA1014T
MOC505-992
78L05
BAT17
BAT17
LOW CURRENT LED
SDA
SCL
Vcc
9.6MHz
+7.5V