- **Pin and functional compatibility with the industry standard 8237/8237A**
- **Fully static, high speed - 10, 8 and 5 MHz versions available**
- **Low power CMOS implementation**
- **TTL input/output compatibility**
- **Compatible with 8080/85, 8086/88, 80286/386 and 68000 μP families**
- **Fully static**
- **Four independent maskable DMA channels with autoinitialize capability**
- **Memory-to-memory transfer**
- **Fixed or rotating DMA request priority**
- **Independent polarity control for DREQ and DACK signals**
- **Address increment or decrement selection**
- **Cascadable to any number of channels**

The CA82C37A is a high performance, programmable Direct Memory Access (DMA) controller offering pin-for-pin functional compatibility with industry standard 8237/8237A. It features four channels, each independently programmable, and is cascadable to any number of channels. Each channel can be programmed to auto-initialize following DMA termination.

In addition, the CA82C37A supports memory-to-memory transfer capability and memory block initialization, as well as a programmable transfer mode.

The CA82C37A is designed to improve system performance by allowing external devices to transfer data directly from the system memory. High speed and very low power consumption make it an ideal component for aerospace and defence applications. The low power consumption also makes it an attractive addition in portable systems, or systems with low power standby modes.

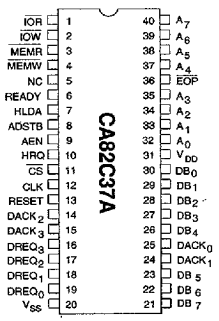

Figure 2-1: PDIP Pin Configurations

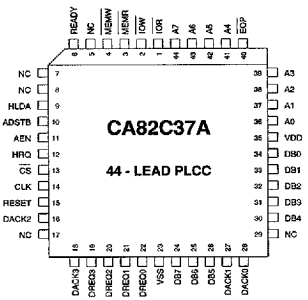

Figure 2-2: PLCC Pin Configurations

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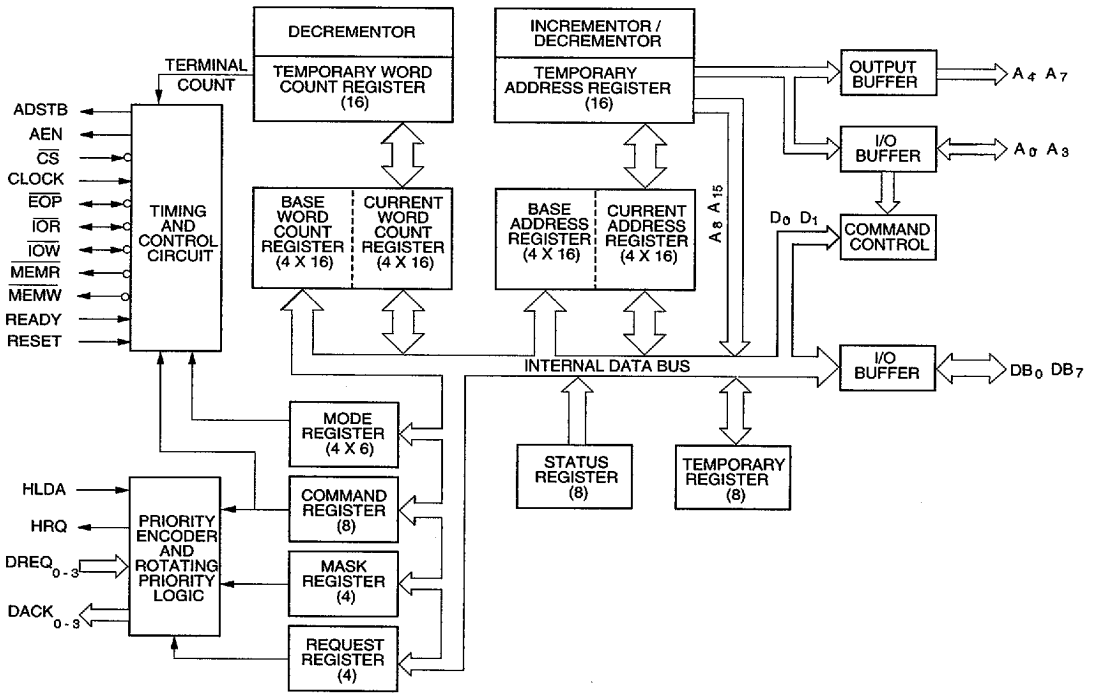

Figure 2-3: CA82C37A Block Diagram

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Table 2-1: Pin Descriptions

Symbol	Pins		Type	Name and Function
	PLCC	PDIP		
A_{0-3}	36-39	32-35	I/O	**Low Address Bus**: Bi-directional, 3-state signals. The 4 least significant address lines. Idle Cycle (Inputs). Addresses the CA82C37A control register to be loaded or read. Active Cycle (Outputs). Lower 4 bits of the transfer address.
A_{4-7}	41-44	37-40	O	**High Address Bus**: 3-state output signals. The 4 most significant address lines representing the upper 4 bits of the transfer address. Enabled during DMA service only.
ADSTB	10	8	O	**Address Strobe**: Active HIGH output signal to control latching of the upper address byte. Drives the strobe input of external transparent octal latches. During block operations, ADSTB is activated only if the upper address byte needs updating, eliminating S1 states and accelerating operation.
AEN	11	9	O	**Address Enable**: Active HIGH output signal to enable the 8-bit latch containing the higher order address byte onto the system address bus. During DMA transfers, it can disable other system bus drivers.
CLK	14	12	I	**Clock Input**: Generates timing signals to control internal operations and data transfer rate. Input can be driven from DC to maximum frequency. CLK may be stopped in Active or Idle Cycle for standby operation.
$\overline{CS}$	13	11	I	**Chip Select**: Active LOW input signal to select the CA82C37A as an I/O device (Idle Cycle) for CPU communication on the data bus.
$DACK_{0-3}$	28, 27, 16, 18	14, 15, 24, 25	O	**DMA Acknowledge**: Individual channel active LOW (RESET) or HIGH (programmable) output lines. Informs a peripheral that the requested DMA transfer has been granted.
DB_{0-7}	34-30 26-24	21-23 26-30	I/O	**Data Bus**: Bi-directional tri-state data lines connected to the system data bus. Idle Cycle. During I/O Read (Program condition), outputs are enabled and contents of CA82C37A internal registers are read by the CPU. In I/O Write, outputs are disabled and data from the data bus are written into the registers. Active Cycle. The upper byte of the transfer address is output to the data bus during DMA I/O device to-memory transfers. In memory-to-memory transfers, data is read into the CA82C37A Temporary Register from data bus inputs during the read-from-memory transfer, and written to the new memory location by data bus outputs during the write-to-memory transfer.
$DREQ_{0-3}$	19, 20, 21, 22	16, 17, 18, 19	I	**DMA Request**: Asynchronous DMA service request input lines from I/O devices. DMA service is requested by activation of the channel from a specific device. DREQ must be maintained until DACK (service acknowledge) is activated. I/O Device Priority. Order of service is programmable.Priority may be Fixed (descending order from Channel 0) or Rotating (Most recent channel served gets the lowest priority).

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Table 2-1: Pin Descriptions Cont'd

Symbol	Pins		Type	Name and Function
	PLCC	PDIP		
$\overline{EOP}$	40	36	I/O	**End of Process**: Active LOW bi-directional 3-state signal. The CA82C37A terminates DMA service when $\overline{EOP}$ is activated. Internal $\overline{EOP}$ (Output). $\overline{EOP}$ is activated when the word count for any channel turns over from 0000(H) to FFFF(H) and a TC pulse is generated. In memory-to-memory transfers, service is terminated when TC for channel 1 occurs. External $\overline{EOP}$ (Input). An external $\overline{EOP}$ signal pulling $\overline{EOP}$ low terminates active DMA service. An $\overline{EOP}$ signal also resets the DMA request. If auto-initialize is enabled, the base registers are written to the current registers of the channel. If the channel is not programmed for auto-initialize, the mask bit (Mask Register) and TC bit (Status Register) are set for the currently active channel. The mask bit is not changed if the channel is set for autoinitialize. Since $\overline{EOP}$ is driven by an open drain transistor on-chip, it should be maintained HIGH with a pull-up resistor in order to avoid erroneous $\overline{EOP}$ inputs.
HLDA	9	7	I	**Hold Acknowledge**: Active HIGH input signal to the CPU following an HRQ. Notifies the CA82C37A that the CPU has released control of the system buses.
HRQ	12	10	O	**Hold Request**: Active HIGH out put signal to the CPU. Requests control of the system buses. HRQ is issued following a request for DMA service (DREQ) from a peripheral, and is acknowledged by the HLDA signal.
$\overline{IOR}$	2	2	I/O	**I/O Read**: Active LOW bi-directional, 3-state signal. Idle Cycle. CPU input control signal for reading the Control Registers. Active Cycle. Output control signal to read data from a peripheral device during a DMA cycle.
$\overline{IOW}$	2	2	I/O	**I/O Write**: Active LOW bi-directional, 3-state signal. Idle Cycle. CPU input control signal for loading information into the CA82C37A. Active Cycle. Output control signal to load data to a peripheral device during a DMA cycle.
$\overline{MEMR}$	3	3	O	**Memory Read**: Active LOW 3-state output signal. CA82C37A reads data from a selected memory address during a DMA Read or Memory-to-Memory transfer.
$\overline{MEMW}$	4	4	O	**Memory Write**: Active LOW 3-state output signal. CA82C37A writes data to a selected memory address during a DMA Write or Memory-to-Memory transfer.
READY	6	6	I	**Ready**: A LOW Ready signal extends the Memory Read and Write pulse widths from the CA82C37A to accommodate slow I/O peripherals or memories. Transitions must not be made during the specified setup/hold time.
RESET	15	13	I	**Reset**: Active HIGH asynchronous input signal. Clears the Command, Status, Request and Temporary Registers, the Mode Register Counter and the First/Last Flip-Flop. The Mask Register is set to ignore DMA requests. The CA82C37A is in Idle Cycle following Reset.
V_{DD}	35	31	-	**Power**: 5 V ± 10% DC Supply.
V_{SS}	23	20	-	**Ground**: 0 V

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FUNCTIONAL DESCRIPTION

The CA82C37A DMA controller is a state-driven address and control signal generator designed to accelerate data transfer in systems by moving data from an I/O device to memory, or a block memory to an I/O device. Data transfers are direct, rather than being stored enroute in a temporary register.

The CA82C37A also mediates memory-to-memory block transfers and will move data from a single location to a memory block. Temporary storage of data is required, but the transfer rate is significantly faster than CPU processes. The device provides operating modes to carry out both single byte and block transfers of data. An operational flowchart of the CA82C37A is shown in Figure 2-4.

The organization of the CA82C37A is shown in the block diagram. It is composed of three logic blocks, a series of internal registers and a counter section. The logic blocks include the Timing Control, Command Control and Priority Encoder circuits.

The Timing Control block generates internal timing signals from the clock input and produces external control signals.

Command Control decodes incoming instructions from the CPU, and the Priority Encoder block regulates DMA channel priority.

The internal registers hold internal states and instructions from the CPU. Addresses and word counts are computed in the counter section.

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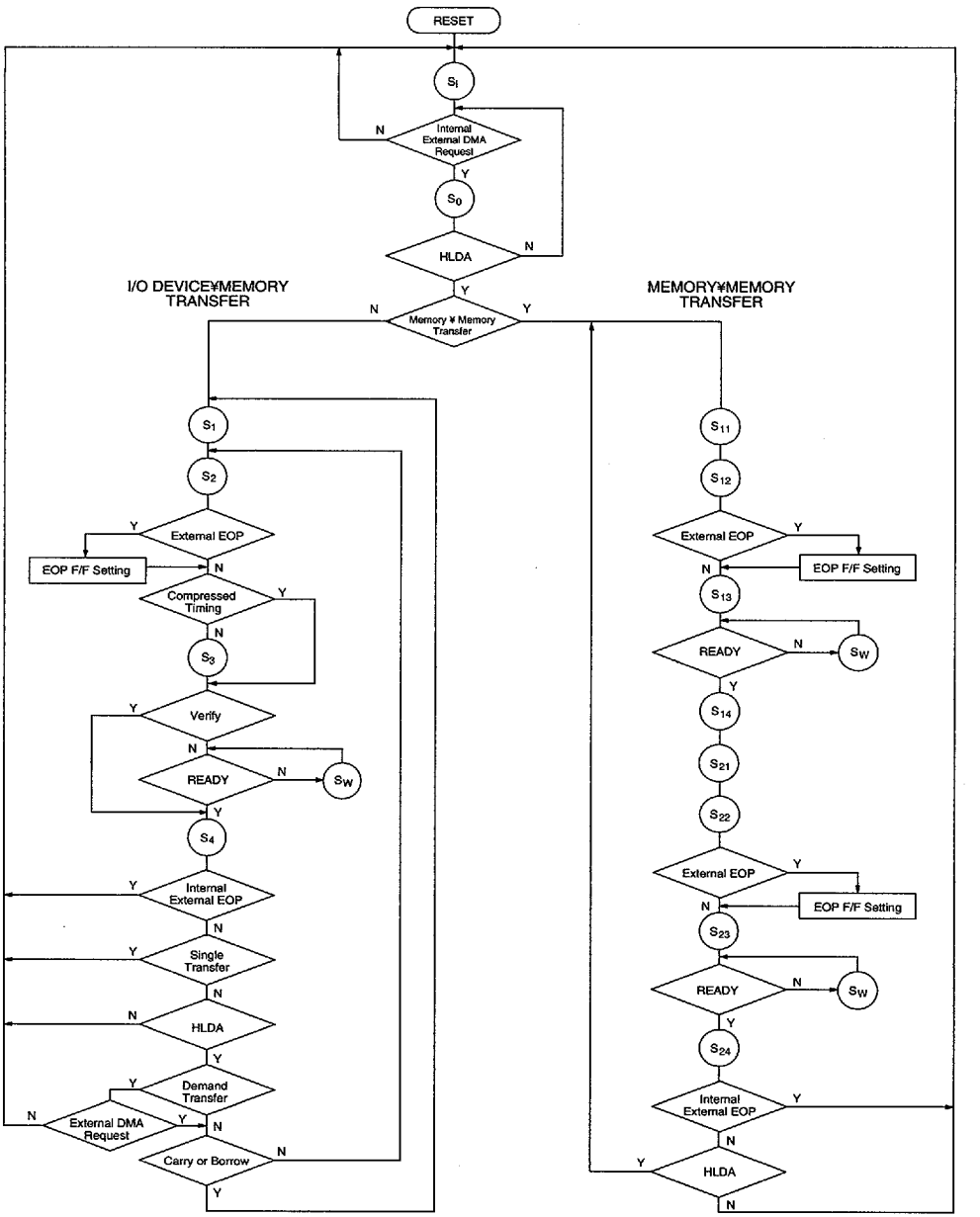

Figure 2-4: Operational Flowchart

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Table 2-2: AC Characteristics, DMA (Master) Mode (T_A = -40° to +85°C, V_{DD} = 5V ±10%, V_{SS} = 0V)

Symbol	Parameter	Limits (5 MHz)		Limits (8 MHz)		Limits (10 MHz)		Units
		Min	Max	Min	Max	Min	Max	
t_{AEL}	AEN HIGH from CLK LOW (S_1) Delay Time	-	175	-	105	-	90	ns
t_{AET}	AEN LOW from CLK HIGH (S_1) Delay Time	-	130	-	80	-	80	ns
t_{AFAB}	ADR Active to Float Delay from CLK HIGH	-	90	-	55	-	55	ns
t_{AFC}	$\overline{READ}$ or $\overline{WRITW}$ Float Delay from CLK HIGH	-	120	-	75	-	75	ns
t_{AFDB}	DB Active to Float Delay from CLOCK HIGH	-	170	-	135	-	100	ns
t_{AHR}	ADR from $\overline{READ}$ HIGH Hold Time	t_{CY} - 100	-	t_{CY} - 75	-	t_{CY} - 75	-	ns
t_{AHS}	DB from ADSTB LOW Hold Time (see Note 1)	30	-	25	-	20	-	ns
t_{AHW}	ADR from $\overline{WRITE}$ HIGH Hold Time	t_{CY} - 50	-	t_{CY} - 50	-	t_{CY} - 50	-	ns
t_{AK}	DACK Valid from CLK LOW Delay Time	-	170	-	105	-	90	ns
	$\overline{EOP}$ HIGH from CLK HIGH Delay Time	-	170	-	105	-	90	ns
	$\overline{EOP}$ LOW from CLK HIGH Delay Time	-	100	-	60	-	60	ns
t_{ASM}	ADR Stable from CLK HIGH	-	110	-	90	-	80	ns
t_{ASS}	DB to ADSTB LOW Setup Time	100	-	85	-	50	-	ns
t_{CH}	CLK HIGH Time (Transitions 10 ns)	70	-	55	-	45	-	ns
t_{CL}	CLK LOW Time (Transitions 10 ns)	70	-	55	-	40	-	ns
t_{CY}	CLK Cycle Time	200	-	125	-	100	-	ns
t_{DCL}	CLK HIGH to $\overline{READ}$ or $\overline{WRITE}$ LOW Delay	-	190	-	120	-	90	ns
t_{DCTR}	$\overline{READ}$ HIGH from CLK HIGH (S_4) Delay Time	-	190	-	115	-	95	ns
t_{DCTW}	WRITE HIGH from CLK HIGH (S_4) Delay Time	-	130	-	80	-	80	ns
t_{DO1}	HRQ Valid from CLK HIGH Delay Time	-	120	-	75	-	75	ns
t_{DO2}	HRQ Valid from CLK HIGH Delay Time	-	120	-	75	-	75	ns
t_{EPS}	$\overline{EOP}$ LOW from CLK LOW Setup Time	40	-	25	-	25	-	ns
t_{EPW}	$\overline{EOP}$ Pulse Width	220	-	135	-	80	-	ns

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Table 2-2: AC Characteristics, DMA (Master) Mode (T_A = -40° to +85°C, V_{DD} = 5V ±10%, V_{SS} = 0V) Cont'd

Symbol	Parameter	Limits (5 MHz)		Limits (8 MHz)		Limits (10 MHz)		Units
		Min	Max	Min	Max	Min	Max	
t_{FAAB}	ADR Float to Active Delay from CLK HIGH	-	110	-	90	-	80	ns
t_{FAC}	$\overline{READ}$ or $\overline{WRITE}$ Active from CLK HIGH	-	150	-	90	-	90	ns
t_{FADB}	DB Float to Active Delay from CLK HIGH	-	110	-	90	-	80	ns
t_{HS}	HLDA Valid to CLK HIGH Setup Time	75	-	45	-	45	-	ns
t_{IDH}	Input Data from $\overline{MEMR}$ HIGH Hold Time	0	-	0	-	0	-	ns
t_{IDS}	Input Data to $\overline{MEMR}$ HIGH Setup Time	155	-	90	-	80	-	ns
t_{ODH}	Output Data from $\overline{MEMW}$ HIGH Hold Time	15	-	15	-	15	-	ns
t_{ODV}	Output Data Valid to $\overline{MEMW}$ HIGH	125	-	85	-	65	-	ns
t_{QS}	DREQ to CLK LOW (S_1, S_4) Setup Time	0	-	0	-	0	-	ns
t_{RH}	CLK to READY LOW Hold Time	20	-	20	-	10	-	ns
t_{RS}	READY to CLK LOW Setup Time	60	-	35	-	35	-	ns
t_{STL}	ADSTB HIGH from CLK HIGH Delay Time	-	80	-	50	-	50	ns
t_{STT}	ADSTB LOW from CLK HIGH Delay Time	-	90	-	90	-	90	ns

Note 1: t_{AHS} = 20 ns minimum for industrial temperature range devices.

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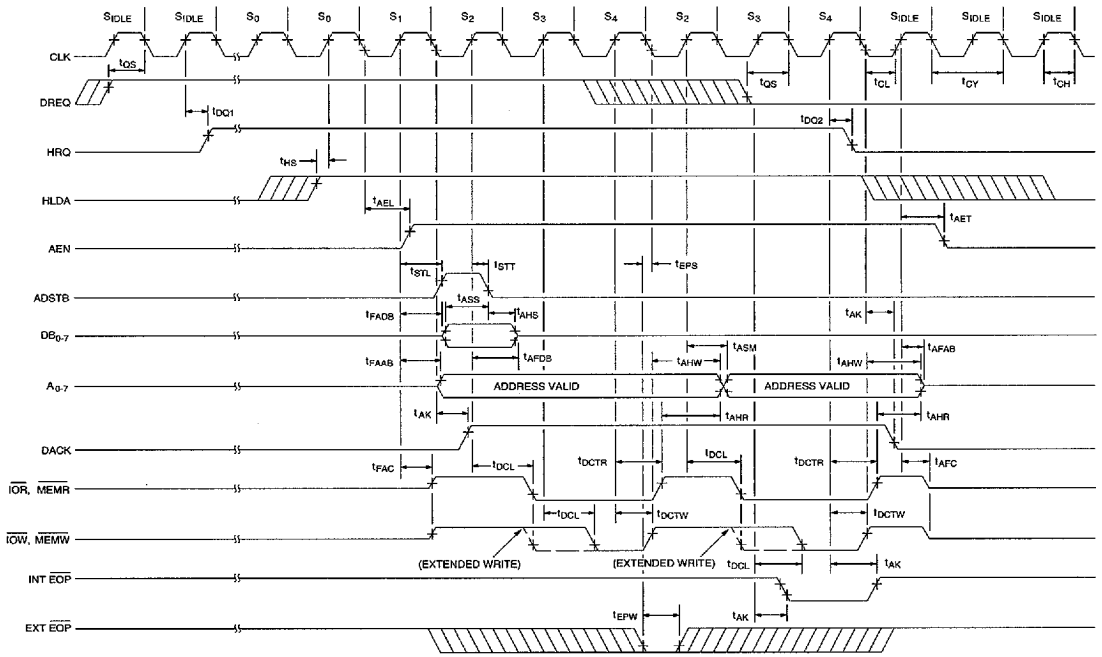
Figure 2-5: Timing Diagrams (Master Mode)

a) DMA Transfer Timing



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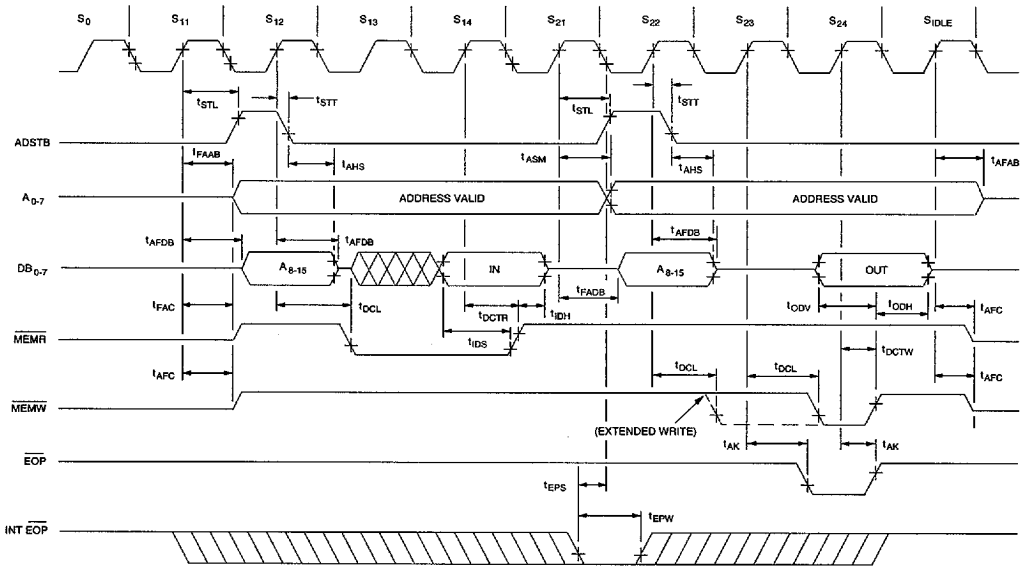
b) Memory-to-Memory Transfer Timing



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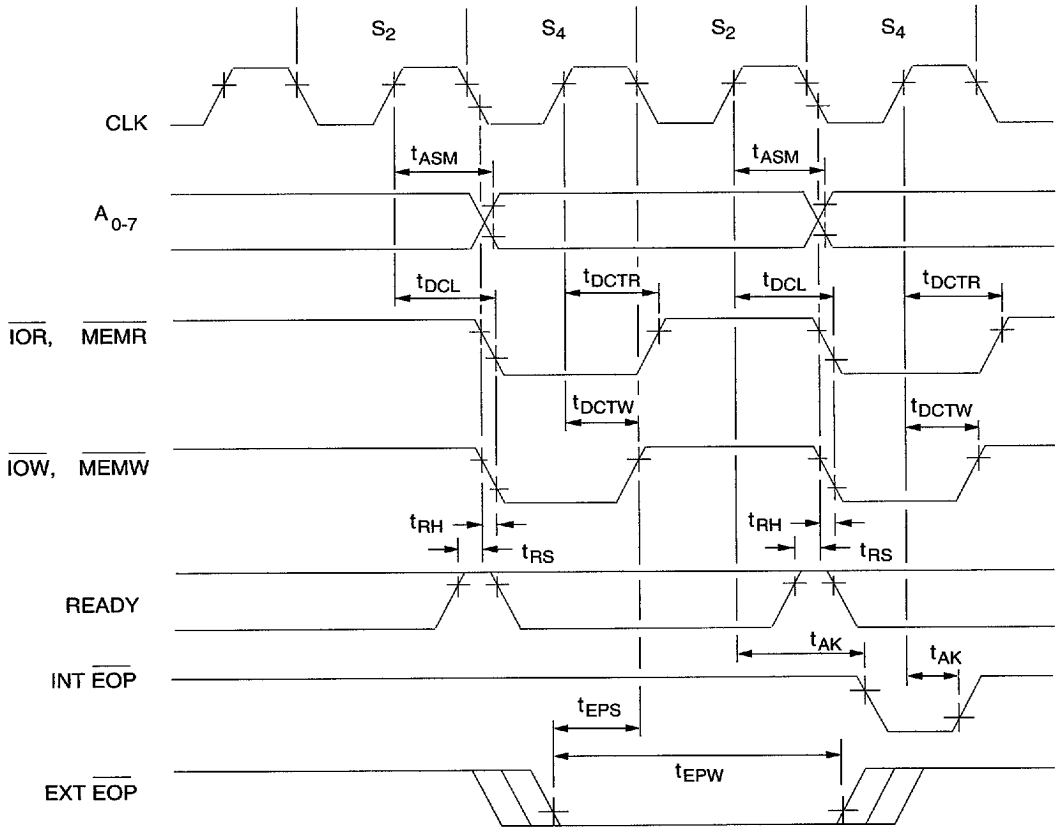
c) **Compressed Transfer Timing**



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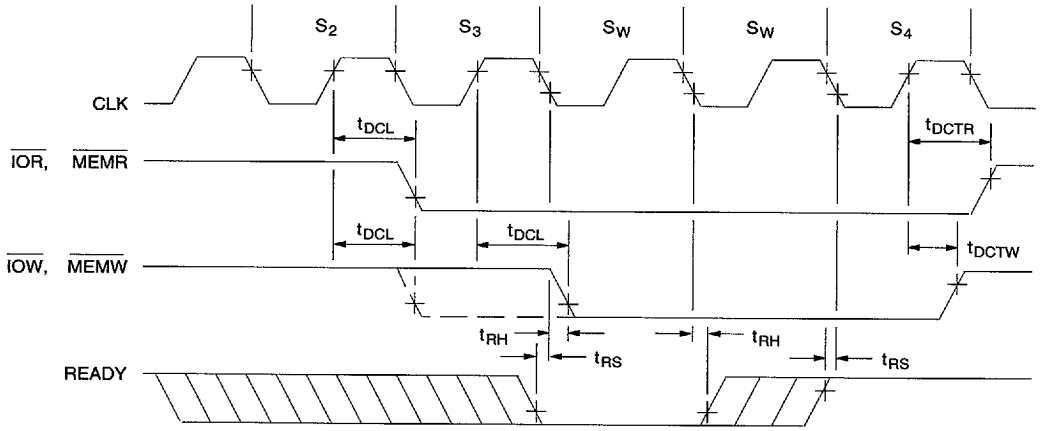
d) Ready Timing



e) Reset Timing

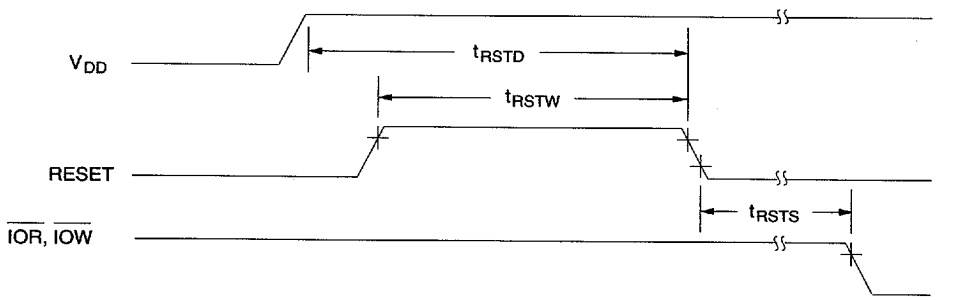


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Table 2-3: AC Characteristics, Peripheral (Slave) Mode (T_A = -40° to +85°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Limits (5 MHz)		Limits (8 MHz)		Limits (10 MHz)		Units
		Min	Max	Min	Max	Min	Max	
t_{AR}	ADR Valid or $\overline{CS}$ LOW to $\overline{READ}$ LOW	10	-	10	-	0	-	ns
t_{AW}	ADR Valid to $\overline{WRITE}$ HIGH Setup Time	130	-	90	-	60	-	ns
t_{CW}	$\overline{CS}$ LOW to $\overline{WRITE}$ HIGH Setup Time	130	-	100	-	85	-	ns
t_{DW}	Data Valid to $\overline{WRITE}$ HIGH Setup Time	130	-	90	-	60	-	ns
t_{RA}	ADR or CS Hold from $\overline{READ}$ HIGH	0	-	0	-	0	-	ns
t_{RDE}	Data Access from $\overline{READ}$	-	140	-	120	-	110	ns
t_{RDF}	DB Float Delay from $\overline{READ}$ HIGH	0	70	0	70	0	70	ns
t_{RSTD}	Pwr Supply HIGH to RESET LOW Setup Time	500	-	500	-	500	-	ns
t_{RSTS}	Reset to First $\overline{IOWR}$	$2 \cdot t_{CY}$	-	$2 \cdot t_{CY}$	-	$2 \cdot t_{CY}$	-	ns
t_{RSTW}	RESET Pulse Width	300	-	200	-	100	-	ns
t_{RW}	$\overline{READ}$ Width	200	-	155	-	120	-	ns
t_{WA}	ADR from $\overline{WRITE}$ HIGH Hold Time	0	-	0	-	0	-	ns
t_{WC}	CS HIGH from $\overline{WRITE}$ HIGH Hold Time	0	-	0	-	0	-	ns
t_{WD}	Data from $\overline{WRITE}$ HIGH Hold Time	10	-	10	-	10	-	ns
t_{WWS}	$\overline{WRITE}$ Width	150	-	100	-	90	-	ns

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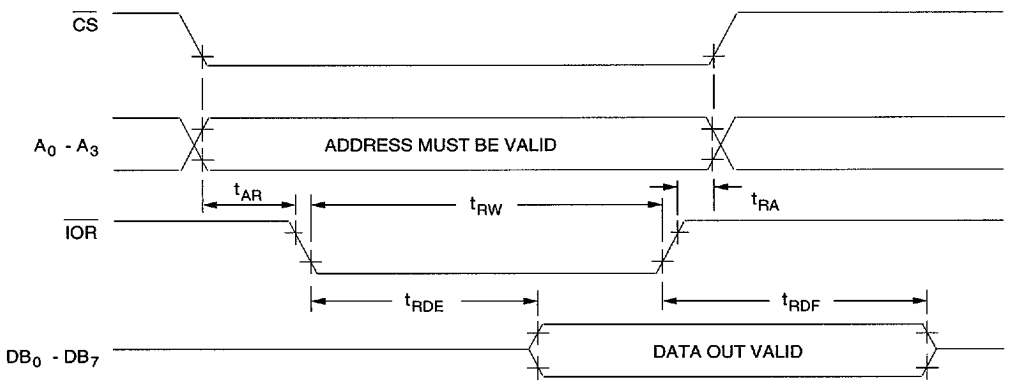
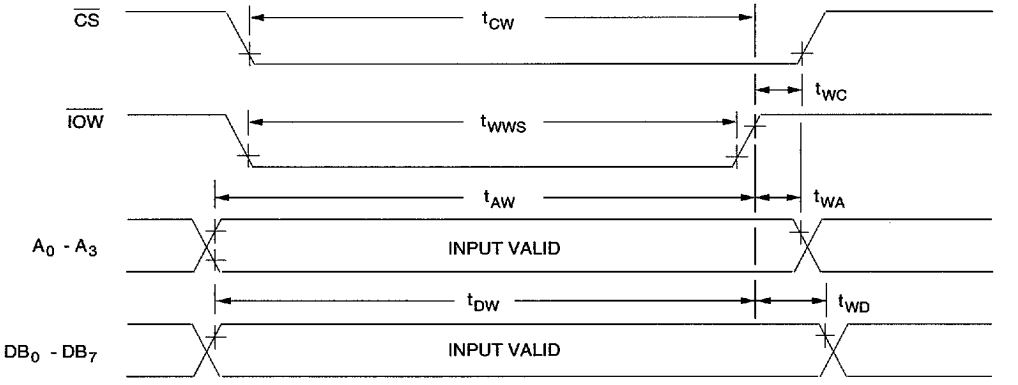
Figure 2-6: Timing Diagrams (Slave Mode)

a) Slave Mode Read Timing



b) Slave Mode Write Timing



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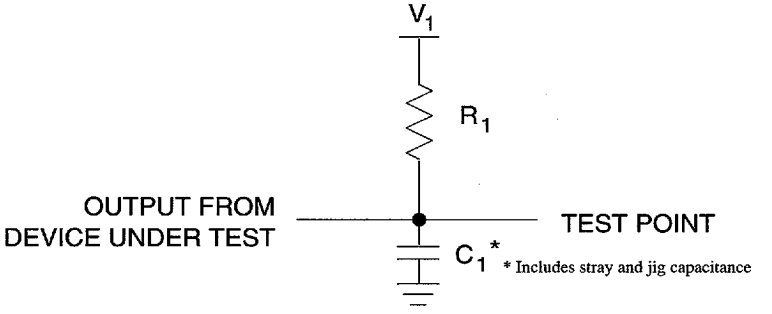

Pins	V_1	R_1	C_1
All Outputs Except $\overline{EOP}$	1.7 V	520	100 pF
$\overline{EOP}$	VDD	1.6 k	50 pF

Figure 2-7: AC Test Circuits

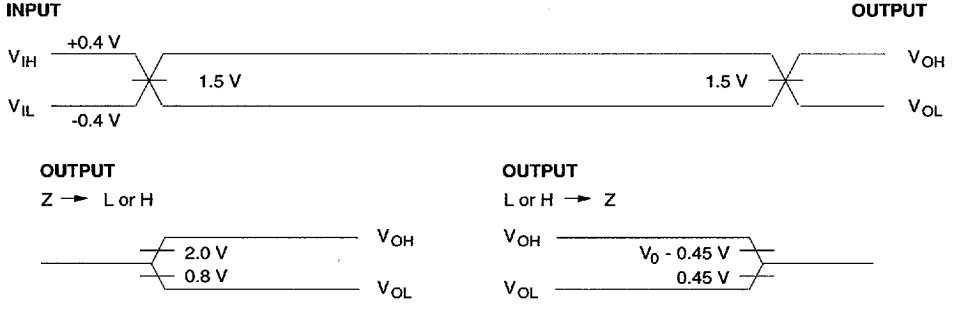

Figure 2-8: AC Testing Input, Output Waveforms

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Table 2-4: DC Characteristics (T_A = -40° to +85°C, except as noted, V_{DD}=+5 V ±10%, V_{SS}=0V)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{DDOP}	Operating Power Supply Current	V_{DD} = 5.5 V V_{IN} = V_{DD} or V_{SS} Outputs Open	-	2.0	mA/ mHz
I_{IL}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-1.0	+1.0	µA
I_{OL}	Output Leakage Current	0 V ≤ V_{OUT} ≤ V_{DD}	-10.0	+10.0	µA
V_{IH}	Input High Voltage	Note 8	2.0	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	Note 8	-0.3	0.8	V
V_{IHS}	Schmitt Trigger Input High Voltage	Note 9	2.1	V_{DD} + 0.3	V
V_{ILS}	Schmitt Trigger Input Low Voltage	Note 9	-0.3	0.7	V
V_{HY}	Schmitt Trigger Hysteresis	Note 9	-	0.4	V
V_{OH}	Output High Voltage	IOH = -2.5 mA IOH = -100 µA	2.4 VDD - 0.4	- -	V V
V_{OL}	Output Low Voltage	IOL = +3.2 mA	-	0.4	V

Notes:

1. *Input timing parameters assume rise and fall transition times of 20 ns or less.*
2. *The net $\overline{IOW}$ or $\overline{MEMW}$ pulse width for a normal write will be t_{CY} - 100 ns, and for an extended write will be 2•t_{CY} - 100 ns. The net IOR or MEMR pulse width for a normal read will be 2•t_{CY} - 50 ns and for a compressed read will be t_{CY} - 50 ns.*
3. *DREQ should be held active until DACK is returned.*
4. *DREQ and DACK signals may be active HIGH or active LOW. The timing diagrams assume active HIGH.*
5. *Successive read and/or write operations by the external processor to program or examine the controller must be timed to allow at least 100 ns (CA82C37A-10) and 200 ns (CA82C37A-5) as recovery time between active read or write pulses.*
6. *$\overline{EOP}$ is an open drain output, and requires a pullup resistor to V_{DD}.*
7. *Pin 5 can be either tied to V_{DD}, or left unconnected.*
8. *Applies to pins $\overline{IOR}$, $\overline{IOW}$, DB_{7-0}, A_{3-0} and $\overline{EOP}$*
9. *Applies to pins READY, HLDA, CLK, $\overline{CS}$, RESET and $DREQ_{3-0}$*

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Table 2-5: Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0V, V_{IN} = +5 V or V_{SS})

Symbol	Parameter	Test Conditions	Min	Max	Units
$C_{I/O}$	I/O Capacitance	FREQ = 1 MHz Unmeasured pins returned to V_{SS}	-	15	pF
C_{IN}	Input Capacitance		-	10	pF
C_{OUT}	Output Capacitance		-	10	pF

Table 2-6: Recommended Operating Conditions

DC Supply Voltage		+4.5 V to +5.5 V
Operating Temperature Range	Commercial	0°C to +70°C
	Industrial	-40°C to +85°C

Table 2-7: Absolute Maximum Ratings

DC Supply Voltage	-.03 to +7.0 V
Input, Output or I/O Voltage Applied	V_{SS} - 0.3 V to V_{DD} + 0.3 V
Storage Temperature Range	-55°C to +150°C
Maximum Package Power Dissipation	1 W
Input Pin Current (@ 25°C)	-10.0 mA to +10.0 mA
Lead Temperature (soldering: 10 sec.)	300°C

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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INTERNAL REGISTERS

The CA82C37A contains 27 registers that are used internally for control and temporary data storage. These registers are listed in Table 2-8 below, and described in the subsections following.

Table 2-8: Internal Registers

Name	Number	Size
Base Address Registers	4	16-bit
Base Word Count Registers	4	16-bit
Command Register	1	8-bit
Current Address Registers	4	16-bit
Current Word Count registers	4	16-bit
Mask Register	1	4-bit
Mode Registers	4	6-bit
Request Register	1	4-bit
Status Register	1	8-bit
Temporary Address Register	1	16-bit
Temporary Register	1	8-bit
Temporary Word Count Register	1	16-bit

Base Address and Base Word Count Registers

Each of the four (4) channels has a pair of Base Address and Base Word Count Registers. These 16-bit registers store the original value of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values.

The base registers are written simultaneously with their corresponding current register (in 8-bit bytes) by the microprocessor when in the Program Condition. These registers cannot be read by the microprocessor.

Command Register

The operation of the CA82C37A is controlled by the 8-bit Command Register. It is programmed by the microprocessor and is cleared by a Reset or a Master Clear instruction.

Figure 2-9 lists the function of the command bits, while Table 2-12 contains the Read and Write addresses.

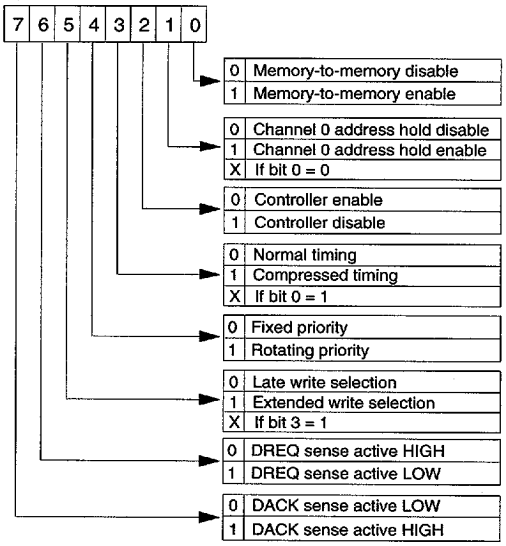

Figure 2-9: Command Register

Current Address Register

Each of the channels has a 16-bit Current Address Register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer, with the values of the address stored in the Current Address Register during the transfer.

This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized (by an Auto-initialize) back to its original value, where an Auto-initialize takes place only after an $\overline{EOP}$.

In memory-to-memory mode, the channel 0 Current Address Register can be prevented from incrementing or decrementing by setting the address hold bit in the Command Register.

Current Word Register

Each of the channels also has a 16-bit Current Word Count register which is used to determine the number of transferso be performed. The actual number of transfers is one more than the number programmed in the Current Word Count

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register (i.e. programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer, and when the value in the register goes from zero to FFFFH, a terminal count (TC) is generated.

This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. Following the end of a DMA service it may also be reinitialized by an Autoinitialize back to its original value. Again, Auto-initialization can occur only after an $\overline{EOP}$. If not Auto-initialized, this register will have a count of FFFFH after TC.

Mask Register

Each of the channels has associated with it one mask bit in the 4-bit Mask register which can be set to disable an incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$ if the channel is not programmed to Autoinitialize. The Mask Register bit for each channel can be set or cleared either individually or simultaneously as a group under software control.

To set and reset the mask bits for all channels at once, refer to the Write All Mask Bits command in Table 2-12, and to Figure 2-10.

The entire register can also be set by a Reset or Master Clear. This disables all hardware DMA requests until a clear Mask register instruction allows them to occur. The instruction to individually set or clear single mask bits is similar in form to that used with the Request register. Refer to the Figure 2-11 and to Write Single Mask Bit command in Table 2-12 for details.

In reading the Mask Register, bits 4-7 will always read as logical ones, and bits 0-3 will display the mask bits of channel 0-3, respectively. The 4 bits of the Mask Register may be cleared simultaneously by using the Clear Mask Register command (see Table 2-12).

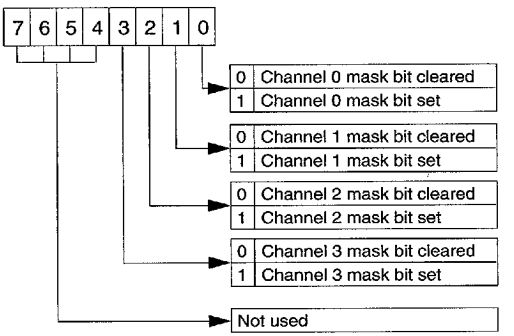

Figure 2-10: Mask Register (Write Operation)

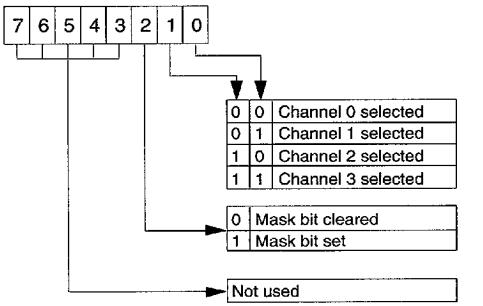

Figure 2-11: Mask Register (Set/Reset

Mode Register

Each of the channels has a 6-bit mode register associated with it. When this register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode Register is to be written. When the processor reads a Mode Register, bits 0 and 1 are both ones. See Figure 2-12 and Table 2-12 for Mode Register functions and addresses.

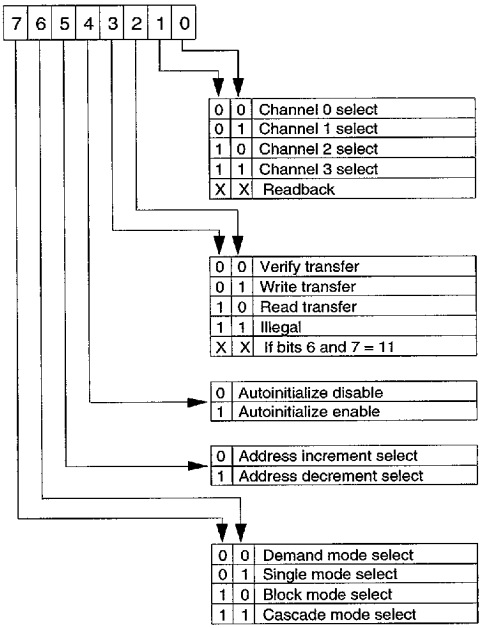

Figure 2-12: Mode Register

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Request Register

The CA82C37A responds to requests for DMA service initiated by the software and by a DREQ. Each channel has a non-maskable request bit associated with it in the 4-bit Request Register. These are subject to prioritization by the priority Encoder network with each bit set or reset separately under software control. To set/reset a bit, the software loads the proper form of the data word. The entire register is cleared by a Reset. See Table 2-12 for register address coding, and Figure 2-13 for Request Register format.

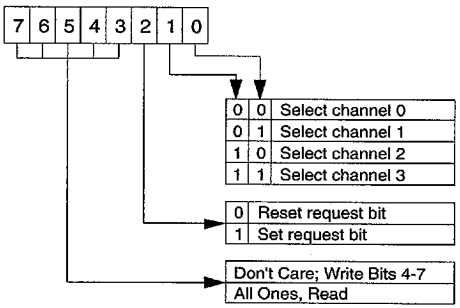

Figure 2-13: Request Register

A software request for DMA operation can be made in block or single modes. For memory-to-memory transfers, the software request for channel 0 should be set. When reading the request register, bits 4-7 will always read as ones, and bits 0-3 will display the request bits of channels 0-3 respectively.

Status Register

The CA82C37A Status Register can be read by the microprocessor. It contains information about which channels have reached a terminal count and which channels have pending DMA requests.

Bits 0-3 are set every time a TC is reached by that channel or an external $\overline{EOP}$ is applied. Theses bits are cleared upon Reset, Master Clear and on each Status Read.

Bits 4-7 are set whenever their corresponding channel is requesting service, regardless of the mask bit state. If the mask bits are set, software can poll the status register to determine which channels have DREQs, and selectively clear a mask bit, thus allowing user defined service priority. Status bits 4-7 are updated while the clock is high, and latched on the falling edge. Status bits 4-7 are cleared upon Reset or Master Clear.

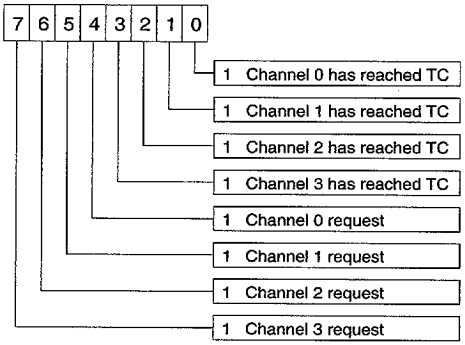

Figure 2-14: Status Register

Temporary Register

The Temporary Register is used to hold data during memory-to-memory transfers. When the transfers are completed, the last word moved can be read by the microprocessor.

Note that the Temporary Register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset or Master Clear.

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OPERATIONAL DESCRIPTION

DMA Operation

In a system, the CA82C37A address and control outputs and data bus pins are usually connected in parallel with the system buses with an external latch required for the upper address byte. When inactive, the controller's outputs are in a high impedance state. When activated by a DMA request (and bus control has been relinquished by the host), the CA82C37A drives the buses and generates the control signals to perform the data transfer. The operation performed by activating one of the four DMA request inputs has previously been programmed into the controller via the command, mode, address, and word count registers.

For example, if a block of data is to be transferred from RAM to an I/O device, the starting address of the data is loaded into the CA82C37A Current and Base Address Registers for a particular channel, and the length of the block is loaded into that channel's Word Count Register. The corresponding Mode Register is programmed for a memory-to-I/O operation (read transfer) with various options selected by the Command Register and other Mode Register bits. The channel's mask bit is cleared to enable recognition of a DMA request (DREQ), where the DREQ can be generated by a hardware signal or by a software command.

Once initiated, the block DMA transfer proceeds as the controller outputs the data address, simultaneous $\overline{MEMR}$ and $\overline{IOW}$ pulses, then selects an I/O device via the DMA acknowledge (DACK) outputs. The data byte flows directly from the RAM to the I/O device. After each byte is transferred, the address is automatically incremented (or decremented) and the word count is decremented. The operation is then repeated for the next byte. The controller stops transferring data when the word count register underflows, or an external $\overline{EOP}$ is applied.

To better understand CA82C37A operation, consider the states generated by each clock cycle. The DMA controller operates in two major cycles, active and idle. After being programmed, the controller is normally idle until a DMA request occurs on an unmasked channel, or a software request is given. The CA82C37A then requests control of the system buses and enters the active cycle. The active cycle is composed of several internal states, depending on the options that have been selected and the type of operation that has been requested.

When performing I/O-to-memory or memory-to-I/O DMA the CA82C37A can enter seven distinct states, each composed of one full clock period. State 1 (S_{idle}) is the idle state. It is entered when the CA82C37A has no valid DMA requests pending, at the end of a transfer sequence, or when a Reset or Master Clear occurs. While in S_{idle}, the DMA controller is inactive, though it may be in the process of being programmed by the processor (Program Condition).

State 0 (S0) is the first state of a DMA service. The CA82C37A has requested a hold but the processor has not yet returned an acknowledge. The CA82C37A may still be programmed until it has received HLDA from the CPU. An acknowledge from the CPU will signal that DMA transfers may begin. S1, S2, S3, and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted between S2 or S3 and S4 by the use of the Ready line on the CA82C37A.

Note that the data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active at the same time. The data is neither read into nor driven out of the CA82C37A in I/O-to-memory or memory-to-I/O transfers.

The CA82C37A can enter eight distinct states when performing memory-to-memory DMA, each composed of one full clock period. Four states are required for the read-from-memory step, and four for the write-to-memory operations. Data bytes in transit are stored briefly in the Temporary Register.

Table 2-9: Memory-to-Memory Transfer States

Transfer States	State Numbers	Notes
Read-from-Memory	S11, S12, S13, S14	Memory-to-Memory transfers require 8 states for a single transfer, 4 states for the Read-to-Memory half, and 4 Write-to-Memory states to complete the transfer.
Write-to-Memory	S21, S22, S23, S24	

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Idle Cycle

When none of the channels is requesting service, the CA82C37A enters the Idle cycle and performs Sidle states. In this cycle, the CA82C37A samples the DREQ lines on the falling edge of every clock cycle to determine if any channel is requesting a DMA service.

Note that DMA requests will be ignored in standby operation where the clock has been stopped. The device will respond to a $\overline{CS}$ (chip select), in case of an attempt by the micro-processor to write or read the internal registers of the CA82C37A. When $\overline{CS}$ is low and HLDA is low, the CA82C37A enters the Program Condition. The CPU can then establish, change or inspect the internal definition of the part by reading or writing the internal registers.

The CA82C37A may be programmed with the clock stopped, provided HLDA is low and at least one rising clock edge occurred after HLDA was driven low, so the controller is in a S_{idle} state. Address lines A_0 - A_3 are inputs to the device and select which registers are read or written. The $\overline{IOR}$ and $\overline{IOW}$ lines are used to select and time the read or write operations.

Due to the number and size of the internal registers, an internal flip-flop is used to generate an additional address bit. This bit is used to determine the upper or lower byte of the 16-bit Address and Word Count registers. The flip-flop is reset by a Master Clear or Reset. Separate software commands can also set or reset this flip-flop.

Special software commands can be executed by the CA82C37A in the Program Condition. These commands are decoded as sets of addresses with $\overline{CS}$, $\overline{IOR}$, and $\overline{IOW}$, and do not make use of the data bus. The commands include: Set and Clear First/Last Flip-Flop, Master Clear, Clear Mode Register Counter, and Clear Mask Register.

Active Cycle

When the CA82C37A is in the Idle cycle, and a software request or an unmasked channel requests a DMA service, the device outputs an HRQ to the micro-processor and enters the Active cycle. It is in this cycle that the DMA service will take place, in one of the four modes described below:

Single Transfer Mode

In single transfer Mode, the device is programmed to make one transfer only. The word count is decremented and the address decremented or incremented following each transfer. When the word count rolls over from zero to FFFFH, a terminal count bit in the Status Register is set, an $\overline{EOP}$ pulse is generated, and the channel autoinitializes if this option has been selected. If not programmed to Autoinitialize, the mask bit is set, along with the TC bit and $\overline{EOP}$ pulse.

DREQ must be held active until DACK becomes active. If DREQ is held active throughout the single transfer, HRQ goes inactive and releases the bus to the system. It again goes active and, upon receipt of a new HLDA, another single transfer is performed, unless a higher priority channel takes over. In 8080A, 8085A, or 8088/86 systems, this ensures one full machine cycle execution between DMA transfers. Details of the timing between the CA82C37A and other bus control protocols depends upon the characteristics of the microprocessor involved.

Block Transfer Mode

In Block Transfer Mode, the CA82C37A is activated by DREQ or software request and continues making data transfers during the service until a TC, caused by word count going to FFFFH, or an external End of Process ($\overline{EOP}$) is encountered. DREQ need only be held active until DACK becomes active. Again, Autoinitialization occurs at the end of the service if the channel has been programmed for that option.

Demand Transfer Mode

In Demand Transfer Mode the CA82C37A continues making transfers until a TC or an external $\overline{EOP}$ is encountered, or until DREQ goes inactive. Thus, transfers continue until the I/O device has exhausted its data capacity. When the I/O device has caught up, DMA service is re-established by means of a DREQ. In the interim between services when the microprocessor is allowed to operate, the intermediate values of address and word count are stored in the CA82C37A Current Address and Current Word Count Registers.

Higher priority channels may intervene in the demand process, once DREQ has gone inactive. Only an EOP can cause an Autoinitialization at the end of the service. The EOP is generated either by TC or by an external signal.

Cascade Mode

This mode is used to cascade more than one CA82C37A for simple system expansion. The HRQ and HLDA signals from additional CA82C37A devices are connected, respectively, to the DREQ and DACK signals of a channel in the initial CA82C37A. This allows the DMA requests of the additional devices to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel of the initial CA82C37A is used only for setting the priority of additional devices, it does not output an address or control signals of its own. These could conflict with the outputs of the active channel in the extra devices.

The CA82C37A will respond to DREQ and generate DACK but all other outputs except HRQ will be disabled. An external EOP will be ignored by the initial device, but will have the usual effect on the added device.

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Figure 2-15 shows two additional devices cascaded with an initial device and using two of the initial device's channels. This forms a two-level DMA system. More CA82C37As could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices, forming a third level.

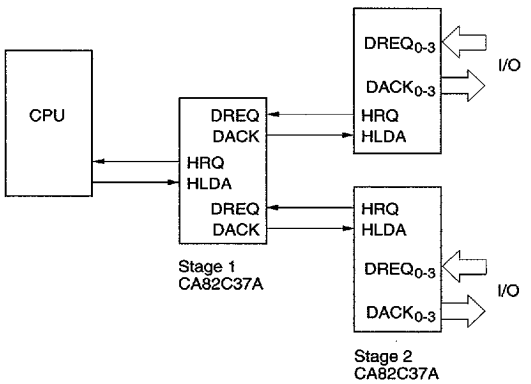

Figure 2-15: Cascaded CA82C37As

When programming cascaded controllers, start with the first level device (the one closest to the microprocessor). After Reset, the DACK outputs are programmed to be active low and are held in the high state. If they are used to drive HLDA directly, the second level device(s) cannot be programmed until DACK polarity is selected as active high on the initial device. In addition, the initial device's mask bits function normally on cascaded channels, so they may be used to inhibit second-level services.

Transfer Types

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from an I/O device to the memory by activating $\overline{\text{MEMW}}$ and $\overline{\text{IOR}}$. Read transfers move data from memory to an I/O device by activating $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$ (refer to Table 2-10).

Verify transfers are pseudo-transfers. The CA82C37A operates like Read or Write transfers, generating addresses and responding to $\overline{\text{EOP}}$, etc., however the memory and I/O control lines all remain inactive. Verify mode is not allowed for memory-to-memory operation. Note that Ready is ignored during verify transfers.

Table 2-10: I/O Memory Transfer States *

Operational State	Description	Notes
S1	AEN High Low Order Bits: A_0 - A_7 High Order Bits: DB_0 - DB_7 ADSTB High DACK Active	S1 state is omitted if there is no change in the 8 high order bit transfer address during demand and block mode transfers.
S2	$\overline{\text{IOR}}$ Low or $\overline{\text{MEMR}}$ goes Low	S2 state (and S3) are I/O or memory I/O timing control states
S3	$\overline{\text{IOW}}$ Low or $\overline{\text{MEMW}}$ goes Low	S3 is omitted when compressed timing is used.
S4	$\overline{\text{IOR}}$ High $\overline{\text{IOW}}$ High $\overline{\text{MEMR}}$ High $\overline{\text{MEMW}}$ High Word count register decremented by 1 Address register incremented (or decremented) by 1	S4 state completes the DMA transfer of one word.

* In I/O memory transfers, data is transferred directly without being handled by the CA82C37A.

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Auto-initialize

By programming a bit in the Mode Register, a channel may be set up as an Auto-initialize channel. During Auto-initialization, the original values of the Current Address and Current Word Count Registers are automatically restored from the Base Address and Base Word Count Registers of that channel following $\overline{EOP}$. The base registers are loaded at the same time as the current registers by the micro-processor and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in Autoinitialize. Following Auto-initialization, the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected, or a software request is made.

Memory-to-Memory

The CA82C37A incorporates a memory-to-memory transfer feature, to perform block moves of data from one memory address space to another with minimum of program effort and time. Programming bit 0 in the Command Register selects channels 0 and 1 to operate as memory-to-memory transfer channels.

The transfer is initiated by setting the software or hardware DREQ for channel 0. The CA82C37A requests a DMA service in the normal manner. When HLDA goes high, the device, using four-state transfers in Block Transfer mode, reads data from the memory. The channel 0 Current Address register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the CA82C37A internal Temporary Register. Another four-state transfer moves the data to memory using the address in the channel 1 Current Address register. The Current Address is incremented or decremented in the normal manner, and the channel 1 Current Word Count is decremented.

When the word count of channel 1 goes to FFFFH, a TC is generated, causing an $\overline{EOP}$ output which terminates the service. When Channel 0 word count decrements to FFFFH the channel 0 TC bit in the Status Register is not set nor is an $\overline{EOP}$ generated in this mode. However, channel 0 is Auto-initialized, if that option has been selected.

If full Auto-initialization for a memory-to-memory operation is desired, the channel 0 and channel 1 word counts must be set to the same value before the transfer begins. Otherwise, should channel 0 underflow before channel 1, it Auto-initializes and sets the data source address back to the beginning of the block. Should the channel 1 word count underflow before channel 0, the memory-to-memory DMA service terminates, and channel 1 Auto-initializes but not channel 0.

In memory-to-memory mode, Channel 0 may be programmed to retain the same address for all transfers, allowing a single byte to be written to an entire block of memory. This channel 0 address hold feature is selected by bit 1 in the Command Register.

The CA82C37A responds to external $\overline{EOP}$ signals during memory-to-memory transfers, but only relinquishes the system buses after the transfer is complete (i.e. after an S24 state). Data comparators in block search schemes may use this input to terminate the service when a match is found. The timing of memory-to-memory transfers is found in Figure 2-5b. Memory-to-memory operations can be detected as an active AEN with no DACK outputs.

Priority

The CA82C37A has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon their descending numerical value. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0. After a channel has been recognized for service, remaining channels are prevented from interfering with the service until it is completed.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotated accordingly. The next lower channel from the channel serviced has highest priority on the following request. Priority rotates every time control of the system buses is returned to the CPU.

Table 2-11: Priority Decision Modes

Priority Mode		Fixed	Rotating			
Service Terminated Channel		-	CH_0	CH_1	CH_2	CH_3
Order of priority or next DMA	Highest	CH_0	CH_1	CH_2	CH_3	CH_0
		CH_1	CH_2	CH_3	CH_0	CH_1
		CH_2	CH_3	CH_0	CH_1	CH_2
	Lowest	CH_3	CH_0	CH_1	CH_2	CH_3

With rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. Thus any one channel is prevented from monopolizing the system.

Note that regardless of which priority scheme is chosen, priority is evaluated every time a HLDA is returned to the CA82C37A.

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Compressed Timing

In order to achieve even greater throughput where system characteristics permit, the CA82C37A can compress the transfer time to two clock cycles. From Figure 2-5a it can be seen that state S3 is used to extend the access time of the read pulse. By removing state S3, the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 states will still occur when

A8 - A15 need updating (see Address Generation). Timing for compressed transfers is found in Figure 2-5c. $\overline{EOP}$ will be output in S2 if compressed timing is selected.

Compressed timing is not allowed for memory-to-memory transfers.

Address Generation

In order to reduce the pin count, the CA82C37A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. Lower order address bits are output by the CA82C37A directly. Lines A_0 - A_7 should be connected to the address bus. The timing diagram of Figure 2-5a shows the time relationships between CLK, AEN, ADSTB, DB_0 - DB_7 and A_0 - A_7.

During Block and Demand Transfer mode service, which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A_7 to A_8 takes place in the normal sequence of addresses. To save time and speed transfers, the CA82C37A executes the S1 states only when updating of A_8 - A_{15} in the latch is necessary. This means for long services, S1 states and ADSTB may occur only once every 256 transfers, a saving of 255 clock cycles for each 256 transfers.

External EOP Operation

The $\overline{EOP}$ pin is bidirectional and open drain, and can be driven by external signals to terminate DMA operation. It is important to note that the CA82C37A will not accept external $\overline{EOP}$ signals when it is in an S_{idle} state. The controller must be active to latch external $\overline{EOP}$. Once latched, the external $\overline{EOP}$ will be acted upon during the next S2 state, unless the CA82C37A enters an idle state first. In the latter case, the latched $\overline{EOP}$ is cleared. External $\overline{EOP}$ pulses that occur between active DMA transfers in demand mode are not recognized, since the CA82C37A is in an S1 state.

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PROGRAMMING

The CA82C37A accepts programming from the host processor any time that HLDA is inactive, and at least one rising clock edge has occurred after HLDA has gone low. It is necessary for the host processor to ensure that programming and HLDA are mutually exclusive. Note that a problem can occur if a DMA request occurs on an unmasked channel while the CA82C37A is being programmed. For example: where the CPU is starting to reprogram the two byte Address Register of channel 1 when channel 1 receives a DMA request: if the CA82C37A is enabled (bit 2 in the Command Register is set to 0), and channel 1 is unmasked, then a DMA service will occur after only one byte of the Address Register has been reprogrammed. This condition can be avoided by disabling the controller (bit 2 in the Command Register is set to 1) or masking the channel before programming any of its registers. Once the programming is complete, the controller can be enabled or the channel unmasked.

It is highly recommended that after power-up all internal locations be loaded with some known value, even if some channels are unused.

Table 2-12: Software Command and Register Codes

Operation	A_3	A_2	A_1	A_0	$\overline{IOR}$	$\overline{IOW}$
Read Status Register	1	0	0	0	0	1
Write Command Register	1	0	0	0	1	0
Read Request Register	1	0	0	1	0	1
Write Request Register	1	0	0	1	1	0
Read Command Register	1	0	1	0	0	1
Write Single Bit Mask	1	0	1	0	1	0
Read Mode Register	1	0	1	1	0	1
Write Mode Register	1	0	1	1	1	0
Set Byte Pointer F/F	1	1	0	0	0	1
Clear Byte Pointer F/F	1	1	0	0	1	0
Read Temporary Register	1	1	0	1	0	1
Master Clear	1	1	0	1	1	0
Clear Mode Register Counter	1	1	1	0	0	1
Clear Mask Register	1	1	1	0	1	0
Read All Mask Bits	1	1	1	1	0	1
Write All Mask Bits	1	1	1	1	1	0

Software Commands

There are several special software commands which can be executed by reading or writing to the CA82C37A. These commands do not depend on the specific data pattern on the data bus, but are activated by the I/O operation itself. Note that on read type commands, the data value is not guaranteed.

The CA82C37A software commands are summarized below:

Clear First/Last Flip-Flop

This command is executed prior to writing or reading new address or word count information to the CA82C37A. It initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor address upper and lower bytes in the correct sequence.

Set First/Last Flip-Flop

This command sets the flip-flop to first select the high byte on read and write operations to Address and Word Count Registers.

Master Clear

This software command has the same effect as the hardware Reset. The Command, Status, Request, and Temporary Registers, and the Internal First/Last Flip-Flop and Mode Register counter are cleared and the Mask Register is set. The device then enters the Idle cycle.

Clear Mask Register

This command clears the mask bits of all four channels, enabling them to accept DMA requests.

Clear Mode Register Counter

Since only one address location is available for reading Mode Registers, an internal two-bit counter is included to select Mode Registers during read operations.

To read the Mode Registers, first execute the Clear Mode Register Counter command, then do consecutive reads until the desired channel is read. Read order is channel 0 first, channel 3 last. The lower two bits on all Mode Registers will read as ones.

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Table 2-13: Word Count and Address Register Command Codes

Channel	Register	Operation	Signals							Internal Flip-Flop	Data Bus DB_0 - DB_7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A_3	A_2	A_1	A_0		
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A_0 - A_7
			0	1	0	0	0	0	0	1	A_8 - A_{15}
	Current Address	Read	0	0	1	0	0	0	0	0	A_0 - A_7
			0	0	1	0	0	0	0	1	A_8 - A_{15}
	Base and Current Word Count	Write	0	1	0	0	0	0	1	0	W_0 - W_7
			0	1	0	0	0	0	1	1	W_8 - W_{15}
	Current Word Count	Read	0	0	1	0	0	0	1	0	W_0 - W_7
			0	0	1	0	0	0	1	1	W_8 - W_{15}
1	Base and Current Address	Write	0	1	0	0	0	1	0	0	A_0 - A_7
			0	1	0	0	0	1	0	1	A_8 - A_{15}
	Current Address	Read	0	0	1	0	0	1	0	0	A_0 - A_7
			0	0	1	0	0	1	0	1	A_8 - A_{15}
	Base and Current Word Count	Write	0	1	0	0	0	1	1	0	W_0 - W_7
			0	1	0	0	0	1	1	1	W_8 - W_{15}
	Current Word Count	Read	0	0	1	0	0	1	1	0	W_0 - W_7
			0	0	1	0	0	1	1	1	W_8 - W_{15}
2	Base and Current Address	Write	0	1	0	0	1	0	0	0	A_0 - A_7
			0	1	0	0	1	0	0	1	A_8 - A_{15}
	Current Address	Read	0	0	1	0	1	0	0	0	A_0 - A_7
			0	0	1	0	1	0	0	1	A_8 - A_{15}
	Base and Current Word Count	Write	0	1	0	0	1	0	1	0	W_0 - W_7
			0	1	0	0	1	0	1	1	W_8 - W_{15}
	Current Word Count	Read	0	0	1	0	1	0	1	0	W_0 - W_7
			0	0	1	0	1	0	1	1	W_8 - W_{15}
3	Base and Current Address	Write	0	1	0	0	1	1	0	0	A_0 - A_7
			0	1	0	0	1	1	0	1	A_8 - A_{15}
	Current Address	Read	0	0	1	0	1	1	0	0	A_0 - A_7
			0	0	1	0	1	1	0	1	A_8 - A_{15}
	Base and Current Word Count	Write	0	1	0	0	1	1	1	0	W_0 - W_7
			0	1	0	0	1	1	1	1	W_8 - W_{15}
	Current Word Count	Read	0	0	1	0	1	1	1	0	W_0 - W_7
			0	0	1	0	1	1	1	1	W_8-W_{15}

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APPLICATIONS

Figure 2-16 shows an application for a DMA system utilizing the CA82C37A DMA controller and an 80C88 microprocessor. The CA82C37A DMA controller is used here to improve system performance by allowing an I/O device to transfer data directly to, or from the system memory.

Components

The system clock is generated by the CA82C84A clock driver and is inverted to meet the clock high and low times required by the CA82C37A DMA controller. The four OR gates are used to support an 80C88 microprocessor in minimum mode by producing the control signals used by the processor to access memory or I/O. A decoder is used to generate the chip select for the DMA controller and memory.

Since the most significant bits of the address are output on the address/data bus, an 82C82 octal latch is used to demultiplex the address. Hold Acknowledge (HLDA) and Address Enable (AEN) are ORed together to insure that the DMA controller does not encounter bus contention with the microprocessor.

Operation

A DMA request (DREQ) is generated by the I/O device. After receiving the DMA request, the DMA controller issues a Hold Request (HRQ) to the microprocessor. The system buses are not released to the DMA controller until a Hold Acknowledge signal is returned to the DMA controller from the 80C88 processor. After the Hold Acknowledge has been received, addresses and control signals are generated by the DMA controller to accomplish the DMA transfers. Data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active. Recall that data is not read into or driven out of the DMA controller in I/O-to-memory or memory-to- I/O data transfers.

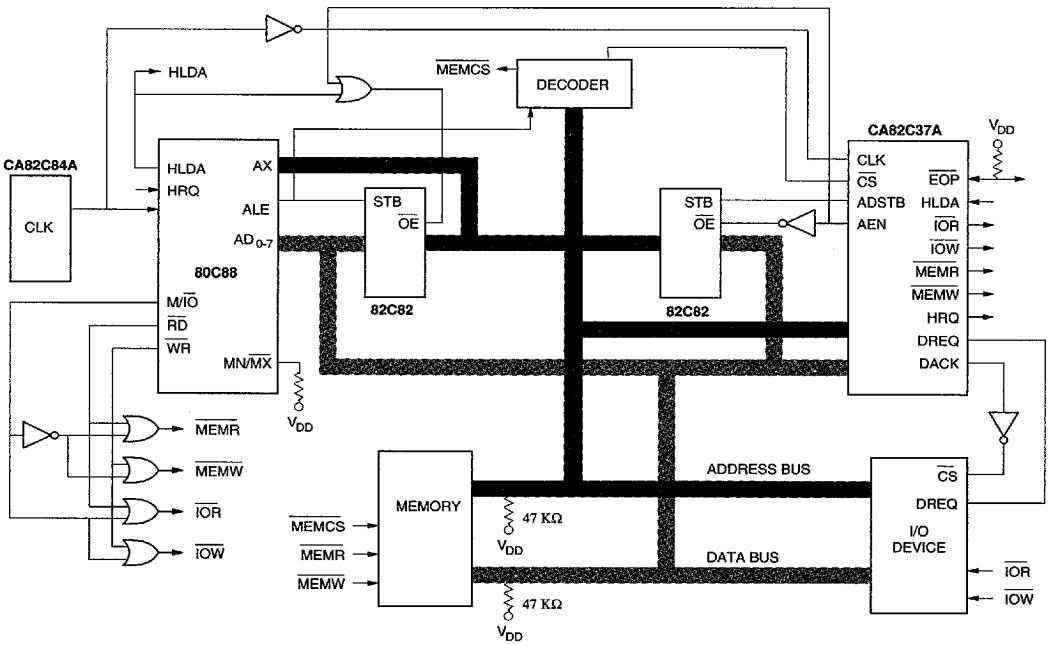

Figure 2-16: Application for DMA System

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