CALMOS™

CA82C88

MICROPROCESSOR BUS CONTROLLER

- **Pin and functional compatibility with the industry standard 8288**
- **Supports 8086/88 and 80186/188 µPs**
- **Very high speed - 8 and 5 MHz**
- **Low power CMOS implementation**
- **Bipolar drive capability**
- **TTL I/O compatibility**
- **3-state command output drivers**
- **Configurable for use with an I/O bus**
- **Facilitates interface to one or two multi-master buses**

The CA82C88 Bus Controller is a 20-pin CMOS component which includes command control timing generation as well as a bipolar bus drive capability while optimizing system performance. A strapping option on the bus controller configures it for use with a multi-master system bus and separate I/O bus.

The CA82C88 is a fully static device, and is designed to be used in high speed, medium-to-large 8088/86 microprocessor systems. Its high performance makes it ideally suited for aerospace and defense applications, where its very low power consumption makes it useful in portable systems and systems with low power standby modes.

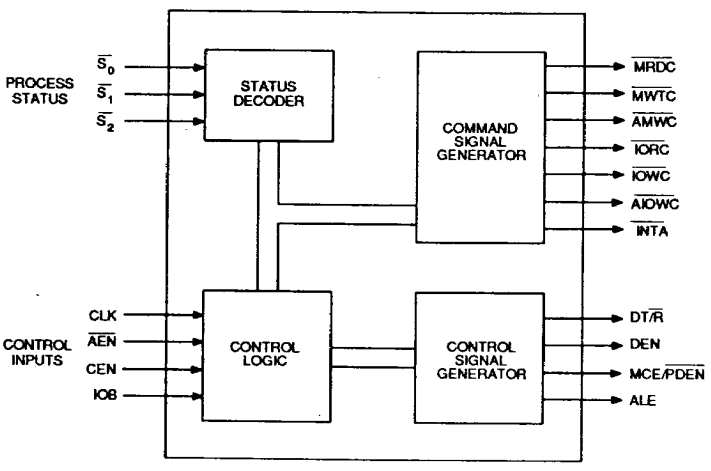

Figure 1 : CA82C88 BLOCK DIAGRAM

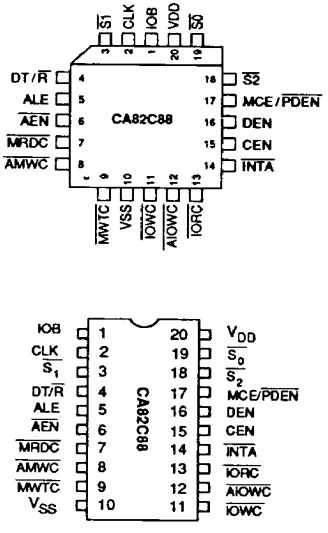

Figure 2 : PLCC and DIP PIN CONFIGURATIONS

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Table 1 : PIN DESCRIPTIONS

Symbol	Pin(s)		Type	Name and Function
	PLCC	PDIP		
$\overline{AEN}$	6	6	I	**Address Enable:** $\overline{AEN}$ enables the CA82C88 command outputs at least t_{AELCV} nanosec (Table 4) after it becomes active (LOW). When $\overline{AEN}$ goes inactive, the command output drivers are immediately 3-stated. $\overline{AEN}$ does not affect the I/O command lines if the CA82C88 is in the I/O Bus mode (IOB tied HIGH).
$\overline{AIOWC}$	12	12	O	**Advanced I/O Write Command:** The $\overline{AIOWC}$ issues an I/O Write Command earlier in the machine cycle to give I/O devices an early indication of a write instruction. Its timing is the same as a read command signal. This signal is active LOW.
ALE	5	5	O	**Address Latch Enable:** This signal serves to strobe an address into the address latches. It is active HIGH and latching occurs on the falling (HIGH to LOW) transition. ALE is intended for use with transparent D type latches.
$\overline{AMWC}$	8	8	O	**Advanced Memory Write Command:** This active LOW signal is used to issue a memory write command earlier in the machine cycle to give memory devices an early indication of a write instruction. Its timing is the same as a read command signal.
CEN	15	15	I	**Command Enable:** When LOW all CA82C88 command outputs, and the control outputs DEN and PDEN are forced to the inactive state. When HIGH, these outputs are enabled.
CLK	2	2	I	**Clock:** This clock signal from the CA82C84A clock generator is used to determine when command and control signals are generated.
DEN	16	16	O	**Data Enable:** This active HIGH signal enables data transceivers onto either the local or system data bus.
DT/$\overline{R}$	4	4	O	**Data Transmit/Receive:** This signal establishes the direction of data flow through the transceivers. HIGH indicates Transmit (write to I/O or memory), LOW indicates Receive (Read).
$\overline{INTA}$	14	14	O	**Interrupt Acknowledge:** This active LOW signal tells an interrupting device that its interrupt has been acknowledged and that it should drive vector information onto the data bus.
IOB	1	1	I	**Input/Output Bus Mode:** When IOB is strapped HIGH the CA82C88 functions in the I/O Bus mode. When strapped LOW, the CA82C88 functions in the System Bus mode. (See sections on I/O Bus and System Bus modes)
$\overline{IORC}$	13	13	O	**I/O Read Command:** This active LOW signal instructs an I/O device to drive its data onto the data bus.
$\overline{IOWC}$	11	11	O	**I/O Write Command:** This active LOW signal instructs an I/O device to read the data on the data bus.
MCE/$\overline{PDEN}$	17	17	O	**MCE (IOB is tied LOW):** Master Cascade Enable occurs during an interrupt sequence and serves to read a Cascade Address from a master PIC (Priority Interrupt Controller) onto the data bus. The MCE signal is active HIGH. $\overline{PDEN}$ *(IOB is tied HIGH):* Peripheral Data Enable enables the data bus transceiver for the I/O bus that DEN performs for the system bus. This signal is active LOW.
$\overline{MRDC}$	7	7	O	**Memory Read Command:** This active low signal instructs the memory to drive its data onto the data bus.
$\overline{MWTC}$	9	9	O	**Memory Write Command:** This active LOW signal instructs the memory to record the data present on the data bus.
$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$	19, 3, 18	19, 3, 18	I	**Status Input Pins:** These are status input pins from 8088/86/89 processors. The CA82C88 decodes these generate command and control signals at the appropriate time. These pins are HIGH when not in use. Active Bus Hold circuits hold these lines HIGH when no other driving source is present.
V_{DD}	20	20		**Power:** 5V ± 10% DC Supply
V_{SS}	10	10		**Ground:** 0V

FUNCTIONAL DESCRIPTION

Command and Control Logic

The CA82C88 decodes the status line signals ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$) common to the 8086/88/89 processors to determine what command is to be issued, (Table 2).

Table 2 : CA82C88 COMMANDS

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Processor State	8288 Command
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

Operating Modes

The CA82C88 can be operated in one of two modes, I/O Bus Mode or System Bus Mode according to the system hardware configuration.

I/O Bus Mode: (IOB strapped HIGH) In the I/O Bus (IOB) mode the I/O command lines ($\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$) are always enabled (not dependent on $\overline{AEN}$). When an I/O command is initiated by the processor, the CA82C88 immediately activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control the I/O bus transceiver. *Since no arbitration is present*, the I/O command lines should not be used to control the system bus in this mode. This mode allows one CA82C88 to handle two external buses. No waiting is involved when the CPU wants to gain access to the I/O bus. Normal memory access requires a *Bus Ready* signal ($\overline{AEN}$ LOW) before proceeding. The IOB mode is aimed at applications where I/O or peripherals dedicated to one processor exist in a multi-processor system.

System Bus Mode: (IOB strapped LOW) In this mode no commands are issued until t_{AELCV} ns (Table 4) after the $\overline{AEN}$ Line is activated (LOW). This mode assumes bus arbitration logic will inform the bus controller (on the $\overline{AEN}$ line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists, and both I/O and memory are shared by more than one processor.

Command Outputs

Advanced write commands prevent the processor from entering unnecessary wait states. They are available to initiate write procedures early in the machine cycle.

Table 3 : COMMAND OUTPUTS

$\overline{MRDC}$	Memory Read Command
$\overline{MWTC}$	Memory Write Command
$\overline{IORC}$	I/O Read Command
$\overline{IOWC}$	I/O Write Command
$\overline{AMWC}$	Advanced Memory Write Command
$\overline{AIOWC}$	Advanced I/O Write Command
$\overline{INTA}$	Interrupt Acknowledge

$\overline{INTA}$ (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. $\overline{INTA}$ informs an interrupting device that its interrupt is being acknowledged and that it should place service vector information on the data bus.

Control Outputs

CA82C88 control outputs include Data Enable (DEN), Data Transmit/Receive (DT/$\overline{R}$) and Master Cascade Enable/Peripheral Data Enable (MCE/$\overline{PDEN}$). DEN determines when the external bus should be enabled onto the local bus and DT/$\overline{R}$ determines the direction of data transfer. These two signals are usually connected to the transceiver *chip select* and *direction* pins.

MCE/$\overline{PDEN}$ alters its function with the operating mode. In the IOB mode, the $\overline{PDEN}$ signal serves as a dedicated data enable signal for the I/O or Peripheral System Bus.

In the System Bus Mode, MCE is used during interrupt acknowledge cycles. Two interrupt acknowledge cycles occur back to back during interrupt sequences, with no data or address transfers during the first cycle. Thus logic should be provided to mask off MCE. Just before the second cycle, MCE gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE strobes it into the address latches. On the leading edge of the second interrupt cycle, the addressed slave PIC gates an interrupt vector onto the system data bus where it is read by the processor.

If the system contains only one PIC, MCE is *not used* and the second Interrupt Acknowledge signal gates the interrupt vector onto the processor bus.

Address Latch Enable (ALE) and Halt

ALE occurs every machine cycle and strobes the current address into the address latches. ALE also strobes $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$ into a latch for halt state decoding.

Command Enable (CEN)

CEN is a command qualifier for the CA82C88. If CEN is HIGH, the CA82C88 functions normally, and all command lines are held in their inactive state (not 3-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus and resident bus devices.

Table 4 : AC CHARACTERISTICS (T_A = –40° to +85°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits (5MHz)		Limits (8MHz)		Units
			Min	Max	Min	Max	
t_{AEHCZ}	Command Disable Time	D (Note 2)	-	40	-	40	ns
t_{AELCH}	Command Enable Time	C (Note 1)	-	45	-	40	ns
t_{AELCV}	Enable Delay Time	B (Note 4)	85	250	85	250	ns
t_{AEVNV}	$\overline{AEN}$ to DEN	A	-	35	-	25	ns
t_{CELRH}	CEN to Command	B	-	t_{CLML}+20	-	t_{CLML}+10	ns
t_{CEVNV}	CEN to DEN, $\overline{PDEN}$	A	-	35	-	25	ns
t_{CHCL}	CLK High Time		65	-	40	-	ns
t_{CHDTH}	Direction Control Inactive Delay	A	-	35	-	30	ns
t_{CHDTL}	Direction Control Active Delay	A	-	50	-	50	ns
t_{CHLL}	ALE Inactive Delay	A (Note 3)	4	35	4	25	ns
t_{CHSV}	Status Inactive Hold Time		10	-	10	-	ns
t_{CLCH}	CLK Low Time		118	-	66	-	ns
t_{CLCL}	CLK Cycle Period		200	-	125	-	ns
t_{CLLH}	ALE Active Delay (from CLK)	A	-	35	-	20	ns
t_{CLMCH}	MCE Active Delay (from CLK)	A	-	35	-	25	ns
t_{CLMH}	Command Inactive Delay	B	5	45	5	35	ns
t_{CLML}	Command Active Delay	B	5	45	5	35	ns
t_{CLSH}	Status Active Hold Time		10	-	10	-	ns
t_{CVNV}	Control Active Delay	A	5	45	5	45	ns
t_{CVNX}	Control Inactive Delay	A	5	45	10	45	ns
t_{OHOL}	Output, Fall Time	From 2.2 V to 0.8 V	-	12	-	15	ns
t_{OLOH}	Output, Rise Time	From 0.8 V to 2.2 V	-	20	-	15	ns
t_{SHCL}	Status Inactive Setup Time		35	-	35	-	ns
t_{SVCH}	Status Active Setup Time		35	-	35	-	ns
t_{SVLH}	ALE Active Delay (from Status)	A	-	35	-	20	ns
t_{SVMCH}	MCE Active Delay (from Status)	A	-	35	-	30	ns

Refer to Figure 5 for Test Conditions Definition Table

Notes:
1. t_{AELCH} measurement is between 1.5 V and 2.5 V.
2. t_{AEHCZ} measured at 0.5 V change in V_{OUT}.
3. In 5 MHz 80C86/88 systems, minimum ALE HIGH time = t_{CLCL} - (t_{CHSV}(max) + t_{SVLH}) + t_{CHLL}(min) = 74 ns.
4. t_{AELCV} = 60 ns minimum for industrial temperature range devices.

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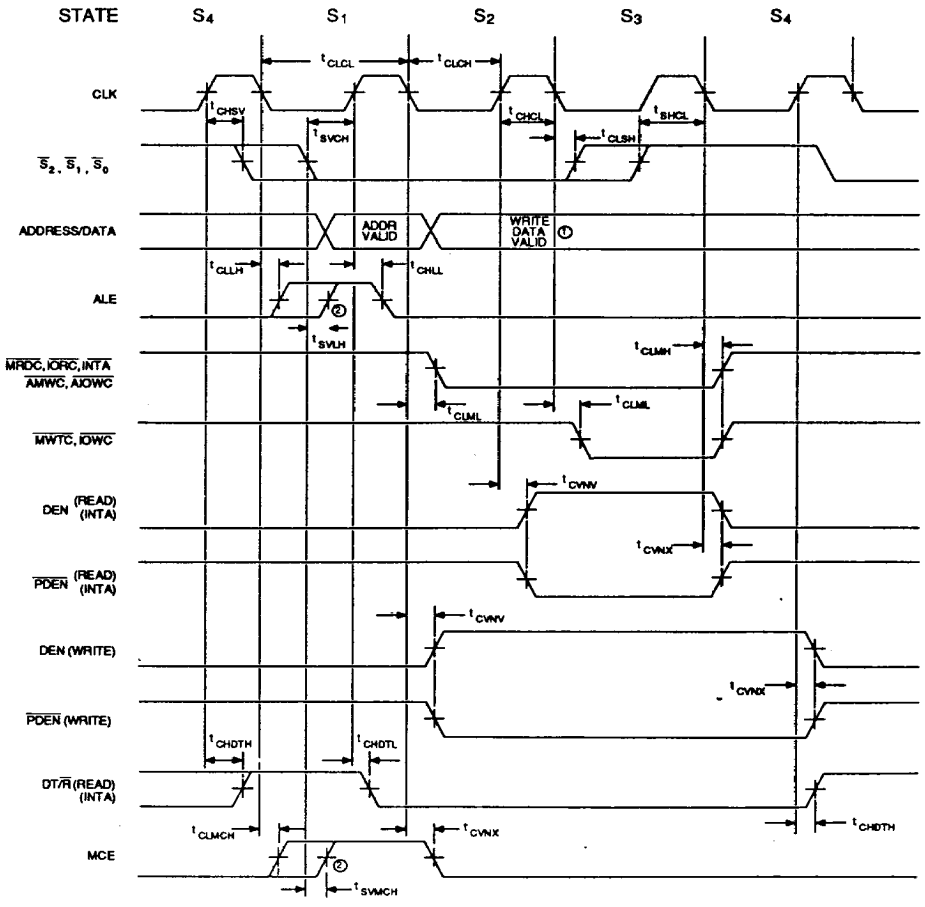
Figure 3 : TIMING DIAGRAMS

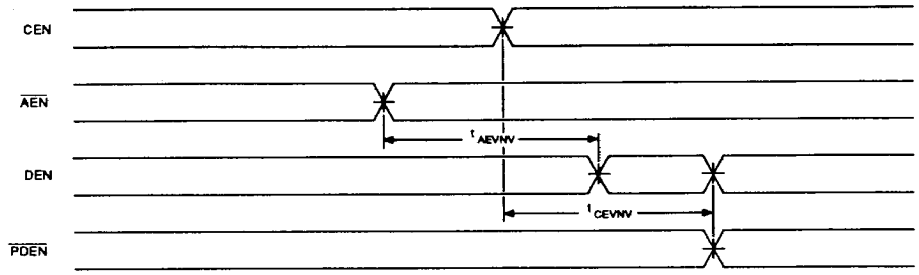
a) Read/Write Timing



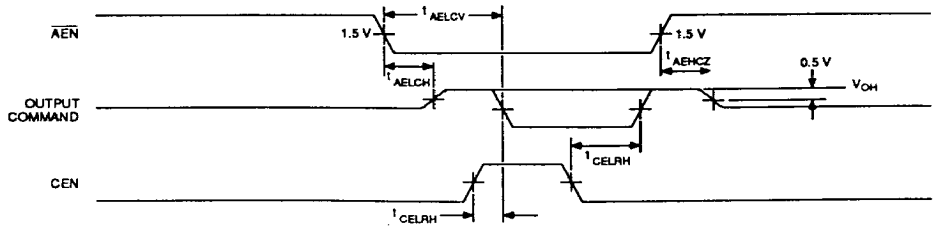
Notes:

1. Address/Data bus is shown only for reference purposes.
2. Leading edge of ALE and MCE is determined by the falling edge of CLK or STATUS going active, whichever occurs last.

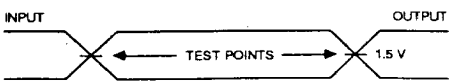
b) DEN, $\overline{PDEN}$ Qualification Timing



c) Address Enable Timing (3-State Enable/Disable)



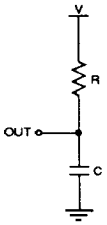
Note: CEN must be low or valid prior to T2 to prevent the command from being generated.



AC Testing: Input rise and fall times are:

5ns ± 2ns between 0.8V and 2.2V for $\overline{AEN}$, $\overline{CEN}$ & IOB

8ns ± 2ns between 0.8V and 3.0V for $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$ & CLK



Test Condition	V (V)	R (W)	C (pF)
A	3.34	360	80
B	2.74	190	150
C	1.5	300	150
D	1.5	180	50

Figure 4 : AC TESTING I/O WAVEFORM

Figure 5 : TEST LOAD CIRCUITS, 3-STATE COMMAND OUTPUT TEST LOAD

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Table 5 : DC CHARACTERISTICS (T_A = –40° to +85°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter		Test Conditions	Limits		Units
				Min	Max	
C_{IN}	Input Capacitance		Freq. = 1 MHz	-	5	pF
C_{OUT}	Output Capacitance		Unmeasured pins at V_{SS}	-	15	pF
I_{DD}	Operating Supply Current		$V_{IN} = V_{DD}$ or V_{SS} V_{DD} = 5.5 V, Freq = 5MHz Outputs Unloaded	-	10	mA
I_{DDS}	Standby Supply Current		$V_{IN} = V_{DD}$ or V_{SS} V_{DD} = 5.5 V Outputs Unloaded (Note 2)	-	100	µA
I_{LI}	Input Leakage Current		$0V \le V_{IN} \le V_{DD}$ (Note 1)	-	±10.0	µA
I_{LO}	Output Leakage Current		$0V \le V_{OUT} \le V_{DD}$	-	±10	µA
V_{CH}	V_{IH} for Clock, $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$			3.0	V_{DD} + 0.3	V
V_{CL}	V_{IL} for Clock, $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$			–0.3	0.8	V
V_{IH}	Input High Voltage			2.2	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			–0.3	0.8	V
V_{OH}	Output High Voltage	Command Outputs	I_{OH} = –5 mA	3.7	-	V
		Control Outputs	I_{OH} = –1 mA	3.7	-	V
V_{OL}	Output Low Voltage	Command Outputs	I_{OL} = 12 mA	-	0.45	V
		Control Outputs	I_{OL} = 8 mA	-	0.45	V

Notes: 1. Except $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$. Input leakage current for status inputs is between –100µA and +10µA.
2. I_{DDS} test conditions are: Status input @ V_{DD} or V_{SS}, Outputs open.

Table 6 : RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage		+4 V to +6 V
Operating Temperature Range	Commercial	0°C to 70°C
	Industrial	–40°C to +85°C

Table 7 : ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	+7.0 V
Input, Output or I/O Voltage Applied	V_{SS} – 0.5 V to V_{DD} + 0.5 V
Storage Temperature Range	–65°C to +150°C
Maximum Package Power Dissipation	1 W

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.