CALMOS™

CA91C014

VMEbus AVICS CONTROL CIRCUIT (ACC)

- **Full VMEbus system controller functions**
- **Auto-ID slot identification**
- **Automatic VMEbus SYSCON identification**
- **Bus isolation (BI-mode™) controller**
- **Multiple VMEbus request and release options**
- **Local bus requester/arbiter**
- **Bus request on any of the four VMEbus levels**
- **Multiple VMEbus arbitration schemes**
- **VMEbus interrupt handler for all seven VMEbus interrupts**
- **VMEbus interrupter on any of the seven VMEbus interrupts**
- **Local interrupt handler**
- **Watchdog timer and local bus timeout**
- **Reset and clock generation**
- **Four general purpose clocks**
  14μs DRAM refresh clock
  2.4615 MHz baud clock
  1μs and 14 ms general purpose clocks
  Tick clocks from 200μs to 100ms
- **Low power CMOS, with power dissipation < 1W)**
- **144 Pin Grid Array package**
- **Available in MIL-STD 883C Class B version**

The CA91C014 Advanced System Architecture Control Circuit (ACC) is part of the Advanced VMEbus Interface Chip Set (AVICS); the other part being the CA91C015 Data and Address Register File (DARF). The AVICS integrates all the functions commonly required to interface a card to the VMEbus, while adding features that provide major architectural improvements.

The ACC is designed to work with the DARF, but is also capable of being used as a stand-alone device to provide the feature list above. The functions of the ACC are separated into seven distinct modules:

- Reset, Clock, and BI-mode™ Module
- Local Bus Requester/Arbiter
- Interrupt Handler
- VMEbus Requester
- VMEbus Arbiter
- IACK Daisy Chain Driver
- Register Block

The Reset, Clocks, and BI-mode™ module and the *Local Bus Requester* module are basically service functions and have very little interaction with software. The *Register Block* module provides the programming interface to the device. The remaining four modules; the *Interrupt Handler*, the *VMEbus Arbiter*, *VMEbus Requester* and *IACK Daisy Chain Driver* modules, can be configured by software to operate in various modes. They are accessed via the Register Block module.

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BI-mode™ is a trademark of DY-4 Systems Inc, denoting the Bus Isolation mode.

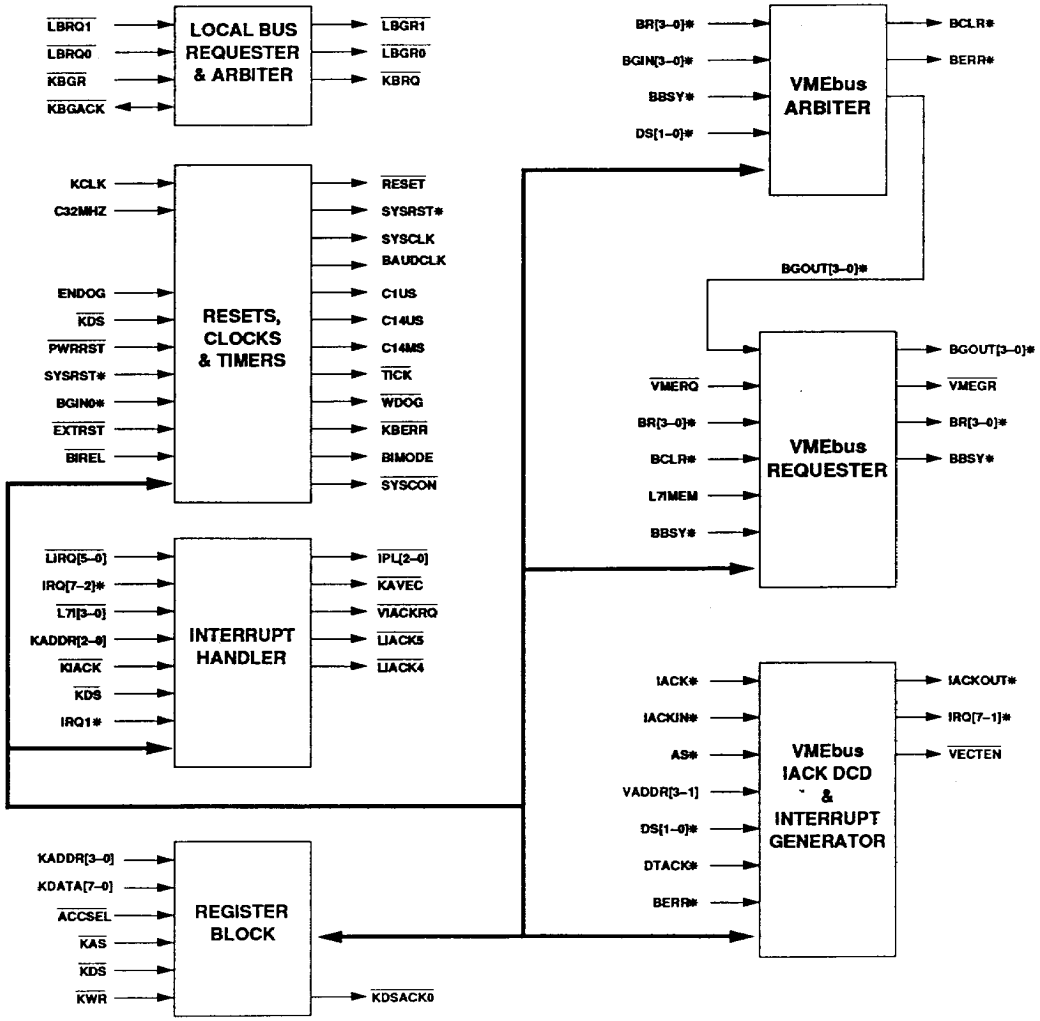

Figure 1 : CA91C014 ACC BLOCK DIAGRAM

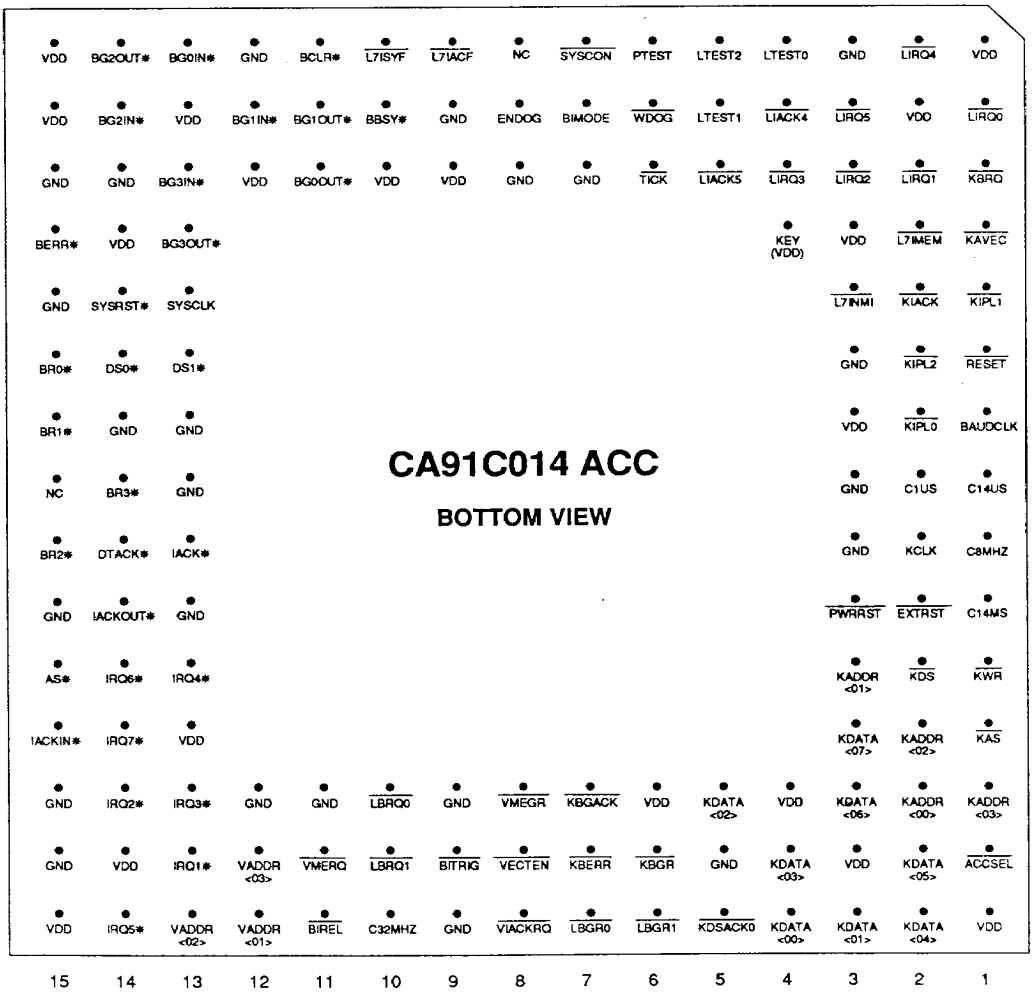

Figure 2 : PIN CONFIGURATION for 144–PIN PGA PACKAGE

Table 1 : ACC PGA PINOUT

Pin	Signal	Signal Group	Pin	Signal	Signal Group
A1	V_{DD}		C9	V_{DD}	
A2	$\overline{LIRQ4}$	Interrupt	C10	V_{DD}	
A3	V_{SS}		C11	BG0OUT*	VMEbus
A4	LTEST0	Reset, Clock & Mode	C12	V_{DD}	
A5	LTEST2	Reset, Clock & Mode	C13	BG3IN*	VMEbus
A6	PTEST	Reset, Clock & Mode	C14	V_{SS}	
A7	$\overline{SYSCON}$	Reset, Clock & Mode	C15	V_{SS}	
A8	N/C		D1	$\overline{KAVEC}$	Interrupt
A9	$\overline{L7IACF}$	Interrupt	D2	$\overline{L7IMEM}$	Interrupt
A10	$\overline{L7ISYF}$	Interrupt	D3	V_{DD}	
A11	BCLR*	VMEbus	D13	BG3OUT*	VMEbus
A12	V_{SS}		D14	V_{DD}	
A13	BG0IN*	VMEbus	D15	BERR*	VMEbus
A14	BG2OUT*	VMEbus	E1	$\overline{KIPL1}$	Interrupt
A15	V_{DD}		E2	$\overline{KIACK}$	Interrupt
B1	$\overline{LIRQ0}$	Interrupt	E3	$\overline{L7INMI}$	Interrupt
B2	V_{DD}		E13	SYSCLK	Reset, Clock & Mode
B3	$\overline{LIRQ5}$	Interrupt	E14	SYSRST*	Reset, Clock & Mode
B4	$\overline{LIACK4}$	Interrupt	E15	V_{SS}	
B5	LTEST1	Reset, Clock & Mode	F1	$\overline{RESET}$	Reset, Clock & Mode
B6	$\overline{WDOG}$	Reset, Clock & Mode	F2	$\overline{KIPL2}$	Interrupt
B7	BIMODE	Reset, Clock & Mode	F3	V_{SS}	
B8	ENDOG	Reset, Clock & Mode	F13	DS1*	VMEbus
B9	V_{SS}		F14	DS0*	VMEbus
B10	BBSY*	VMEbus	F15	BR0*	VMEbus
B11	BG1OUT*	VMEbus	G1	BAUDCLK	Reset, Clock & Mode
B12	BG1IN*	VMEbus	G2	$\overline{KIPL0}$	Interrupt
B13	V_{DD}		G3	V_{DD}	
B14	BG2IN*	VMEbus	G13	V_{SS}	
B15	V_{DD}		G14	V_{SS}	
C1	$\overline{KBRQ}$	Local Bus	G15	BR1*	VMEbus
C2	$\overline{LIRQ1}$	Interrupt	H1	C14US	Reset, Clock & Mode
C3	$\overline{LIRQ2}$	Interrupt	H2	C1US	Reset, Clock & Mode
C4	$\overline{LIRQ3}$	Interrupt	H3	V_{SS}	
C5	$\overline{LIACK5}$	Interrupt	H13	V_{SS}	
C6	$\overline{TICK}$	Reset, Clock & Mode	H14	BR3*	VMEbus
C7	V_{SS}		H15	N/C	
C8	V_{SS}		J1	C8MHZ	Reset, Clock & Mode

Table 1 : ACC PGA PINOUT CON'T

Pin	Signal	Signal Group	Pin	Signal	Signal Group
J2	KCLK	Reset, Clock & Mode	N12	V_{SS}	
J3	V_{SS}		N13	IRQ3*	Interrupt
J13	IACK*	VMEbus	N14	IRQ2*	Interrupt
J14	DTACK*	VMEbus	N15	V_{SS}	
J15	BR2*	VMEbus	P1	$\overline{ACCSEL}$	Local Bus
K1	C14MS	Reset, Clock & Mode	P2	KDATA 05	Local Bus
K2	$\overline{EXTRST}$	Reset, Clock & Mode	P3	V_{DD}	
K3	$\overline{PWRRST}$	Reset, Clock & Mode	P4	KDATA 03	Local Bus
K13	V_{SS}		P5	V_{SS}	
K14	IACKOUT*	VMEbus	P6	$\overline{KBGR}$	Local Bus
K15	V_{SS}		P7	$\overline{KBERR}$	Local Bus
L1	$\overline{KWR}$	Local Bus	P8	$\overline{VECTEN}$	Interrupt
L2	$\overline{KDS}$	Local Bus	P9	$\overline{BITRIG}$	Reset, Clock & Mode
L3	KADDR 01	Local Bus	P10	$\overline{LBRQ1}$	Local Bus
L13	IRQ4*	Interrupt	P11	$\overline{VMERQ}$	VMEbus
L14	IRQ6*	Interrupt	P12	VADDR 03	VMEbus
L15	AS*	VMEbus	P13	IRQ1*	Interrupt
M1	$\overline{KAS}$	Local Bus	P14	V_{DD}	
M2	KADDR 02	Local Bus	P15	V_{SS}	
M3	KDATA 07	Local Bus	Q1	V_{DD}	
M13	V_{DD}		Q2	KDATA 04	Local Bus
M14	IRQ7*	Interrupt	Q3	KDATA 01	Local Bus
M15	IACKIN*	VMEbus	Q4	KDATA 00	Local Bus
N1	KADDR 03	Local Bus	Q5	$\overline{KDSACK0}$	Local Bus
N2	KADDR 00	Local Bus	Q6	$\overline{LBGR1}$	Local Bus
N3	KDATA 06	Local Bus	Q7	$\overline{LBGR0}$	Local Bus
N4	V_{DD}		Q8	$\overline{VIACKRQ}$	Interrupt
N5	KDATA 02	Local Bus	Q9	V_{SS}	
N6	V_{DD}		Q10	C32MHZ	Reset, Clock & Mode
N7	$\overline{KBGACK}$	Local Bus	Q11	$\overline{BIREL}$	Reset, Clock & Mode
N8	$\overline{VMEGR}$	VMEbus	Q12	VADDR 01	VMEbus
N9	V_{SS}		Q13	VADDR 02	VMEbus
N10	$\overline{LBRQ0}$	Local Bus	Q14	IRQ5*	Interrupt
N11	V_{SS}		Q15	V_{DD}	

Note: Ceramic PGA packages have an additional pin, D4, that is internally connected to pin D3 (V_{DD}).

Table 2a : VMEbus SIGNALS

Symbol	Pin(s)	Type	Name and Function
AS*	L15	I	VMEbus address strobe
BBSY*	B10	I/O	Bus Busy indicator
BCLR*	A11	I/O	Bus Clear request
BERR*	D15	I/O	VMEbus data transfer error
BG3IN* – BG0IN*	C13, B14, B12, A13	I	Bus Grant In of grant daisy chain
BG3OUT* – BG0OUT*	D13, A14, B11, C11	O	Bus Grant Out of grant daisy chain
BR3* – BR0*	H14, J15, G14, F15	I/O	Bus request lines
DS1* – DS0*	F13, F14	I	VMEbus data strobes 1, 0
DTACK*	J14	I	VMEbus data transfer acknowledge
IACK*	J13	I	Interrupt Acknowledge cycle indicator
IACKIN*	M15	I	IACK daisy chain
IACKOUT*	K14	O	IACK daisy chain
VADDR 03 – 01	P12, Q13, Q12	I	VMEbus address bits 3, 2, 1
$\overline{\text{VMEGR}}$	N8	O	VMEbus grant to the DARF
$\overline{\text{VMERQ}}$	P11	I	VMEbus request from the DARF

Table 2b : LOCAL BUS SIGNALS

Symbol	Pin(s)	Type	Name and Function
$\overline{\text{ACCSEL}}$	P1	I	ACC select
KADDR 03 – 00	N1, M2, L3, N2	I	Address lines 3 through 0
$\overline{\text{KAS}}$	M1	I	Local address strobe
$\overline{\text{KBERR}}$	P7	O	Local bus timeout error signal
$\overline{\text{KBGACK}}$	N7	I/O	Bus grant acknowledge
$\overline{\text{KBGR}}$	P6	I	Local bus grant from the local CPU
$\overline{\text{KBRQ}}$	C1	O	Local bus request to the local CPU
KDATA 07 – 00	M3, N3, P2, Q2, P4, N5, Q3, Q4	I/O	Data lines 7 through 0
$\overline{\text{KDS}}$	L2	I	Local data strobe
$\overline{\text{KDSACK0}}$	Q5	O	Data transfer acknowledge signal
$\overline{\text{KWR}}$	L1	I	Local write control
$\overline{\text{LBGR0}}$	Q7	O	Local bus grant to the DARF
$\overline{\text{LBGR1}}$	Q6	O	Local bus grant to the second device
$\overline{\text{LBRQ0}}$	N10	I	Local bus request from the DARF
$\overline{\text{LBRQ1}}$	P10	I	Local bus request from a second device

Table 2c : INTERRUPT SIGNALS

Symbol	Pin(s)	Type	Name and Function
IRQ1*	P13	I/O	VMEbus interrupt 1 and BI-mode™ trigger
IRQ7* – IRQ2*	M14, L14, Q14, L13, N13, N14	I/O	VMEbus interrupts 7-2
$\overline{\text{KAVEC}}$	D1	O	Autovector response to acknowledge cycle
$\overline{\text{KIACK}}$	E2	I	Interrupt acknowledge cycle indicator
$\overline{\text{KIPL2}}$ – $\overline{\text{KIPL0}}$	F2, E1, G2	O	Interrupt level code to CPU
$\overline{\text{L7INMI}}$	E3	I	Local level 7 non maskable interrupt
$\overline{\text{L7IMEM}}$	D2	I	Local level 7 interrupt typically memory failure
$\overline{\text{L7IACF}}$	A9	I	Level 7 interrupt, typically ACFAIL*
$\overline{\text{L7ISYF}}$	A10	I	Level 7 interrupt, typically SYSFAIL*
$\overline{\text{LIACK4}}$	B4	O	Acknowledge to interrupt on LIRQ4
$\overline{\text{LIACK5}}$	C5	O	Acknowledge to interrupt on LIRQ5
$\overline{\text{LIRQ5}}$ – $\overline{\text{LIRQ0}}$	B3, A2, C4, C3, C2, B1	I	Local general purpose interrupts 5 - 0
$\overline{\text{VECTEN}}$	P8	O	Vector enable signal to DARF
$\overline{\text{VIACKRQ}}$	Q8	O	Signal to DARF to acknowledge VMEbus interrupt

Table 2d : RESET, CLOCK, and MODE SIGNALS

Symbol	Pin(s)	Type	Name and Function
BAUDCLK	G1	O	2.4615 megahertz baud rate clock
BIMODE	B7	O	BI-mode™ indicator
$\overline{\text{BIREL}}$	Q11	I	BI-mode™ exit signal
$\overline{\text{BITRIG}}$	P9	I	BI-mode™ trigger signal
C1US	H2	O	1 microsecond clock output
C14MS	K1	O	14 millisecond clock output
C14US	H1	O	14 microsecond clock output
C8MHZ	J1	O	8 MHz clock output
C32MHZ	Q10	I	32 megahertz clock input
ENDOG	B8	I	Enable watchdog control pin
$\overline{\text{EXTRST}}$	K2	I	External reset
KCLK	J2	I	CPU clock
LTEST2 – LTEST0	A5, B5, A4	I	IC manufacturing test
PTEST	A6	O	IC manufacturing test
$\overline{\text{PWRRST}}$	K3	I	Power up reset input, from R-C network
$\overline{\text{RESET}}$	F1	O	Local (card) reset output
SYSCLK	E13	I/O	VMEbus SYSCLK signal
$\overline{\text{SYSCON}}$	A7	O	VMEbus system controller indicator
SYSRST*	E14	I/O	VMEbus SYSRST* signal
$\overline{\text{TICK}}$	C6	O	Tick output, available for interrupting
$\overline{\text{WDOG}}$	B6	O	Watchdog signal, 2 second period

TERMINOLOGY

Signals on the VMEbus and those within the circuit card may be active high or active low. Active low signals are defined as being true or asserted when they are at a low voltage, and conversely for active high signals. VMEbus active low signals are indicated by the * suffix. Local active low signals are indicated by an OVERBAR.

Where there is a need to clarify whether a signal is a VMEbus or local signal, a V may be prefixed for VMEbus signals, an L for general local signals, or a K for signals only connecting to the local CPU.

The I/O type abbreviations used in Tables 3 and 14 are defined in this section. A number suffix (where appended) indicates the current rating of the output.

TP	Totem pole output
TS	Tri-state totem pole output
OD	Open drain output
VOD	VMEbus specification open drain output
VTS	VMEbus specification tri-state totem pole output
CMOS SCH	Schmitt trigger input with CMOS thresholds
TTL	Input with TTL thresholds
TTL PD	Input with TTL thresholds and integral pull down
TTL PU	Input with TTL thresholds and integral pull up
TTL SCH	Schmitt trigger input with TTL thresholds

Table 3 : SIGNAL INPUT and OUTPUT TYPE CLASSIFICATION

Signal	Input	Output	Signal	Input	Output
ACCSEL	TTL		KBRQ		TP4
AS*	TTL		KCLK	TTL	
BAUDCLK		TP8	KDATA 07 – 00	TTL	TS6
BBSY*	TTL SCH	VOD48	KDS	TTL	
BCLR*	TTL SCH	VTS64	KDSACK0		TS8
BERR*	TTL SCH	VOD48	KIACK	TTL	
BG2IN* – BG0IN*	TTL PU		KWR	TTL	
BG3IN*	TTL PD		LBGR0		TP4
BG3OUT* – BG0OUT*		TP8	LBGR1		TP4
BIMODE		TP8	LBRQ0	TTL	
BIREL	TTL		LBRQ1	TTL	
BR3* – BR0*	TTL SCH	VOD48	LIACK4		TP4
C1US		TP8	LIACK5		TP4
C14MS		TP4	LIRQ5 – LIRQ0	TTL	
C14US		TP8	LTEST2 – LTEST0	TTL	
C8MHZ		TP8	L7IACF	TTL	
C32MHZ	TTL		L7IMEM	TTL	
DS1*, DS0*	TTL		L7INMI	TTL	
DTACK*	TTL		L7ISYF	TTL	
ENDOG	TTL		PTEST		TP4
EXTRST	TTL		PWRRST	CMOS SCH	
IACK*	TTL		RESET		TP12
IACKIN*	TTL		SYSCLK	TTL SCH	VTS64
IACKOUT*		TP8	SYSCON		TP8
KIPL2 – KIPL0		TP4	SYSRST*	TTL SCH	VOD48
IRQ7* – IRQ1*	TTL SCH	VOD48	TICK		TP4
KADDR 03 – 00	TTL		VADDR 03 – 01	TTL	
KAS	TTL		VECTEN		TP4
KAVEC		TP4	VIACKRQ		TP4
KBERR		TS8	VMEGR		TP4
KBGACK	TTL	OD8	VMERQ	TTL	
KBGR	TTL		WDOG		TP4

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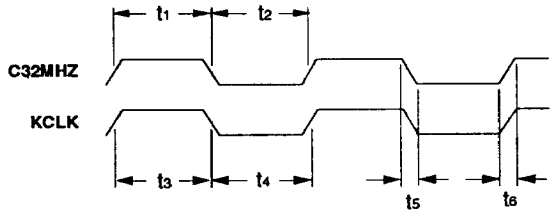
Table 4 : AC CHARACTERISTICS (CLOCK and TIMING SIGNALS)
Commercial: T_A = 0° to +70°C, V_{DD} = 5V ± 5%, Military T_A = −55° to +125°C, V_{DD} = 5V ± 10%

Symbol	Description	Limits				Unit
		Min	Typ	Max		
				Com	Mil	
t_1	C32MHZ high time	10.6	15.6	20.6	20.6	ns
t_2	C32MHZ low time	10.6	15.6	20.6	20.6	ns
t_3	KCLK high time (Note 1)	20	-	-	-	ns
t_4	KCLK low time (Note 1)	20	-	-	-	ns
t_5	C32MHZ and KCLK fall time	0	-	5	5	ns
t_6	C32MHZ and KCLK rise time	0	-	5	5	ns
t_7	C14US low from KCLK fall	3.9	10	20	25	ns
t_8	C14US high from KCLK fall	3.2	8	16	20	ns
t_9	C14US period (Note 2)	-	14	-	-	µs
t_{10}	C14US low time (Note 2)	-	7	-	-	µs
t_{11}	C14US high time (Note 2)	-	7	-	-	µs
t_{12}	C1US period	1	1	1	1	µs
t_{13}	C1US low time	500	500	500	500	ns
t_{14}	C1US high time	500	500	500	500	ns
t_{15}	C14MS period (Note 3)	14.3	14.3	14.3	14.3	ms
t_{16}	C14MS low time (Note 3)	7.16	7.16	7.16	7.16	ms
t_{17}	C14MS high time (Note 3)	7.16	7.16	7.16	7.16	ms
t_{18}	SYSCLK high from C32MHZ rise	3.9	9	18	22	ns
t_{19}	BAUDCLK high from C32MHZ rise	3.2	8	15	18	ns
t_{20}	SYSCLK low from C32MHZ rise	4.7	12	23	29	ns
t_{21}	BAUDCLK low from C32MHZ rise	3.9	10	19	23	ns
t_{22}	SYSCLK high time	25.0	31.3	37.5	37.5	ns
t_{23}	SYSCLK low time	25.0	31.3	37.5	37.5	ns
t_{24}	SYSCLK period	62.5	62.5	62.5	62.5	ns
t_{25}	BAUDCLK high time (Note 4)	187	187	187	187	ns
t_{26}	BAUDCLK low time (Note 4)	219	219	219	219	ns
t_{27}	BAUDCLK period (Note 4)	406	406	406	406	ns
t_{28}	WDOG expiry period (Note 5)	2.0	2.0	2.0	2.0	s
t_{29}	WDOG assertion time (Note 5)	200	200	200	200	ms
t_{30}	C8MHZ high from C32MHZ rise	4.4	11	21	26	ns
t_{31}	C8MHZ low from C32MHZ rise	5.0	13	25	31	ns
t_{32}	C8MHZ high time	-	62.5	-	-	ns
t_{33}	C8MHZ low time	-	62.5	-	-	ns
t_{34}	C8MHZ period	125	125	125	125	ns

Notes:
1. KCLK must be the same as the CPU clock; any frequency up to 25 MHz is valid.
2. C14US changes are synchronized by ACC to falling edge of KCLK, causing jitter on each KCLK edge equal to the KCLK period.
3. The exact frequency of C14MS is 14.3333... ms, equal to 14 µs times 1024.
4. BAUDCLK is 32 MHz divided by 13, high 6 parts out of 13. High time is 187.5 ns, low time is 218.75 ns, frequency is 2.461538 MHz.
5. Expiry period begins at last reset, deassertion of ENDOG pin, or clearing of counter by software. Period and low time tolerance is ±1 µs.

Figure 3 : CLOCK and TIMING SIGNALS

a) Required Clock Input Characteristics



b) Generated Timing Clock Characteristics

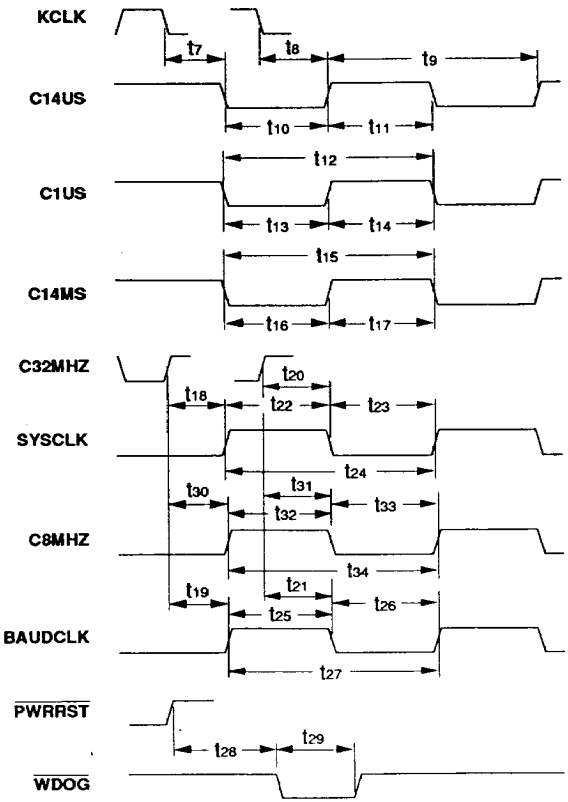


Table 5 : AC CHARACTERISTICS (RESET SIGNAL TIMING)
Commercial: T_A = 0° to +70°C, V_{DD} = 5V ± 5%, Military T_A = −55° to +125°C, V_{DD} = 5V ± 10%

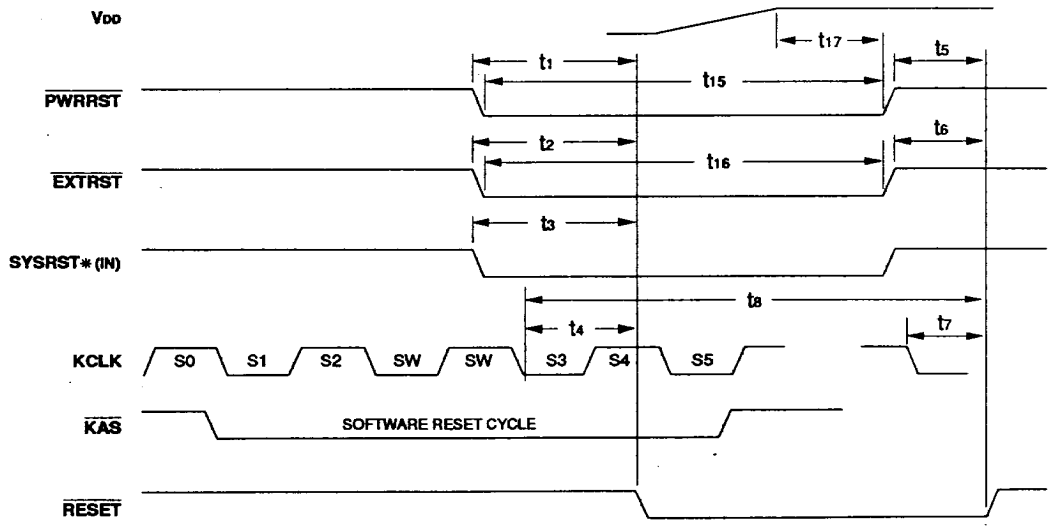
Symbol	Description	Limits				Unit
		Min	Typ	Max		
				Com	Mil	
t_1	$\overline{\text{RESET}}$ assertion from $\overline{\text{PWRRST}}$ (Note 1)	6.2	16	32	39	ns
t_2	$\overline{\text{RESET}}$ assertion from $\overline{\text{EXTRST}}$	5.4	13	27	32	ns
t_3	$\overline{\text{RESET}}$ assertion from SYSRST*	5.6	13	26	31	ns
t_4	$\overline{\text{RESET}}$ assert from s/w reset (Note 2)	10	26	51	62	ns
t_5	$\overline{\text{RESET}}$ negate from $\overline{\text{PWRRST}}$	0.21	0.22	0.23	0.23	s
t_6	$\overline{\text{RESET}}$ negate from $\overline{\text{EXTRST}}$	0.21	0.22	0.23	0.23	s
t_7	$\overline{\text{RESET}}$ negate from KCLK low	3.9	9.2	18	22	ns
t_8	$\overline{\text{RESET}}$ negate from s/w reset (Note 2)	0.21	0.22	0.23	0.23	s
t_9	SYSRST* assert from $\overline{\text{PWRRST}}$ (Note 1)	6.6	17	34	41	ns
t_{10}	SYSRST* assert from s/w reset (Note 2)	10	27	52	64	ns
t_{11}	SYSRST* assert from BG0IN* (Note 3)	43	50	58	58	ms
t_{12}	SYSRST* negate from $\overline{\text{PWRRST}}$	0.21	0.22	0.23	0.23	s
t_{13}	SYSRST* negate from s/w reset (Note 2)	0.21	0.22	0.23	0.23	s
t_{14}	SYSRST* negate from BG0IN* (Note 4)	0.21	0.22	0.23	0.23	s
t_{15}	$\overline{\text{PWRRST}}$ width, low (Note 1)	50	-	-	-	ns
t_{16}	$\overline{\text{EXTRST}}$ width, low (Note 1)	50	-	-	-	ns
t_{17}	$\overline{\text{PWRRST}}$ hold low from V_{DD} = 4.5V	100	-	-	-	ns

Notes:

1. Assumes V_{DD} stable at 5.0 V prior to $\overline{\text{PWRRST}}$ asserting.
2. Measured from indicated edge of S3 of CPU cycle.
3. Four successive samples of a low level on BG0IN* by the rising edge of the internal 14 ms clock are required to initiate reset.
4. Measured from the first high level sampled on BG0IN* after SYSRST* has been started.

Figure 4 : RESET SIGNAL TIMING

a) Local Reset Generation



b) System Reset Generation

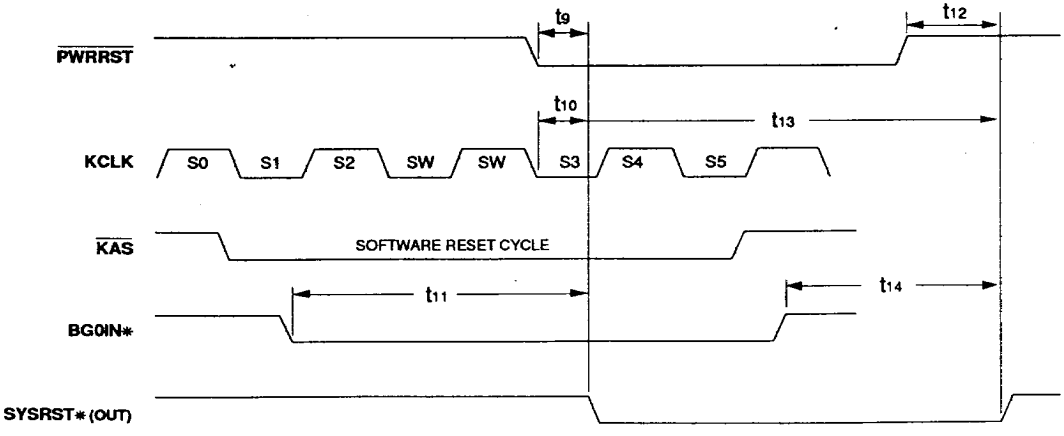


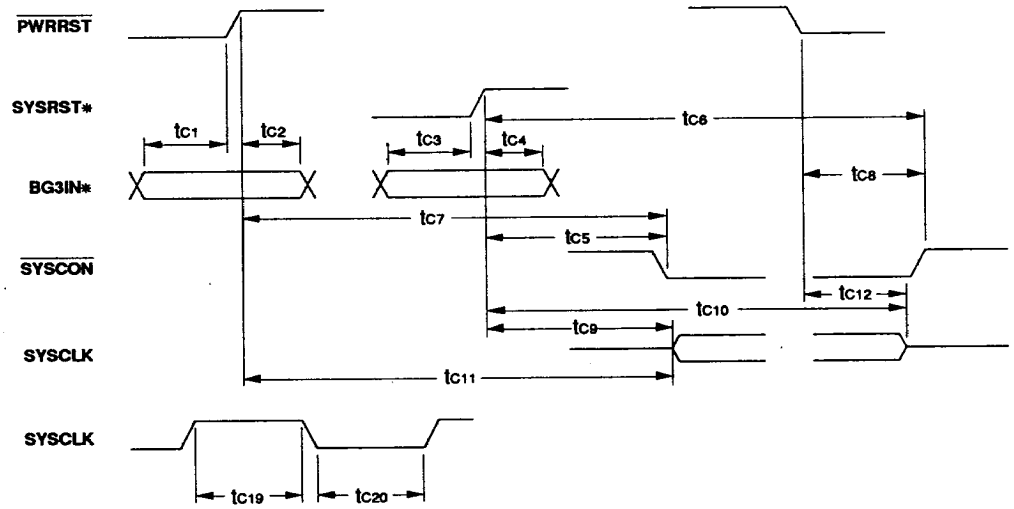
Table 6 : AC CHARACTERISTICS (SYSCON and BI-MODE™ TIMING)
Commercial: T_A = 0° to +70°C, V_{DD} = 5V ± 5%, Military T_A = −55° to +125°C, V_{DD} = 5V ± 10%

Symbol	Description	Limits				Unit
		Min	Typ	Max		
				Com	Mil	
t_{C1}	BG3IN* setup to $\overline{\text{PWRRST}}$ (Note 1)	−200	-	-	-	ns
t_{C2}	BG3IN* hold from $\overline{\text{PWRRST}}$ (Note 1)	565	-	-	-	ns
t_{C3}	BG3IN* setup to SYSRST*	10	-	-	-	ns
t_{C4}	BG3IN* hold from SYSRST*	10	-	-	-	ns
t_{C5}	$\overline{\text{SYSCON}}$ assert from SYSRST* high	7.2	17	34	41	ns
t_{C6}	$\overline{\text{SYSCON}}$ negate from SYSRST* high	6.4	16	31	38	ns
t_{C7}	$\overline{\text{SYSCON}}$ assert from $\overline{\text{PWRRST}}$ up	465	500	565	565	ns
t_{C8}	$\overline{\text{SYSCON}}$ negate from $\overline{\text{PWRRST}}$ down	5.0	13	25	31	ns
t_{C9}	SYSCLK driving from SYSRST* high	7.8	18	37	45	ns
t_{C10}	SYSCLK high-z from SYSRST* high	8.1	20	40	49	ns
t_{C11}	SYSCLK driving from $\overline{\text{PWRRST}}$ up	465	500	565	565	ns
t_{C12}	SYSCLK high-z from $\overline{\text{PWRRST}}$ low	6.8	17	34	42	ns
t_{C13}	BIMODE assert from IRQ1*	37	60	89	95	ns
t_{C14}	IRQ1* assert by ABI s/w bit	8.6	22	43	52	ns
t_{C15}	BIMODE assert by SBI s/w bit	7.4	19	37	45	ns
t_{C16}	BIMODE negate from $\overline{\text{BIREL}}$	3.6	9	17	21	ns

Notes:
1. BG3IN* is sampled 500 ± 31.25 ns after $\overline{\text{PWRRST}}$ reaches logic 1.

Figure 5 : SYSCON and BI-MODE™ TIMING

a) SYSCON and SYSCLK Characteristics



b) BI-MODE™ Entry and Exit Timing

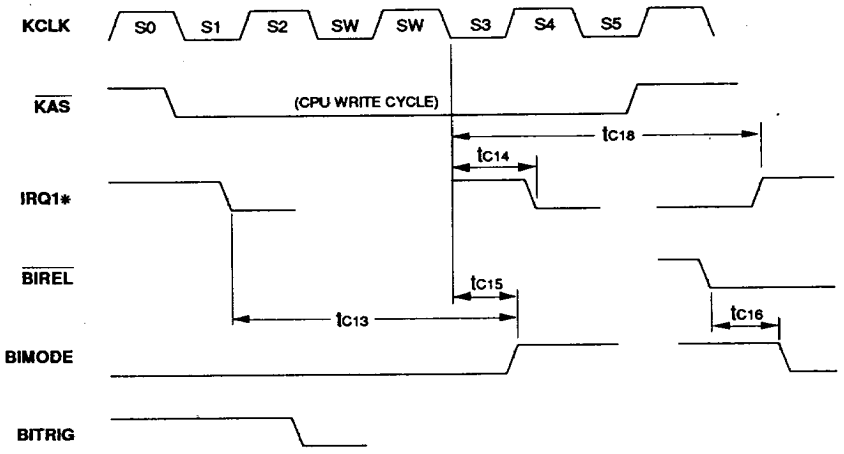


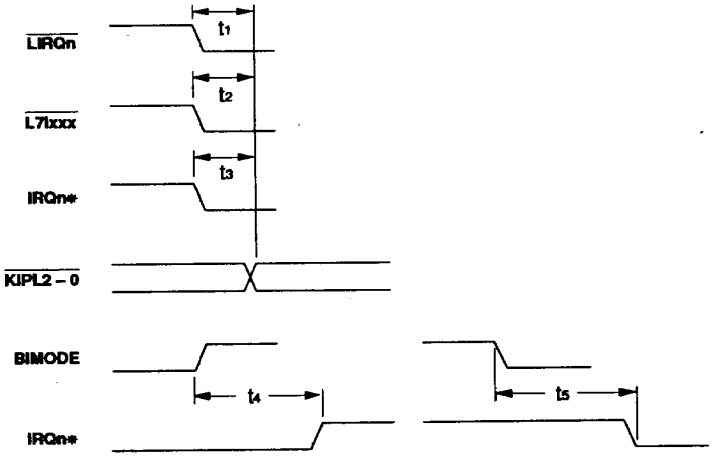
Table 7 : AC CHARACTERISTICS (INTERRUPT SIGNAL TIMING)
Commercial: T_A = 0° to +70°C, V_{DD} = 5V ± 5%, Military T_A = –55° to +125°C, V_{DD} = 5V ± 10%

Symbol	Description	Limits				Unit
		Min	Typ	Max		
				Com	Mil	
t_1	KIPL change from local interrupt	9.3	24	48	59	ns
t_2	Level 7 KIPL change from C32MHZ high	10.8	28	55	68	ns
t_3	KIPL change from VME int	8.2	22	43	53	ns
t_4	VME interrupt negate from BIMODE high	3.0	8	15	39	ns
t_5	VME interrupt reassert from KCLK high	5.7	15	29	35	ns
	(Note 1)					
t_6	Iack generation from KCLK	5.4	14	28	35	ns
t_7	KIPL change from KCLK down	8.1	25	49	60	ns
t_8	VME interrupt assert from KCLK	5.7	15	29	35	ns
t_9	$\overline{IACK}$ negate from $\overline{KDS}$ negate	4.2	11	22	27	ns

Notes:
1. After next KCLK falling edge at which BIMODE is negated.

Figure 6 : INTERRUPT SIGNAL TIMING

a) IPL Generation, BI-MODE Effect on IRQ Generation



b) IRQ Assertion, Interrupt Enabling and Acknowledging

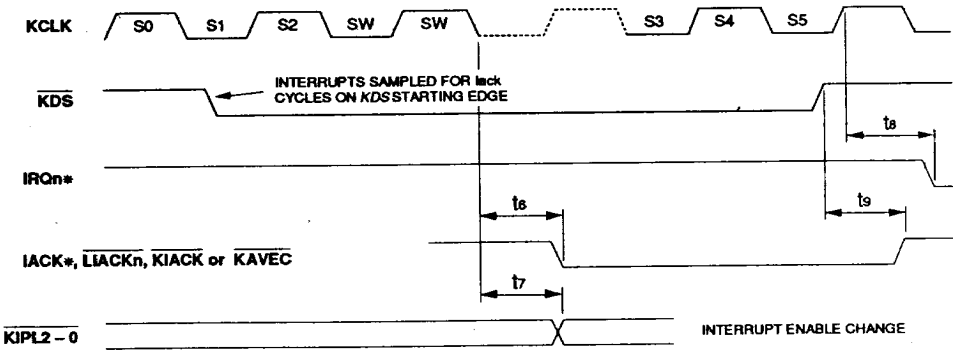


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Table 8 : AC CHARACTERISTICS (REGISTER ACCESS READ and WRITE TIMING)
Commercial: T_A = 0° to +70°C, V_{DD} = 5V ± 5%, Military T_A = −55° to +125°C, V_{DD} = 5V ± 10%

Symbol	Description	Limits				Unit
		Min	Typ	Max		
				Com	Mil	
t_1	$\overline{KAS}$ hold high from KCLK (Note 1)	3.0	-	-	-	ns
t_2	$\overline{KAS}$ setup low to KCLK (Note 1)	3.0	-	-	-	ns
t_3	$\overline{KAS}$ hold low from KCLK (Note 1)	0.0	-	-	-	ns
t_4	$\overline{KAS}$ setup high to KCLK (Note 1)	3.0	-	-	-	ns
t_5	$\overline{KWR}$ setup to $\overline{KDS}$ & $\overline{ACCSEL}$ low	7.0	-	-	-	ns
t_{6A}	$\overline{KWR}$ hold from either $\overline{KDS}$ or $\overline{ACCSEL}$ high	4.4	-	-	-	ns
t_{6B}	$\overline{KWR}$ hold from S4 end	5	-	-	-	ns
t_7	$\overline{KIACK}$ setup to KCLK	10.0	-	-	-	ns
t_8	$\overline{KIACK}$ hold from KCLK	10.0	-	-	-	ns
t_9	Write cycle KADDR setup to KCLK (Note 2)	40.0	-	-	-	ns
t_{10}	Write cycle KADDR hold from KCLK (Note 2)	20.0	-	-	-	ns
t_{11}	KDATA setup to KCLK	20.0	-	-	-	ns
t_{12}	KDATA hold from KCLK	20.0	-	-	-	ns
t_{13}	$\overline{KDSACK0}$ low from SW1 low (Note 6)	4.4	11	23	28	ns
t_{14}	KDATA driven from SW1 (KWR/ high)	4.1	10	17	21	ns
t_{15A}	KDATA valid from $\overline{KDS}$ & $\overline{ACCSEL}$ low	6.5	16	32	39	ns
t_{15B}	KDATA valid from KADDR valid	7.1	17	35	43	ns
t_{16}	KDATA invalid from KADDR change	4.8	9	19	23	ns
t_{17}	KDATA high-z from $\overline{KDS}$ high (Note 7)	3.3	8	16	22	ns
t_{18}	KDATA high-z from $\overline{ACCSEL}$ high (Note 7)	2.9	7	14	20	ns
t_{19}	KDATA high-z from $\overline{KWR}$ low (Note 7)	3.6	9	19	23	ns
t_{20}	$\overline{KDSACK0}$ high from $\overline{KAS}$ high (Note 8)	3.1	8	16	20	ns
t_{22}	$\overline{KDSACK0}$ high from $\overline{ACCSEL}$ high (Note 8)	2.2	6	12	15	ns
t_{23}	$\overline{KDSACK0}$ high-z from KCLK	2.8	7	14	17	ns
t_{24}	$\overline{KBERR}$ low from $\overline{KDS}$ low (Note 9)	511	512	513	513	µs
t_{25}	$\overline{KBERR}$ high from $\overline{KDS}$ high	3.3	8	16	20	ns
t_{26}	$\overline{KBERR}$ high-z from KCLK	3.1	8	18	19	ns
t_{27}	$\overline{TICK}$ negate from KCLK	7	15	31	38	ns

Notes:

1. As detected at ACC pins at applicable logic low or high thresholds.
2. Required for write cycles only; use parameters 15 and 16 for read cycles.
3. Affects wait states inserted by 68020/68030; during write cycles under worst case conditions with a 25 MHz CPU, 2 wait states may be inserted instead of the normal 1 state.
4. $\overline{KDS}$ already low and first wait state SW1 already begun.
5. $\overline{ACCSEL}$ already low and first wait state SW1 already begun.
6. $\overline{ACCSEL}$ and $\overline{KDS}$ already low.
7. First signal to negate will disable data bus drivers.
8. First signal to negate will set $\overline{KDSACK0}$ high.
9. Unless disabled by software.
10. t_{21} is not used.

Figure 7 : REGISTER ACCESS TIMING

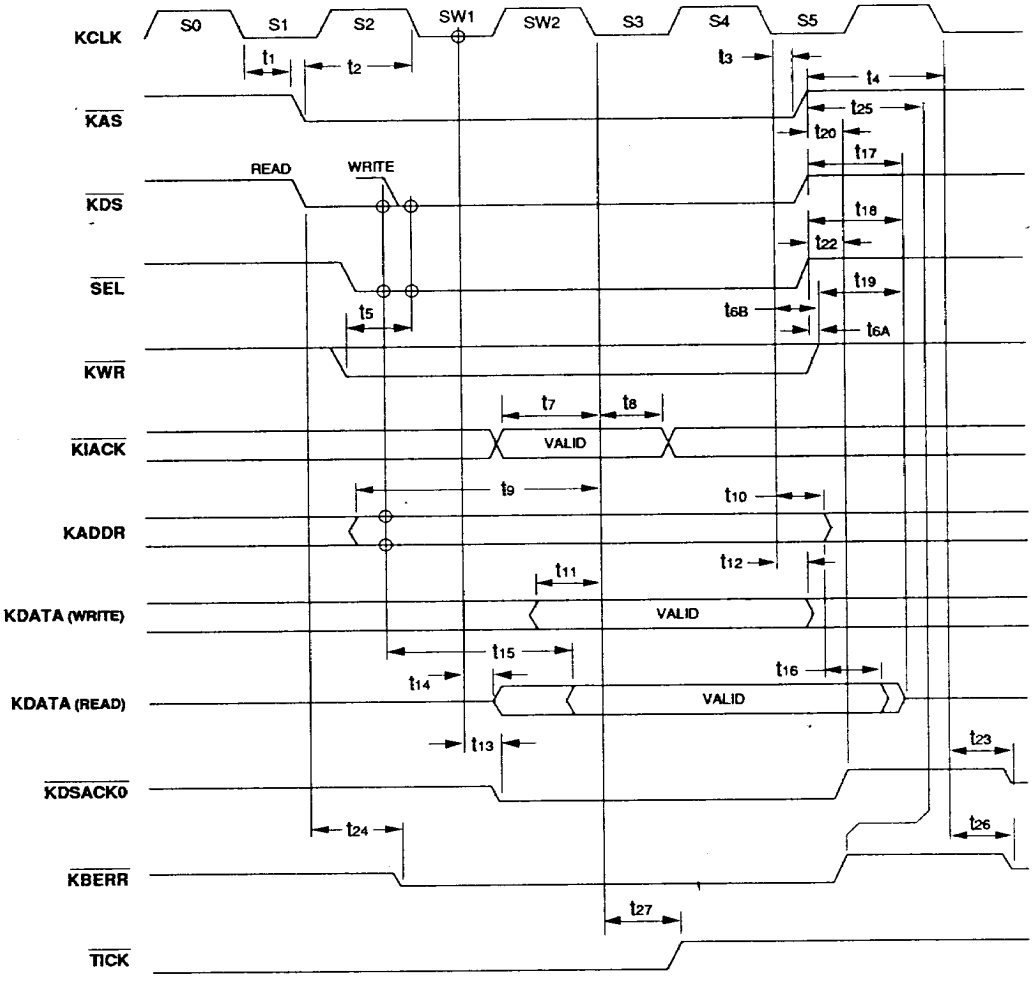
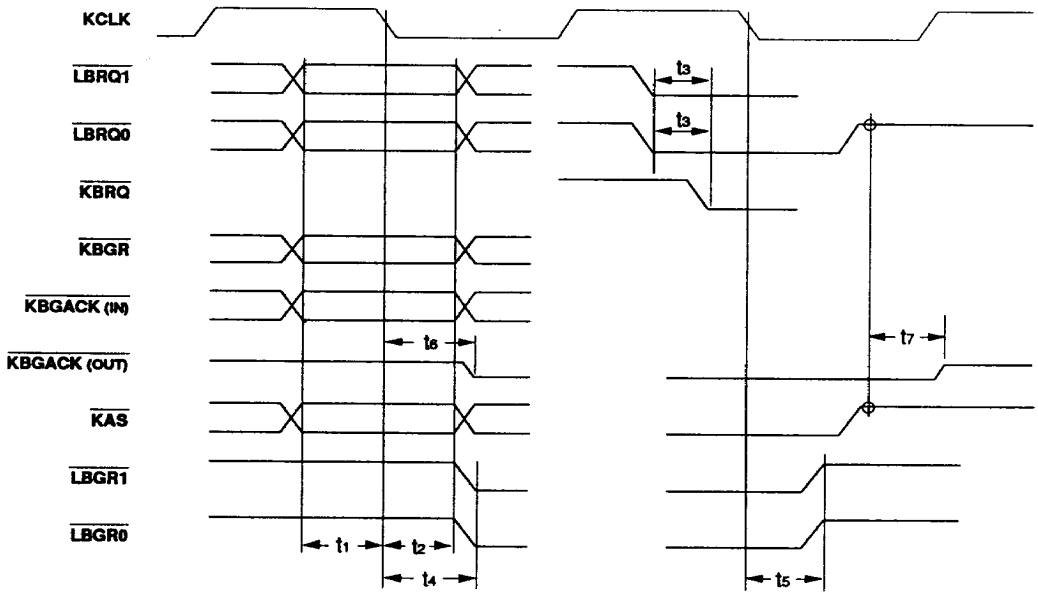


Table 9 : AC CHARACTERISTICS (LOCAL BUS REQUESTER TIMING)
Commercial: T_A = 0° to +70°C, V_{DD} = 5V ± 5%, Military T_A = −55° to +125°C, V_{DD} = 5V ± 10%

Symbol	Description	Limits				Unit
		Min	Typ	Max		
				Com	Mil	
t_1	State variable setup time	15	-	-	-	ns
t_2	State variable hold time	15	-	-	-	ns
t_3	$\overline{LBRQ1}$ or $\overline{LBRQ0}$ to $\overline{KBRQ}$ low	6.3	18	37	45	ns
t_4	KCLK falling edge to $\overline{LBGRn}$ low	5.4	14	27	33	ns
t_5	KCLK falling edge to $\overline{LBGRn}$ high	4.1	11	21	26	ns
t_6	KCLK falling edge to $\overline{KBGACK}$ low (Note 1)	4.9	12	24	30	ns
t_7	$\overline{LBRQ0}$ and $\overline{KAS}$ high to $\overline{KBGACK}$ high-z (Note 1)	3.0	8	16	20	ns

Notes:
1. $\overline{KBGACK}$ is only asserted while device 0 (the DARF) is using the bus; when device 1 is using the bus, the ACC monitors $\overline{KBGACK}$.

Figure 8 : LOCAL BUS REQUESTER TIMING



Note:

Requester state machine transitions will occur if parameters t_1 and t_2 are met. If the signal involved in the present state does not meet parmeters t_1 and t_2, the state transition may or may not occur, but will not fail.

Table 10 : AC CHARACTERISTICS (VMEbus REQUESTER TIMING)
Commercial: T_A = 0° to +70°C, V_{DD} = 5V ± 5%, Military T_A = −55° to +125°C, V_{DD} = 5V ± 10%

Symbol	Description	Limits				Unit
		Min	Typ	Max		
				Com	Mil	
t_1	$\overline{VMERQ}$ setup to C32MHZ rising edge (Note 1)	5.0	-	-	-	ns
t_2	$\overline{VMERQ}$ hold from C32MHZ rising edge (Note 1)	5.0	-	-	-	ns
t_3	$\overline{VMEGR}$ low from C32MHZ rising edge	6.9	17	34	42	ns
t_4	$\overline{VMEGR}$ high from C32MHZ rising edge	5.5	14	27	32	ns
t_5	BRn* low from C32MHZ rising edge (Note 2)	7.2	18	35	43	ns
t_6	BRn* high-z from C32MHZ rising edge (Note 2)	4.9	12	23	28	ns
t_7	BBSY* low from C32MHZ rising edge	8.2	21	41	50	ns
t_8	BBSY* high-z from $\overline{VMERQ}$ rising edge	4.1	10	18	28	ns
t_9	BGnOUT* low from C32MHZ rising edge (Note 2)	4.8	12	23	28	ns
t_{10}	BGnOUT* high from C32MHZ rising edge (Note 2)	4.5	11	22	28	ns
t_{11}	BGnOUT* low from BGnIN* low (Note 3)	3.5	9	19	23	ns
t_{12}	BGnOUT* high from BGnIN* high (Note 3)	3.1	8	15	19	ns

Notes:

1. Meeting parameters 1 and 2 ensure a requester state machine transition on the clock edge shown; otherwise the transition will occur on that edge or the next edge.
2. Applies to the Bus Request and Bus Grant of the level the ACC is configured to use.
3. Applies to the three Bus Grant levels the ACC is not configured to use.

Figure 9 : VMEbus REQUESTER TIMING

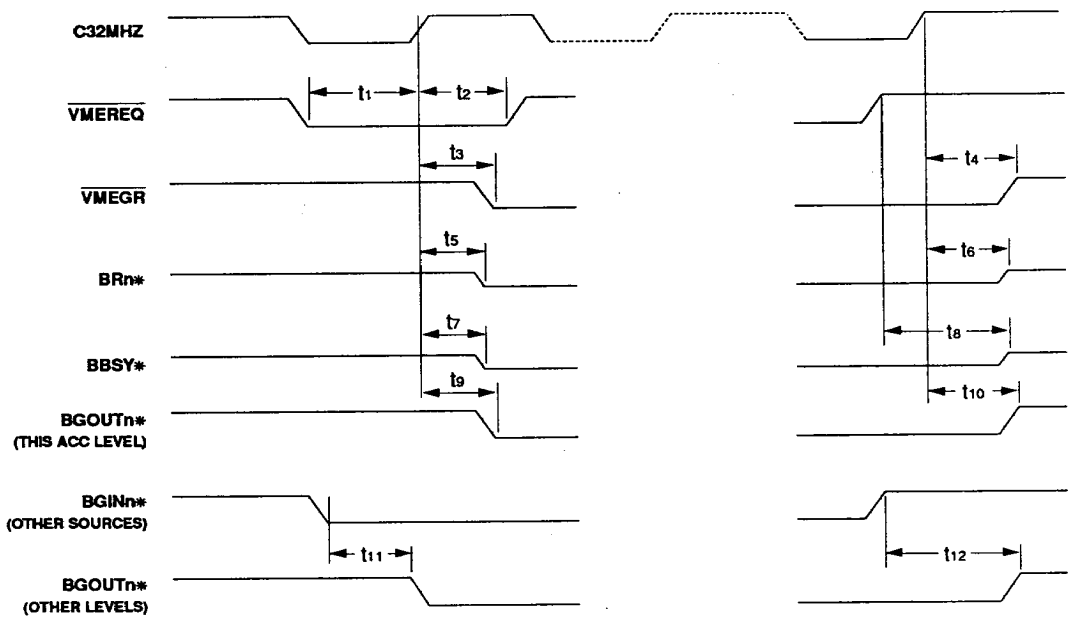


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Table 11 : AC CHARACTERISTICS (VMEbus ARBITER TIMING)
Commercial: T_A = 0° to +70°C, V_{DD} = 5V ± 5%, Military T_A = −55° to +125°C, V_{DD} = 5V ± 10%

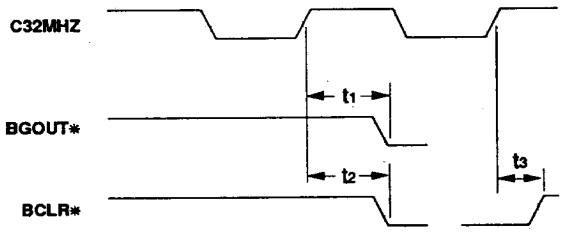
Symbol	Description (Note 1)	Limits				Unit
		Min	Typ	Max		
				Com	Mil	
t_1	BGnOUT* low from C32MHZ rising edge	4.8	13	26	32	ns
t_2	BCLR* low from C32MHZ rising edge	5.7	19	37	45	ns
t_3	BCLR* high from C32MHZ rising edge	5.7	14	28	34	ns
t_4	First DS* low to BERR* asserted	programmable: 16, 32, 64 µs ±1 µs or never				
t_5	Last DS* high to BERR* high impedance	2.6	7	13	16	ns
t_6	BGn* low time	-	-	17	17	µs
t_7	BGn* high timeout recovery time	15	16	17	17	µs

Notes:

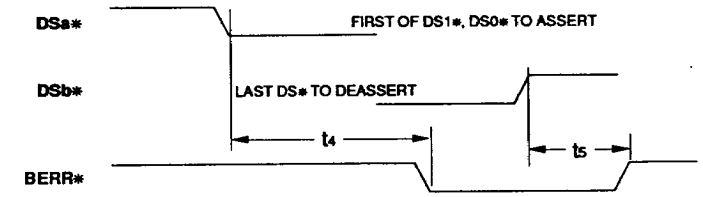
1. Bus Request setup and hold specifications are not provided. The BGn*s are sampled on every C32MHZ rising edge. If a BGn* is not recognized on one edge, it will be recognized on the next edge.

Figure 10 : VMEbus ARBITER TIMING

a) VMEbus Arbiter Signals



b) VMEbus Data Transfer Timeout



c) Arbitration Timeout

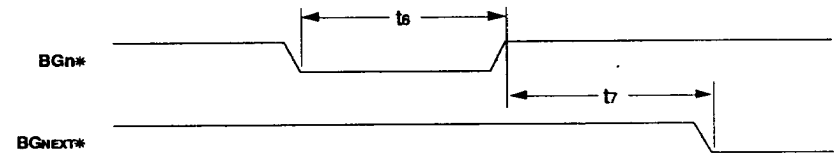


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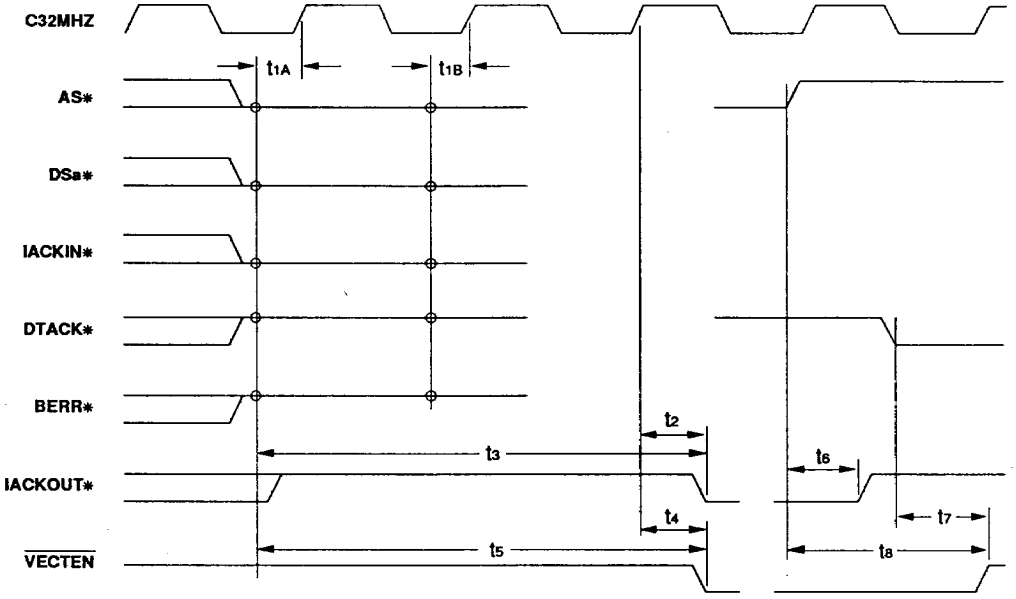
Table 12 : AC CHARACTERISTICS (VMEbus IACK DAISY CHAIN DRIVER TIMING)
Commercial: T_A = 0° to +70°C, V_{DD} = 5V ± 5%, Military T_A = –55° to +125°C, V_{DD} = 5V ± 10%

Symbol	Description	Limits				Unit
		Min	Typ	Max		
				Com	Mil	
t_{1A}	Iack cycle start conditions setup (Note 1)	10.0	-	-	-	ns
t_{1B}	Iack cycle start conditions setup (Note 2)	10.0	-	-	-	ns
t_2	IACKOUT* low from C32MHZ high	4.8	12	23	28	ns
t_3	IACKOUT* from IACK* cycle start	65	84	120	125	ns
t_4	$\overline{\text{VECTEN}}$ low from C32MHZ rising edge	6.2	15	30	37	ns
t_5	$\overline{\text{VECTEN}}$ low from Iack cycle received	69	83	124	131	ns
t_6	IACKOUT* high from AS* high (Note 4)	2.1	6	12	14	ns
t_7	$\overline{\text{VECTEN}}$ high from DTACK* low	3.8	10	19	24	ns
t_8	$\overline{\text{VECTEN}}$ high from AS* high	5.0	13	25	30	ns

Notes:

1. Iack cycle start conditions are: AS* low, either DS1* or DS0* low, IACKIN* low, DTACK* high, and BERR* high. If the setup time is not met, the IACK* cycle start may not be detected on C32MHZ clock edge shown, and would start on the next edge.
2. The Iack cycle start conditions must remain valid on the subsequent edge for the cycle to continue being daisy chained. If the second sample is not valid, two new successive samples are required.
3. Addresses are only required when the ACC is generating an interrupt itself.
4. Applies to all types of Iack cycles, including Auto-ID.

Figure 11 : VMEbus IACK DAISY CHAIN DRIVER TIMING



Note:
Signal timing is the same for both ACC as SYSCON and not SYSCON in Slot 1. IACK is connected to IACK by the backplane.

Table 13 : AC CHARACTERISTICS (VMEbus IACK DAISY CHAIN DRIVER, AUTO-ID CYCLES)
Commercial: T_A = 0° to +70°C, V_{DD} = 5V ± 5%, Military T_A = −55° to +125°C, V_{DD} = 5V ± 10%

Symbol	Description	Limits				Unit
		Min	Typ	Max		
				Com	Mil	
t_1	Iack cycle start conditions setup (Note 1)	10	-	-	-	ns
t_2	Iack cycle start conditions hold (Note 1)	-	-	-	-	ns
t_3	IACKIN* setup to SYSCLK rising edge (Note 2)	-	-	-	-	ns
t_4	IACKOUT* low from SYSCLK rising edge	4.8	12	24	30	ns

Notes:
1. If these conditions are not met, the Auto-ID counter may not start counting on this edge of SYSCLK. The protocol accomodates some modules beginning on a given edge, and others not until the subsequent edge.
2. The module in slot 1 would meet this condition at the same time as condition 1; modules in other slots will wait in state S2 until, one after another, this condition is met. They will then move into S6, finally S4 and generate IACKOUT*.

Figure 12 : VMEbus IACK DAISY CHAIN DRIVER, AUTO-ID CYCLE TIMING

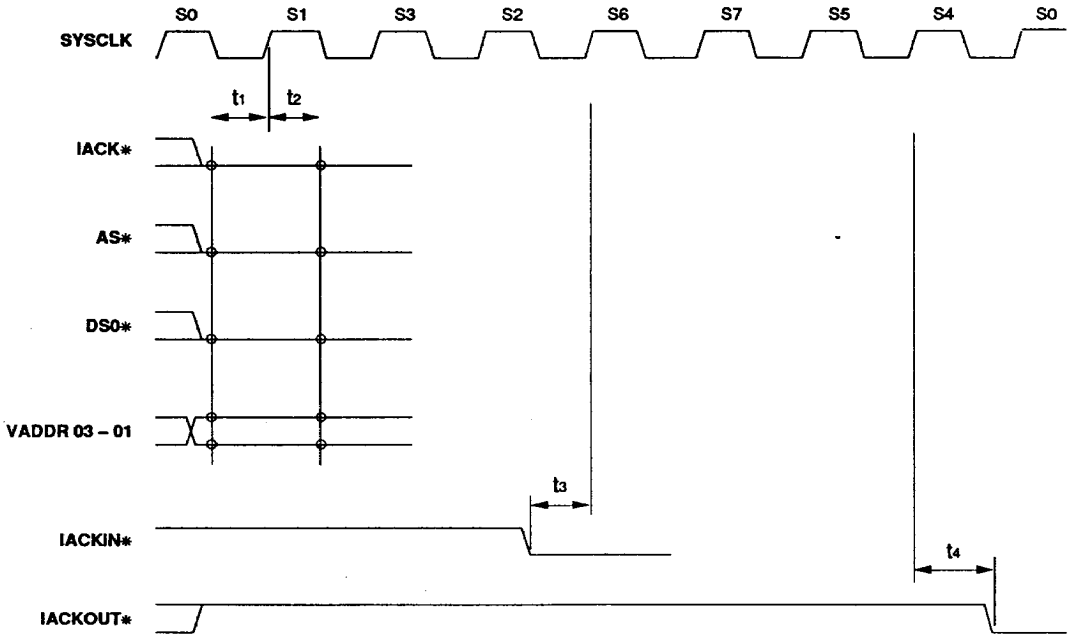


Table 14 : DC CHARACTERISTICS
Commercial: T_A = 0° to +70°C, V_{DD} = 5V ± 5%, Military T_A = –55° to +125°C, V_{DD} = 5V ± 10%

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ	Max	
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$				
	CMOS SCH			1	10	µA
	TTL			1	10	µA
	TTL PD		10	35	120	µA
	TTL PU				40	µA
	TTL SCH			1	10	µA
I_{IL}	Input LOW Current	$V_{IN} = V_{SS}$				
	CMOS SCH			–1	–10	µA
	TTL			–1	–10	µA
	TTL PD				–40	µA
	TTL PU		–8	–30	–100	µA
	TTL SCH			–1	–10	µA
I_{OZ}	Tri-state Output Leakage Current		–10	±1	10	µA
V_{HYST}	Schmitt Trigger Hysteresis					
	CMOS SCH		1.0	1.5		V
	TTL SCH			0.7		V
V_{T+}	Positive-going Schmitt Threshold					
	CMOS SCH			3.0	4.0	V
	TTL SCH			1.7	2.0	V
V_{T-}	Negative-going Schmitt Threshold					
	CMOS SCH		1.0	1.5		V
	TTL SCH		0.8	1.0		V
V_{IH}	Input HIGH voltage					
	TTL	0° to +70°C	2.0			V
	TTL PD	0° to +70°C	2.0			V
	TTL PU	0° to +70°C	2.0			V
	TTL	–55° to +125°C	2.25			V
	TTL PD	–55° to +125°C	2.25			V
	TTL PU	–55° to +125°C	2.25			V
V_{IL}	Input LOW Voltage					
	TTL				0.8	V
	TTL PD				0.8	V
	TTL PU				0.8	V

Table 14 : DC CHARACTERISTICS CON'T

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	Voltage Output HIGH	0° to +70°C				
	TP4	I_{OH} = –4 mA	2.4	4.5		V
	TS6	I_{OH} = –6 mA	2.4	4.5		V
	TP8	I_{OH} = –8 mA	2.4	4.5		V
	TS8	I_{OH} = –8 mA	2.4	4.5		V
	TP12	I_{OH} = –12 mA	2.4	4.5		V
	VTS64	I_{OH} = –22 mA	2.4			V
V_{OH}	Voltage Output HIGH	–55° to 125°C				
	TP4	I_{OH} = –3.2 mA	2.4	4.5		V
	TS6	I_{OH} = –4.8 mA	2.4	4.5		V
	TP8	I_{OH} = –6.4 mA	2.4	4.5		V
	TS8	I_{OH} = –6.4 mA	2.4	4.5		V
	TP12	I_{OH} = –9.6 mA	2.4	4.5		V
	VTS64	I_{OH} = –22 mA	2.4			V
V_{OL}	Voltage Output LOW	0° to +70°C				
	TP4	I_{OL} = 4 mA		0.2	0.4	V
	TS6	I_{OL} = 6 mA		0.2	0.4	V
	OD8	I_{OL} = 8 mA		0.2	0.4	V
	TP8	I_{OL} = 8 mA		0.2	0.4	V
	TS8	I_{OL} = 8 mA		0.2	0.4	V
	TP12	I_{OL} = 12 mA		0.2	0.4	V
	VOD48	I_{OL} = 48 mA			0.6	V
	VTS64	I_{OL} = 64 mA			0.6	V
V_{OL}	Voltage Output LOW	–55° to 125°C				
	TP4	I_{OL} = 3.2 mA		0.2	0.4	V
	TS6	I_{OL} = 4.8 mA		0.2	0.4	V
	OD8	I_{OL} = 6.4 mA		0.2	0.4	V
	TP8	I_{OL} = 6.4 mA		0.2	0.4	V
	TS8	I_{OL} = 6.4 mA		0.2	0.4	V
	TP12	I_{OL} = 9.6 mA		0.2	0.4	V
	VOD48	I_{OL} = 48 mA			0.6	V
	VTS64	I_{OL} = 64 mA			0.6	V

Note that the type abbreviations used above have a number suffix which indicate the current rating. The letter prefixes are defined in the Terminology section, just before Table 3.

Table 15 : CAPACITIVE LOADING

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input Pin Capacitance			10		pF
C_{IO}	Bi-directional Pin Capacitance					
	VOD48			24		pF
	VTS64			32		pF
C_{OUT}	Output Pin Capacitance					
	TP4, TS6, OD8, TP8, TS8, TP12			13		pF

The nominal capacitive load under operating conditions for outputs driving local signals is 50pF; for outputs driving the VMEbus, the rated load is 500pF.

Table 16 : RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage (V_{DD})	+4.5 V to +5.5 V
Power Dissipation (P_{DD})	0.625 W
Ambient Operating Temperature (T_A Commercial)	0° to +70°C
Ambient Operating Temperature (T_A Military)	–55° to +125°C

The power dissipation figure is based on typical internal logic dissipation plus the worst case set of outputs simultaneously active with maximum rated loads.

Table 17 : ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (V_{DD})	–0.3 to +7.0 V
Input Voltage (V_{IN})	–0.3 to V_{DD} +0.3 V
DC Input Current (I_{IN})	–10 to +10 mA
Storage Temperature, ceramic (T_{STG})	–65° to +150°C
Storage Temperature, plastic (T_{STG})	–40° to +125°C

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FUNCTIONAL DESCRIPTION

Reset, Clocks, and BI-mode™ Module

Reset

This module generates the local and VMEbus reset signals, clock signals of several different rates, and contains the local bus timer, tick timer, and watchdog timer. The BI-mode™ controller is also located in this module.

The ACC will assert the local reset ($\overline{RESET}$) signal when any of the power-up reset ($\overline{PWRRST}$), external reset ($\overline{EXTRST}$), or VMEbus system reset (SYSRST*) pins are asserted, or when software initiates a reset via a control register in the ACC.

Clocks: Inputs

The ACC requires two clocks for operation: a constant 32 MHz input to generate clocks of specific frequencies, and the CPU clock for sections that must be synchronous to the CPU. The 1µS, 14µS, 8MHz and SYSCLK (16MHz) signals are exact, within the limits defined by the 32MHz input.

Clocks: Outputs

The ACC provides five clock outputs as described below:

- 1µs — General purpose
- 14µs — General purpose (DRAM refresh clock); ±1 CPU clock
- 14.34ms — General purpose (14µs times 1024)
- 2.4615MHz — Baud clock for serial devices (32MHz divided by 13)
- 8MHz — General purpose
- SYSCLK — SYSCLK for the VMEbus (16MHz)

Tick Clock, Watchdog timer, and Bus Time Out

The ACC provides a tick clock output which can be connected to any of the interrupt inputs and is programmable to one of 200µs, 400µs, 2ms, 4ms, 5ms, 10ms, 50ms or 100 ms. The tick defaults to 100ms. As well as a tick clock the ACC provides a watchdog timer. The watchdog timer, unless restarted, counts out two seconds and then asserts $\overline{WDOG}$ for 200 ms, then begins again. The $\overline{WDOG}$ output can be used for resetting the system or as a source for an interrupt. The local CPU is capable of restarting the watchdog timer via a control bit in the ACC device. The watchdog timer, when used with software, provides a method of detecting when a CPU has stopped functioning. This feature is capable of being disabled via a input pin on the ACC (ENDOG).

The ACC also provides a Local Bus Time Out (LBTO) function. This function asserts the $\overline{KBERR}$ signal when the $\overline{KDS}$ signal has been asserted for 512µs. This provides a method for the CPU to recover if a bad address or device is accessed. This feature can be enabled or disabled under software control (defaults to enabled). The ACC sets a status bit when it asserts $\overline{KBERR}$.

BI-mode™

BI-mode™ entry and exit is controlled by the ACC. The ACC asserts the BI-mode™ pin (BIMODE) on any of the following conditions: local reset, assertion of IRQ1* (programmable), assertion of the SELFBI bit in the ACC device or assertion of $\overline{BITRIG}$ pin. The ACC will only exit BI-mode™ when the $\overline{BIREL}$ signal on the ACC is active and all BI-mode™ entry signals are negated.

Local Bus Requester/Arbiter

The local Bus Requester/Arbiter (LBRA) expands the bus request logic of the 68xxx to handle two sources of requests. The bus request for channel 1 can be programmed to have a higher priority then channel 0. This module receives the two requests from the external sources, obtains the bus from the CPU and passes the grant onto the highest priority device requesting the local bus. The LBRA module uses the standard three wire handshaking to the 68xxx on channel 1, and a modified protocol on channel 0 for the DARF.

Interrupt Handler

The interrupt handler module prioritizes interrupts from dedicated local level 7 sources, general purpose local sources, and the VMEbus. It generates acknowledge signals for the appropriate source when the CPU services an interrupt.

The module also allows each source to be individually enabled, each of the six general purpose sources to be mapped to any of the seven interrupt levels, and the status of any local interrupt to be read.

There are five level seven interrupt inputs of which only four can be disabled. The fifth level seven interrupt is a nonmaskable interrupt.

All of the local interrupt sources are auto-vectored interrupts except that interrupts four and five can be either vectored or auto-vectored. The ACC provides the lack signals for level four and five interrupts when they are programmed as vectored interrupts. The VMEbus interrupts are always handled as vectored interrupts. The priority of acknowledges when there are multiple interrupts on a level is autovectored first, local vectored, then VMEbus interrupts.

The interrupt handler is shown in Figure 13.

VMEbus Requester

The VMEbus Requester obtains ownership of the VMEbus when requested, and can also request that the requesting device (the DARF) cease using the VMEbus when certain conditions exist, such as a Bus Clear or if the programmed ownership period has expired.

Several request and release modes are available and are programmable via the Requester Control Register in the ACC device. The ACC can be programmed to use any of the four VMEbus request levels.

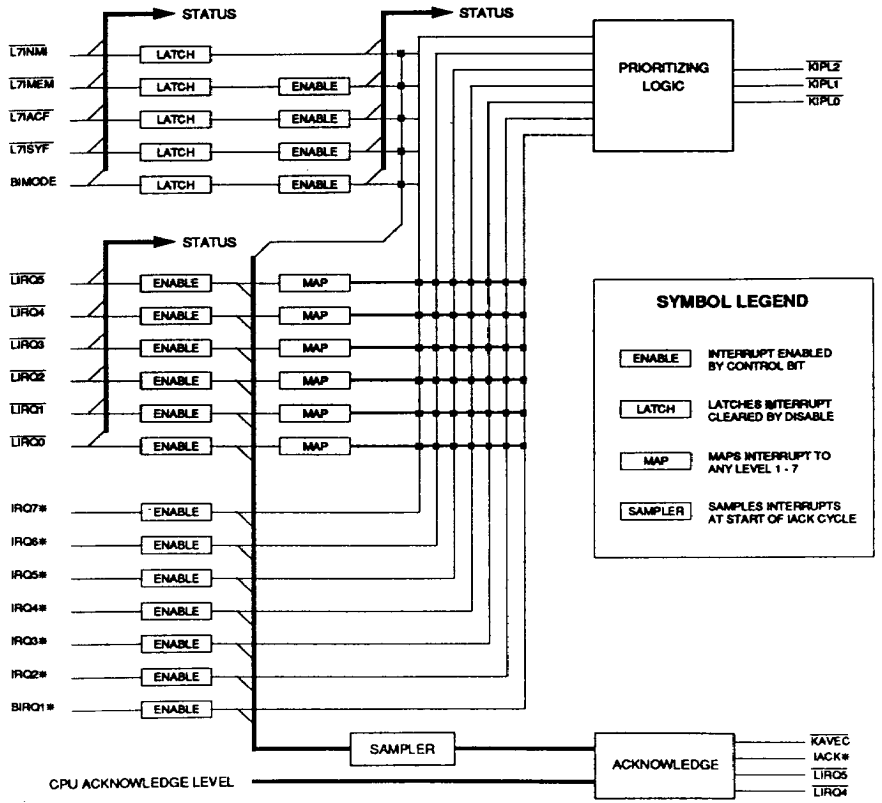


Figure 13 : INTERRUPT HANDLER BLOCK DIAGRAM

Requester Modes

Two request modes are supported: FAIR and DEMAND.

FAIR Mode

In FAIR mode, the ACC does not request the VMEbus until the level that will be used for the request is inactive. This mode ensures that each VME master in a large multi-master VME system will obtain the VMEbus.

DEMAND Mode

In DEMAND mode, the ACC requests the VMEbus regardless of the current state of the VMEbus request lines. This method may prevent other cards on the same bus request level farther down the daisy chain from obtaining the VMEbus, but can be used if the VMEbus is urgently required by this card.

Release Modes

Four release modes are supported by the ACC: Release On Request (ROR), Release When Done (RWD), Release on Bus Clear (ROBCLR), and Release Ownership Timeout (ROTO). The ROR and RWD modes are mutually exclusive, while the ROBCLR and ROTO modes are independently enabled.

Release On Request (ROR)

In ROR mode the ACC requests that the requesting device (eg: DARF) cease using the VMEbus when another VMEbus master asserts its request on the VMEbus. This prevents other VMEbus masters from being starved from the VMEbus, and allows the current VMEbus master to retain bus mastership if no other VMEbus master requires the VMEbus.

Release When Done (RWD)

In RWD mode the ACC gives up the VMEbus when the current cycle is complete. This avoids the *release* overhead of ROR mode.

Release On Bus Clear (ROBCLR)

In ROBCLR mode the ACC requests that the requesting device cease using the VMEbus when the VMEbus Bus Clear (BCLR*) signal is asserted on the VMEbus. The system controller asserts BCLR* when a higher priority request is made while a lower priority request owns the VMEbus. This allows higher priority VMEbus masters to obtain the VMEbus from lower priority VMEbus masters.

Release Ownership Timeout (ROTO)

In ROTO mode the ACC requests that the requesting device cease using the VMEbus after a programmable timeout has expired. The timer can be programmed for 2, 4, or 8 µs or disabled. This mode both limits the time the card owns the VMEbus and, by allowing the card to own the VMEbus for at least that time, it reduces the time spent re-arbitrating the VMEbus.

VMEbus System Controller Functions

VMEbus System Controller functions are provided by the ACC when it is enabled as the System Controller. Internal circuitry detects whether the card is installed at the beginning of the bus grant daisy chain, normally slot 1, at reset and sets the SYSCON mode automatically. Software can also enable or disable the SYSCON mode. The functions that are provided by the ACC as systems controller are listed below:

- Data Transfer Bus Programmable Timeout
- 4 level programmable multi-mode arbiter with timeout
- Iack Daisy Chain Driver
- SYSCLK Generator
- SYSRST* Driver
- Off-card Status Bit Inputs and Reset Input
- $\overline{\text{SYSCON}}$ detection

The system controller functions remain available when the ACC is in BI-mode™.

Data Transfer Bus Programmable Timeout

The ACC provides a timeout circuit, to terminate VMEbus data transfers with bus error (BERR*) signal if no slave responds within a programmed time. The timeout period can be 16, 32 or 64 µs, or *never*.

Four Level VMEbus Arbiter

The arbiter circuitry is enabled whenever the ACC is the system controller, and provides four programmable arbitration schemes along with arbitration timeout.

Arbitration Modes

Four bus arbitration modes are available on the ACC. The arbitration modes are Full Priority, BR3 Priority, BR3,2 Priority and Round Robin Priority. These arbitration modes are software selectable via the ACC device.

Full Priority Mode

While the ACC is in Full Priority mode it issues a bus grant to the highest BR* signal active and assert BCLR* if a lower priority card is using the VMEbus. The priority of the bus request lines are BR3* as the highest to BR0* as the lowest.

BR3 Priority

When the ACC is in BR3 Priority mode the BR3* request has the highest priority and the BR2*, BR1*, and BR0* are placed in round robin mode. BCLR* is asserted due to assertion of BR3*, if required.

BR3, 2 Priority Mode

When the ACC is in BR3,2 Priority mode the BR3*, and BR2* requests are handled in Full Priority mode while BR1* and BR0* are in round robin mode. BCLR* is asserted as required.

Round Robin Mode

When the ACC is in the round robin mode of arbitration, the priority of the request lines is BR3* to BR0*. Once a level has been given a grant a request, it becomes the lowest priority in the chain. For example if BR2* is given a grant the new priority would be: BR3*, BR1*, BR0*, BR2*. BCLR* is not asserted.

IACK Daisy Chain Driver

The IACK Daisy Chain Driver (DCD) circuitry participates in the interrupt acknowledge daisy chain, and either asserts IACKOUT* to the next card on the VMEbus or asserts the VECTEN/ signal to the on-board logic. The VECTEN/ signal indicates to the on-board logic that current acknowledge cycle is for this card.

SYSCLK Generator

The ACC provides a 16 MHZ 50% duty-cycle clock meeting IEEE 1014 when the device is the SYSCON.

SYSRST Driver*

The SYSRST* signal is capable of being driven by the ACC, whether it is the system controller or not. The SYSRST* is asserted when $\overline{\text{PWRRST}}$ is asserted, or while BG0IN* is asserted while the ACC is SYSCON. SYSRST* can also be asserted via a control bit in the ACC regardless of whether the ACC is SYSCON or not. The BG0IN* signal is used as the off-card reset input when the ACC is SYSCON.

Off-Card Status Bit Inputs and Reset Input

The Bus Grant In pins of the card at the beginning of the bus grant daisy chain are not needed by the VMEbus, since the arbiter on that card can drive the local requester directly, instead of via the BGnIN* pins. The use of the BGnIN* pins when the ACC is the SYSCON controller are described below:

BG0IN*	Off-card reset input
BG1IN*	Status input
BG2IN*	Status input
BG3IN*	Used to determine if the card is the system controller

SYSCON Detection

Determining if the card is the system controller is done at reset by sampling the BG3IN* signal. If the card is positioned to the right of another card then the other card is driving the BG3IN* signal inactive (high). If the card is at top of the arbitration chain (SLOT 1) then the BG3IN* line is floating. A 10KΩ external pull-down resistor is required on the BG3IN* signal for SYSCON detection to work. After reset the BG3IN* signal is sampled and depending on the level the ACC can determine if it is the system controller or not.

ACC REGISTERS

The ACC has four address lines (KADDR 00 – KADDR 03) which are used to determine which register is accessed during a CPU access. The 68020/030 processors have an A0 address line last so the four address lines can be mapped directly to the ACC. However the 68000/010 processors do not have this A0 address line so the 68000/010 address lines should be mapped as shown in Table 18, to ensure interrupt acknowledge cycles work correctly.

The ACC registers are summarized in Tables 19 and 20, and more fully described in Tables 21 through 36.

Table 18 : 68000/010 ADDRESS LINE MAP

68000/010	ACC Address Line	68020/030
A4	KADDR 00	A0
A1	VADDR 01	A1
A2	VADDR 02	A2
A3	VADDR 03	A3

Table 19 : ACC Registers

Number	Name	Register Function
F	IC54	Map and autovector bits for local interrupts 5 & 4
E	IC32	Map bits for local interrupts 3 & 2
D	IC10	Map bits for local interrupts 1 & 0
C	VIE	Enable bits for VMEbus interrupts
B	LIE	Enable bits for local general interrupts
A	7IE	Enable bits for dedicated level 7 interrupts
9	LIS	Status bits for local interrupts
8	7IS	Status bits for dedicated level 7 interrupts
7	CTL2	Control and status bits
6	ID	Card ID from Auto-ID
5	VARB	VMEbus Arbiter & Syscon control bits
4	VREQ	VMEbus Requester control bits
3	VINT	VMEbus Interrupter control bits
2	GENCTL	General control bits
1	STAT1	General status bits
0	STAT0	General status bits

Table 20 : ACC REGISTER SUMMARY

Name	#	D7	D6	D5	D4	D3	D2	D1	D0
IC54	F	AVEC|VECT	LIRQ5 Interrupt Level			AVEC|VECT	LIRQ4 Interrupt Level		
IC32	E	(AVEC)	LIRQ3 Interrupt Level			(AVEC)	LIRQ2 Interrupt Level		
IC10	D	(AVEC)	LIRQ1 Interrupt Level			(AVEC)	LIRQ0 Interrupt Level		
VIE	C	Not Used	IRQ7 Enable	IRQ6 Enable	IRQ5 Enable	IRQ4 Enable	IRQ3 Enable	IRQ2 Enable	IRQ1 Enable
LIE	B	Not Used	Not Used	LIRQ5 Enable	LIRQ4 Enable	LIRQ3 Enable	LIRQ2 Enable	LIRQ1 Enable	LIRQ0 Enable
7IE	A	Not Used	Not Used	Not Used	BI-mode Int Enable	L7ISYF Pin Int Enable	L7IACF Pin Int Enable	L7IMEM Pin Int Enable	L7INMI Pin Int Enable
LIS	9	Not Used	Not Used	LIRQ5 Pin Status	LIRQ4 Pin Status	LIRQ3 Pin Status	LIRQ2 Pin Status	LIRQ1 Pin Status	LIRQ0 Pin Status
7IS	8	Not Used	Not Used	Not Used	BI-mode Int Status	L7ISYF Int Status	L7IACF Int Status	L7IMEM Int Status	L7INMI Int Status
CTL2	7	Not Used	Not Used	MYBBSY Status	BITRIG Pin Status	Not Used	LBRAM Pri 1/Fair	MEMIM VME Ctl	TICKM Fast, Norm
ID	6	Eight bit card slot id from Auto-ID cycle							
VARB	5	Not Used	Not Used	Data Transfer Timeout 0–3: Never, 16, 32, 64 µs		Not Used	Arbitration Timeout Enable	Arbitration Mode 0–3: RR, P3RR210, P32RR10, PRI	
VREQ	4	Ownership Timeout Enable	Bus Clear Recognition Enable	Bus Release 0 On request 1 When done	Bus Request 0 Fair 1 Demand	Ownership Timer 0: zero 1: 2 µs 2: 4 µs 3: 8 µs		Bus Request Level	
VINT	3	Not Used	Not Used	Not Used	Not Used	Interrupt On	Interrupt Level 0–7		
GENCTL	2	Software Reset	Assert IRQ1*	Self BI-mode	Tick Period 0–3: 200, 400µs, 2, 4ms 5, 10, 50, 100 ms		Local Bus Timeout Enable	Auto-ID Counter Test	IRQ1* Mode 0: Interrupt 1: BI-mode
STAT1	1	REV B	Not Used	SYSCON	BI-mode	Powered Up	Auto-ID done	BG2IN* Pin	BG1IN* Pin
STAT0	0	Restart Watchdog	Clear Tick	Local Bus Timed Out	IRQ1* Pin State	L7ISYF Pin State	L7IACF Pin State	L7IMEM Pin State	L7INMI Pin State

Notes:

1. All signals are active high, including interrupt pin status.
2. If the value read from a register is different from the value written to, or stored in the register, then read and write values are individually described. Otherwise, no distinction is made. Bits that are not used are also defined, and may be used in future versions of the ACC. To maximize future firmware compatibility, it is recommended that unused bits be set to zero when writing to such registers.
3. Values written to read only bits have no effect. However, it is recommended that these bits be set to zero when writing data to such registers, again to ensure future compatibility.

Table 21 : STATUS REGISTER 0

Register Name: STAT0	Register Number: 0

D7	D6	D5	D4	D3	D2	D1	D0
CLRDOG	CLRTIK	LTO	VI1	SYFIP	ACFIP	MEMIP	NMIIP

Name	Type	Condition after Reset	State	Function
CLRDOG	R/W	0		Watchdog clear and restart
			0	No effect
			1	if 0 before write, resets; if 1 before write, no effect
CLRTIK	R/W	0		Clear TICK signal
			R	Always reads as zero
			W 0	TICK pin cleared to high
			W 1	No effect
LTO	R/W	0		Local Bus Timed Out flag
			R 0	No timeout has occurred
			R 1	Local bus timeout occurred
			W 0	Clears LTO bit to zero
			W 1	No effect
VI1	R	-		VMEbus IRQ1* (BI-mode™ line)
			0	IRQ1* is not asserted
			1	IRQ1* is asserted
SYFIP	R	-		$\overline{\text{L7ISYF}}$ Interrupt Pin
			0	Pin is not asserted
			1	Pin is asserted
ACFIP	R	-		$\overline{\text{L7IACF}}$ Interrupt Pin
			0	Pin is not asserted
			1	Pin is asserted
MEMIP	R	-		$\overline{\text{L7IMEM}}$ Interrupt Pin
			0	Pin is not asserted
			1	Pin is asserted
NMIIP	R	-		$\overline{\text{L7INMI}}$ Interrupt Pin
			0	Pin is not asserted
			1	Pin is asserted

Table 22 : STATUS REGISTER 1

Register Name: STAT1	Register Number: 1

D7	D6	D5	D4	D3	D2	D1	D0
REV B	0	SYSC	BI	PWRUP	IDGOT	BG2IN	BG1IN

Name	Type	Condition after Reset	State	Function
REV B	R	1		Indicates a Revision B ACC device
SYSC	R/W	-		VMEbus SYSCON mode bit
			0	ACC is not SYSCON
			1	ACC is SYSCON
BI	R	1		BI-mode™ Indicator
			0	ACC is not in BI-mode™
			1	ACC is in BI-mode™
PWRUP	R	-		Power-up indicator
			0	Last reset was not by power up
			1	Last reset was due to power up
IDGOT	R	-		Auto-ID Completion indicator
			0	Auto-ID cycle not done yet
			1	Auto-ID cycle completed
BG2IN	R	-		Bus Grant 2 In pin
			0	BG2IN* is low or ACC isn't SYSCON
			1	BG2IN* is high and ACC is SYSCON
BG1IN	R	-		Bus Grant 1 In pin
			0	BG1IN* is low or ACC isn't SYSCON
			1	BG1IN* is high and ACC is SYSCON

Table 23 : GENERAL CONTROL REGISTER

Register Name: GENCTL	Register Number: 2

D7	D6	D5	D4	D3	D2	D1	D0
SWRST	ABI	SBI	TLEN1	TLEN0	LTOEN	IDTST	VI1BI

Name	Type	Condition after Reset	State	Function
SWRST	R/W	0		Software Initiated System Reset
			0	No effect
			1	Initiates reset
ABI	R/W	0		Assert BI-mode™ line (IRQ1*)
			0	De-assert IRQ1*
			1	Assert IRQ1*
SBI	R/W	0		Self BI-mode™ control bit
			0	De-assert self BI-mode™ control
			1	Set self into BI-mode™
TLEN1 TLEN0	R/W	3		Tick timer length code Norm Fast
			0	5 ms 200 µs
			1	10 ms 400 µs
			2	50 ms 2 ms
			3	100 ms 4 ms
LTOEN	R/W	1		Local Bus Timeout Enable
			0	Disable timeout
			1	Enable timeout
IDTST	R/W	0		Auto-ID Test Bit
			W 0	No effect
			W 1	If previously 0, increment ID
			W 1	If previously 1, no effect
VI1BI	R/W	1		IRQ1* Configuration Control Bit
			0	IRQ1* as interrupt only
			1	IRQ1* as BI-mode™ line only

Table 24 : VMEbus INTERRUPTER REGISTER

Register Name: VINT	Register Number: 3

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	INT	IL2	IL1	IL0

Name	Type	Condition after Reset	State	Function
INT	R/W	0		Interrupt Control and Status bit
			R 0	No interrupt is pending
			R 1	Interrupt is presently asserted
			W 0	No effect; does not change to 0
			W 1	Assert interrupt
IL2 IL1 IL0	R/W	0	 0 1–7	Interrupt Level Interrupter clears itself Sets interrupt level

Table 25 : VMEbus REQUESTER REGISTER

Register Name: VREQ	Register Number: 4

D7	D6	D5	D4	D3	D2	D1	D0
OTEN	BCEN	REL	REQ	OT1	OT0	LVL1	LVL0

Name	Type	Condition after Reset	State	Function
OTEN	R/W	1		VMEbus Ownership Timer Enable
			0	Disable timer
			1	Enable timer
BCEN	R/W	0		Bus Clear Recognition Control
			0	Ignore BCLR* signal
			1	Release bus if BCLR* asserted
REL	R/W	1		VMEbus Release Mode Control
			0	Release on request (ROR)
			1	Release when done (RWD)
REQ	R/W	1		VMEbus Request Mode Control
			0	Fair
			1	Demand
OT1 OT0	R/W	3		VMEbus Ownership Timer (Timeout Period)
			0	Zero
			1	2 µs
			2	4 µs
			3	8 µs
LVL1 LVL0	R/W	3		VMEbus Request Level
			0	Level 0
			1	Level 1
			2	Level 2
			3	Level 3

Table 26 : VMEbus ARBITER REGISTER

Register Name: VARB							Register Number: 5
D7	D6	D5	D4	D3	D2	D1	D0
0	0	VXL1	VXL0	0	ATEN	ARB1	ARB0

Name	Type	Condition after Reset	State	Function
VXL1 VXL0	R/W	3		Data Transfer Timeout Period
			0	Never
			1	16 µs
			2	32 µs
			3	64 µs
ATEN	R/W	1		Arbitration Timeout Enable
			0	Disable arbitration timeout
			1	Enable arbitration timeout
ARB1 ARB0	R/W	0		Arbitration Mode
			0	Round Robin all four levels
			1	Priority 3, Round Robin 2, 1, 0
			2	Priority 3, 2, Round Robin 1, 0
			3	Priority on all four levels

Table 27 : ID REGISTER

Register Name: ID							Register Number: 6
D7	D6	D5	D4	D3	D2	D1	D0
ID7	ID6	ID5	ID4	ID3	ID 2	ID1	ID0

Name	Type	Condition after Reset	State	Function
ID	R	0		Auto-ID Card Slot ID
			n	Value of ID counter

Table 28 : LEVEL 7 INTERRUPT STATUS REGISTER

Register Name: 7IS	Register Number: 8

D7	D6	D5	D4	D3	D2	D1	D0
0	0	MYBBSY	BITRIG	0	LRAM	MEMIM	TICKM

Name	Type	Condition after Reset	State	Function
MYBBSY	R	0		ACC BBSY* Output
			0	BBSY* is not asserted
			1	BBSY* is driven low
BITRIG	R	-		State of $\overline{\text{BITRIG}}$ Pin
			0	Pin is not asserted
			1	Pin is asserted
LBRAM	R/W	0		Local Bus Requester Mode
			0	Channels 0 and 1 fair
			1	Channel 1 pre-empts channel 0
MEMIM	R/W	1		L7IMEM Effect on Requester
			0	L7IMEM does not affect Requester
			1	L7IMEM assertion forces Requester to release VMEbus
TICKM	R/W	0		Tick Speed
			0	Normal rates
			1	Fast rates

Table 29 : LEVEL 7 INTERRUPT STATUS REGISTER

Register Name: 7IS	Register Number: 8

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	BI	SYFIS	ACFIS	MEMIS	NMIIS

Name	Type	Condition after Reset	State	Function
BI	R/W	0		BI-mode™ Interrupt
			0	Interrupt is not asserted
			1	Interrupt is asserted
SYFIS	R/W	0		$\overline{\text{L7ISYF}}$ Pin Interrupt
			0	Interrupt is not asserted
			1	Interrupt is asserted
ACFIS	R/W	0		$\overline{\text{L7IACF}}$ Pin Interrupt
			0	Interrupt is not asserted
			1	Interrupt is asserted
MEMIS	R/W	0		$\overline{\text{L7IMEM}}$ Pin Interrupt
			0	Interrupt is not asserted
			1	Interrupt is asserted
NMIIS	R/W	Note 1		$\overline{\text{L7INMI}}$ Pin Interrupt
			0	Interrupt is not asserted
			1	Interrupt is asserted

Note 1: The bits in this status register represent the current state of the interrupt latches corresponding to the five interrupts. The interrupt inputs themselves can be read through Status Register 0. The initial state of NMIIS is dependent on the circuit card design.

Table 30 : LOCAL INTERRUPT STATUS REGISTER

Register Name: LIS	Register Number: 9

D7	D6	D5	D4	D3	D2	D1	D0
0	0	LI5	LI4	LI3	LI2	LI1	LI0

Name	Type	Condition after Reset	State	Function
LI5	R/W	0		Local Interrupt Five ($\overline{\text{LIRQ5}}$)
			0	$\overline{\text{LIRQ5}}$ pin is not asserted
			1	Interrupt pin is asserted
LI4	R/W	0		Local Interrupt Four ($\overline{\text{LIRQ4}}$)
			0	$\overline{\text{LIRQ4}}$ pin is not asserted
			1	Interrupt pin is asserted
LI3	R/W	0		Local Interrupt Three ($\overline{\text{LIRQ3}}$)
			0	$\overline{\text{LIRQ3}}$ pin is not asserted
			1	Interrupt pin is asserted
LI2	R/W	0		Local Interrupt Two ($\overline{\text{LIRQ2}}$)
			0	$\overline{\text{LIRQ2}}$ pin is not asserted
			1	Interrupt pin is asserted
LI1	R/W	0		Local Interrupt One ($\overline{\text{LIRQ1}}$)
			0	$\overline{\text{LIRQ1}}$ pin is not asserted
			1	Interrupt pin is asserted
LI0	R/W	0		Local Interrupt Zero ($\overline{\text{LIRQ0}}$)
			0	$\overline{\text{LIRQ0}}$ pin is not asserted
			1	Interrupt pin is asserted

Table 31 : LEVEL 7 INTERRUPT ENABLE REGISTER

Register Name: 7IE	Register Number: A hex

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	BIE	SYFIE	ACFIE	MEMIE	NMIIE

Name	Type	Condition after Reset	State	Function
BIE	R/W	0		BI-mode™ Interrupt Enable
			0	Disable interrupt
			1	Enable interrupt
SYFIE	R/W	0		$\overline{\text{L7ISYF}}$ Pin Interrupt Enable
			0	Disable interrupt
			1	Enable interrupt
ACFIE	R/W	0		$\overline{\text{L7IACF}}$ Pin Interrupt Enable
			0	Disable interrupt
			1	Enable interrupt
MEMIE	R/W	0		$\overline{\text{L7IMEM}}$ Pin Interrupt Enable
			0	Disable interrupt
			1	Enable interrupt
NMIIE	R/W	1		$\overline{\text{L7INMI}}$ Pin Interrupt Clear
			R	Always reads one
			W 0	Clear interrupt; remains enabled
			W 1	No effect; always enabled

4

Table 32 : LOCAL INTERRUPT ENABLE REGISTER

Register Name: LIE	Register Number: B hex

D7	D6	D5	D4	D3	D2	D1	D0
0	0	L5E	L4E	L3E	L2E	L1E	L0E

Name	Type	Condition after Reset	State	Function
L5E	R/W	0		Local Interrupt 5 ($\overline{\text{LIRQ5}}$) Enable
			0	Disable interrupt
			1	Enable interrupt
L4E	R/W	0		Local Interrupt 4 ($\overline{\text{LIRQ4}}$) Enable
			0	Disable interrupt
			1	Enable interrupt
L3E	R/W	0		Local Interrupt 3 ($\overline{\text{LIRQ3}}$) Enable
			0	Disable interrupt
			1	Enable interrupt
L2E	R/W	0		Local Interrupt 2 ($\overline{\text{LIRQ2}}$) Enable
			0	Disable interrupt
			1	Enable interrupt
L1E	R/W	0		Local Interrupt 1 ($\overline{\text{LIRQ1}}$) Enable
			0	Disable interrupt
			1	Enable interrupt
L0E	R/W	0		Local Interrupt 0 ($\overline{\text{LIRQ0}}$) Enable
			0	Disable interrupt
			1	Enable interrupt

Table 33 : VMEbus INTERRUPT ENABLE REGISTER

Register Name: VIE	Register Number: C hex

D7	D6	D5	D4	D3	D2	D1	D0
0	V7E	V6E	V5E	V4E	V3E	V2E	V1E

Name	Type	Condition after Reset	State	Function
V7E	R/W	0		VMEbus Interrupt 7 Enable
			0	Interrupt disabled
			1	Interrupt enabled
V6E	R/W	0		VMEbus Interrupt 6 Enable
			0	Interrupt disabled
			1	Interrupt enabled
V5E	R/W	0		VMEbus Interrupt 5 Enable
			0	Interrupt disabled
			1	Interrupt enabled
V4E	R/W	0		VMEbus Interrupt 4 Enable
			0	Interrupt disabled
			1	Interrupt enabled
V3E	R/W	0		VMEbus Interrupt 3 Enable
			0	Interrupt disabled
			1	Interrupt enabled
V2E	R/W	0		VMEbus Interrupt 2 Enable
			0	Interrupt disabled
			1	Interrupt enabled
V1E	R/W	0		VMEbus Interrupt 1 Enable
			0	Interrupt disabled
			1	Interrupt enabled

Table 34 : LOCAL INTERRUPTS 1 and 0 CONTROL REGISTER

Register Name: IC10 **Register Number: D hex**

D7	D6	D5	D4	D3	D2	D1	D0
1	1L2	1L1	1L0	1	0L2	0L1	0L0

Name	Type	Condition after Reset	State	Function
1L2	R/W	0		Local Interrupt 1 ($\overline{\text{LIRQ1}}$) Level
1L1			0	Masks interrupt
1L0			1–7	Maps pin to level 1–7
0L2	R/W	0		Local Interrupt 0 ($\overline{\text{LIRQ0}}$) Level
0L1			0	Masks interrupt
0L0			1–7	Maps pin to level 1–7

Table 35 : LOCAL INTERRUPTS 3 and 2 CONTROL REGISTER

Register Name: IC32 **Register Number: E hex**

D7	D6	D5	D4	D3	D2	D1	D0
1	3L2	3L1	3L0	1	2L2	2L1	2L0

Name	Type	Condition after Reset	State	Function
3L2	R/W	0		Local Interrupt 3 ($\overline{\text{LIRQ3}}$) Level
3L1			0	Masks interrrupt
3L0			1–7	Maps pin to level 1–7
2L2	R/W	0		Local Interrupt 2 ($\overline{\text{LIRQ2}}$) Level
2L1			0	Masks interrrupt
2L0			1–7	Maps pin to level 1–7

Table 36 : LOCAL INTERRUPTS 5 and 4 CONTROL REGISTER

Register Name: IC54	Register Number: F hex

D7	D6	D5	D4	D3	D2	D1	D0
5AV	5L2	5L1	5L0	4AV	4L2	4L1	4L0

Name	Type	Condition after Reset	State	Function
5AV	RW	1		Local Interrupt 5 ($\overline{\text{LIRQ5}}$) Vector
			0	Vectored
			1	Autovectored
5L2 5L1 5L0	R/W	0	 0 1–7	Local Interrupt 5 ($\overline{\text{LIRQ5}}$) Level Masks interrupt Maps pin to level 1–7
4AV	R/W	1		Local Interrupt 4 ($\overline{\text{LIRQ4}}$) Vector
			0	Vectored
			1	Autovectored
4L2 4L1 4L0	R/W	0	 0 1–7	Local Interrupt 4 ($\overline{\text{LIRQ4}}$) Level Masks interrupt Maps pin to level 1–7

DARF CONNECTIONS

The ACC signals that connect to the DARF are listed in Table 37.

In addition to using these signals, the DARF will connect to any two of the ACC local auto-vectored interrupt inputs, except for $\overline{\text{LIRQ5}}$, $\overline{\text{LIRQ4}}$, $\overline{\text{L7INMI}}$, and $\overline{\text{L7IMEM}}$. The DARF uses the two interrupts to signal location monitor accesses and general DARF service requests.

Other common signals such as local address strobe ($\overline{\text{KAS}}$), local CPU clock (KCLK), local reset ($\overline{\text{RESET}}$), and others would connect to both devices.

Table 37 : ACC to DARF Connections

ACC Signal	Pin	DARF Signal	Pin
BIMODE	B7	BIMODE	P6
$\overline{\text{BIREL}}$	Q11	$\overline{\text{BIREL}}$	S17
$\overline{\text{LBGR0}}$	Q7	$\overline{\text{LBGR}}$	M15
$\overline{\text{LBRQ0}}$	N10	$\overline{\text{LBRQ}}$	R14
$\overline{\text{VECTEN}}$	P8	$\overline{\text{VECTEN}}$	P13
$\overline{\text{VIACKRQ}}$	Q8	$\overline{\text{VIACKRQ}}$	N15
$\overline{\text{VMEGR}}$	N8	$\overline{\text{VMEGR}}$	L15
$\overline{\text{VMERQ}}$	P11	$\overline{\text{VMERQ}}$	M17

APPLICATION NOTES

Recommendations and requirements for using the ACC in the design of VMEbus cards are highlighted below. For more information on the operation and use of this device, please refer to the *AVICS Technical Manual.*

VMEbus Connection

The ACC is designed to connect directly to the VMEbus, without any intervening buffers. All outputs that drive the bus have the appropriate drive capability, such as 8 mA for daisy chain signals, and 48 and 64 mA drivers that meet the IEEE 1014 VMEbus spec over the full military operating temperature range.

ACC signals that connect to the bus have been located on the pin grid array package to provide a one-to-one correspondence of pins and practically eliminate PC trace cross overs. To support this, the ACC should be located towards the pin 1 end of the P1 connector, with column 15 of the pins closest to and parallel to P1. The VMEbus two inch signal length rules allow enough room for a row of buffer ICs between the ACC and P1, for address and data lines.

Internal Signals

The relationship between $\overline{KAS}$ and KCLK is critical at the start of an access to the ACC, or an interrupt acknowledge cycle. The ACC samples $\overline{KAS}$ with KCLK to determine the start of CPU cycles (the end of S2 is located); if $\overline{KAS}$ goes low at the ACC sooner than the margin shown in the timing specifications, then hold time at internal flip flops is not assured. The 68020 and 68030 provide 3 ns delay in generating $\overline{KAS}$ from KCLK; signal distortion or skew must not reduce this, nor are buffers allowed between the CPU CLK and AS* pins and the ACC KCLK and $\overline{KAS}$ pins.

Bus Grant In Signals

The four BGnIN* signals have integral termination resistors of between 40KΩ and 140KΩ. These are sufficient to protect against floating inputs. BG3IN* has a pull-down resistor, while BG2IN* through BG0IN* have pull-up resistors.

In application, BG3IN* requires an external pull down resistor to support the automatic Syscon determination, and BG0IN* requires a pull-up resistor, since that input becomes the off-card reset input. BG2IN* and BG1IN* should also be terminated, if they are going to be used as status inputs. A value of 10KΩ is recommended for each resistor.

The input loading generated by internal and external termination resistors exceeds the I_{IH} limits specified in rule 6.20 of the IEEE 1014 specication, but is within the capability of the driver specified on the preceding card.

Reset via the Watchdog

A typical use of a watchdog is to reset the card or system when a timeout occurs.

To assert local reset, the watchdog output connects to the $\overline{EXTRST}$ pin of the ACC. Local reset is then asserted for 450ms at timeout (watchdog 200ms + ACC 250ms reset timer).

Asserting SYSRST* requires a 48 mA driver for the watchdog. The watchdog output must not be connected to the $\overline{PWRRST}$ pin, since this pin also clears the watchdog, resulting in an undefined WDOG/ low time.

Power Reset Pin R-C Network

The $\overline{PWRRST}$ pin completely initializes the ACC, and must be used after power is applied; asserting SYSRESET* from another source is not sufficient. The $\overline{PWRRST}$ pin only needs to be asserted for 50ns after supply voltage V_{DD} comes within operating specification. After $\overline{PWRRST}$ is released, the internal reset generator will maintain $\overline{RESET}$ and SYSRST* for another 250ms.

Factors to consider in selecting the resistor and capacitor values for the reset network are the worst case logic high threshold of 4.0 V, the 10 µA leakage current on the $\overline{PWRRST}$ pin, and the capacitor leakage current. Recommended values are a 10µF tantalum capacitor, 22KΩ pull-up resistor and IN4001 discharge diode.

Expansion of Local Bus Request Channel 1

Either channel of the local bus requester can be expanded to handle requests from multiple devices. This would be done with external logic, providing a second level of request and grant arbitration, interfacing to the ACC via the request and grant signal for one channel, and the $\overline{KBGACK}$ signal.