CALMOS™ AUGUST 1991 **CA91C064**

# VMEbus 64–BIT DATA ADDRESS REGISTER FILE (DARF64)

- 64-bit Data/Address Register File (DARF64)
- Pin compatible with CA91C015 DARF32
- IEEE-1014/VMEbus Rev D compatible
- Full master/slave A64/D64, A32, A24/D32, D16, D08(EO) interface
- Master A16/D16, D08(EO) capabilities
- High performance bus bandwidth:
  - 30 MB/s - Standard cycles
  - 35 MB/s - BLT Mode
  - 70 MB/s - MBLT Mode
- 15 x 64 bit wide transmit and receive decoupling FIFOs
- Direct connection with 68020/030
- Support for 68040 and RISC processors
- Location monitor with 31 deep message FIFO for inter-process communication
- 68030 like local bus burst mode
- Programmable
  - Atomic and decoupled modes
  - A64 master and slave base address
  - A32 slave image base address and size
  - A24 slave image base address and size
  - Slave image access protection
  - VMEbus/VSB routing
- Integral A64,A32,A24/D64,D32,D16 DMAC
  - DMAC initiated read or write cycles
  - Discrete, block, multiplexed block transfers
  - Up to 4 megabyte block length
  - Automatic address phase insertion
- Bi-mode®: bus isolation mode
- Low power CMOS implementation
- Card and system testability support
- 224 pin PGA and CLDCC packages
- Commercial, military temperature and MIL-STD-883 processed versions

The CA91C064 DARF64 provides a complete high performance VMEbus 64 data transfer interface, including high level functions such as a DMA Controller and a Location Monitor with associated message FIFO.

Transmit and Receive FIFOs are used to decouple read and write cycles between the local bus and the VMEbus using a store-and-forward technique, thereby overlapping bus access and response delays with other data transfer activity. Read-modify-write cycles are always performed using atomic mode only, after any write cycles pending in the FIFO have been transferred. The decoupling FIFOs and specialized bus interfaces in the CA91C064 allow data transfer rates up to 70 MB/s to be sustained for the duration of blocks transferred by the DMA. A burst mode is provided on the local bus to support this data rate.

Address maps, slave image characteristics such as size and access protection and DARF64 and DMAC operating modes are all programmed through twenty internal registers. Eight of the registers assist card and system level diagnostics and the recovery of any data transfers that fail. A CONFIGURATION ERROR flag is also provided, which generates an interrupt when incompatible operating modes are selected.

The integral DMAC can transfer data between local memory and the VMEbus in either direction, using discrete, block or multiplexed block (64 bit data mode) mode. The DMAC can be programmed for up to a 4 megabyte block length and can insert addressing phases when necessary.

The CA91C064 is one of four components in the Newbridge Microsystems *VMEbus Family of Chip Sets*. The other three are the CA91C010 MSC, CA91C014 ACC and CA91C015 DARF32. The CA91C014 ACC provides service functions such as a VMEbus requester, and interrupt handlers. The CA91C010 and CA91C015 provide the address and data path VMEbus master and slave functions.

The CA91C064 DARF64 and CA91C014 ACC, buffers for the DARF64 VMEbus address, data and control signals, plus two delay line modules provide a complete VMEbus interface.

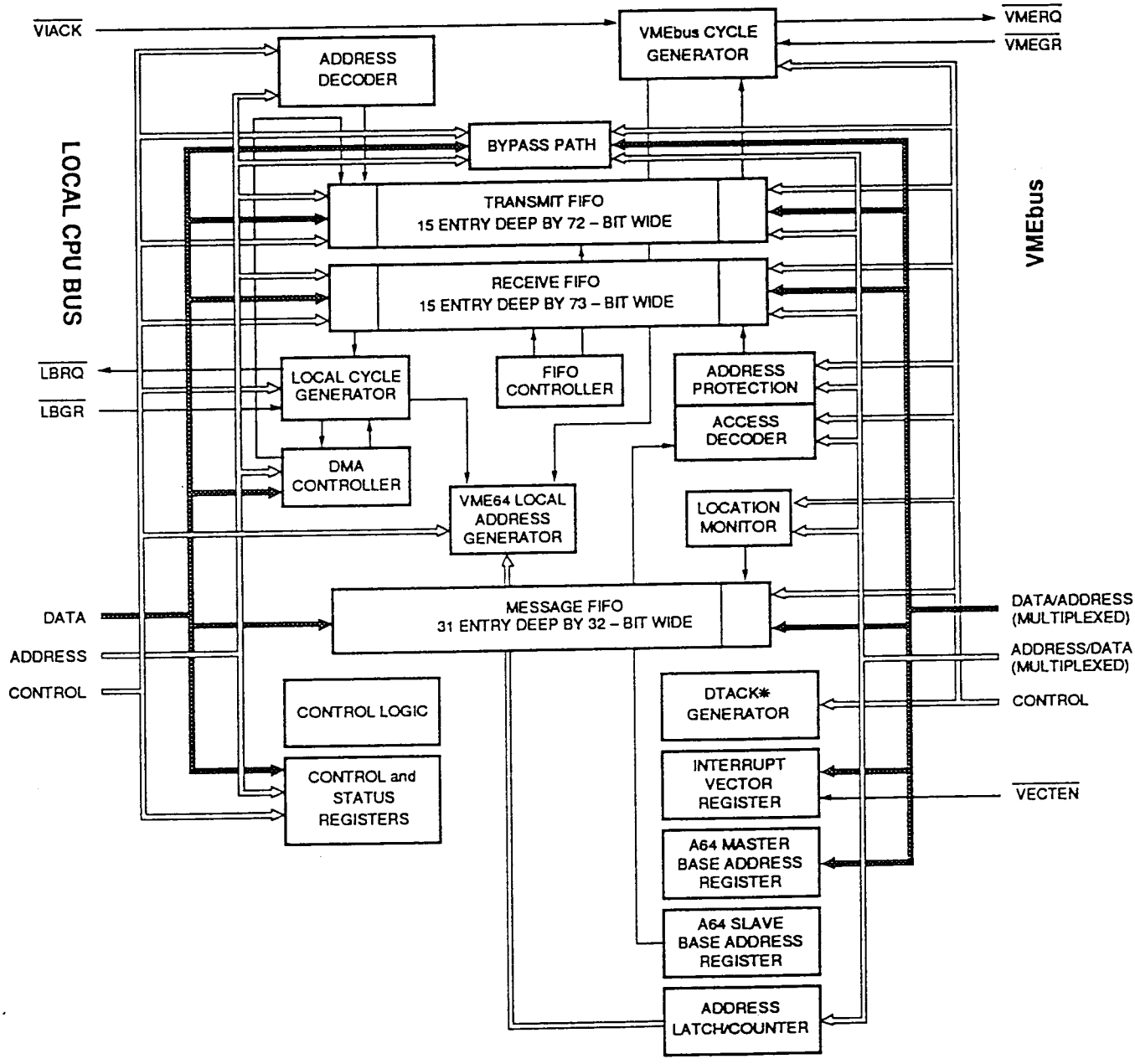



**Figure 1 : CA91C064 DARF64 BLOCK DIAGRAM**

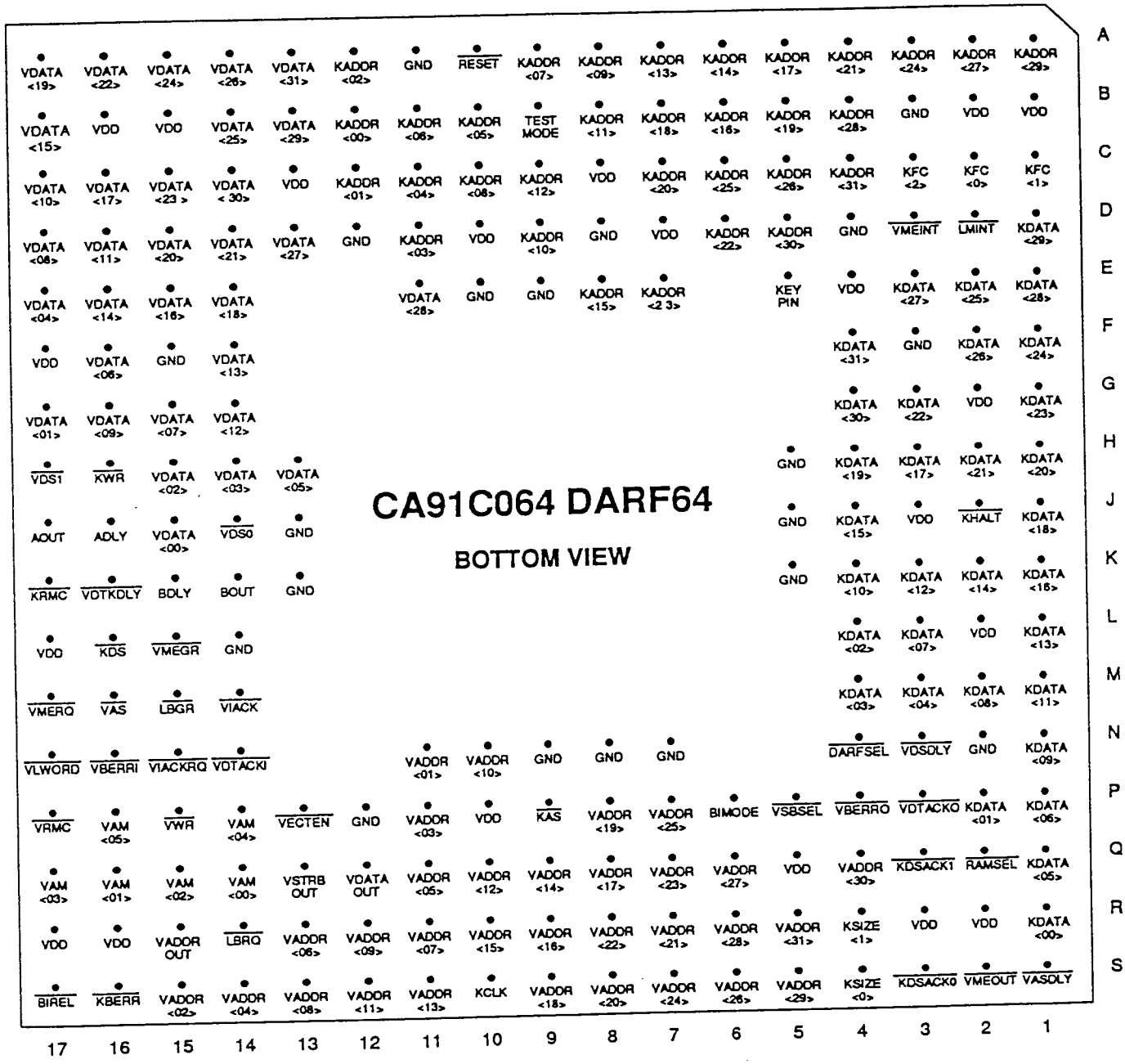



**Figure 2 : PIN CONFIGURATION for 224–PIN PGA PACKAGE**

**Table 1 : DARF64 PGA PINOUT**

| Pin | Signal | Signal Group |
|---|---|---|
| A1 | KADDR 29 | Local Bus |
| A2 | KADDR 27 | Local Bus |
| A3 | KADDR 24 | Local Bus |
| A4 | KADDR 21 | Local Bus |
| A5 | KADDR 17 | Local Bus |
| A6 | KADDR 14 | Local Bus |
| A7 | KADDR 13 | Local Bus |
| A8 | KADDR 09 | Local Bus |
| A9 | KADDR 07 | Local Bus |
| A10 | $\overline{\text{RESET}}$ | Reset, Clock & Mode |
| A11 | $V_{SS}$ | |
| A12 | KADDR 02 | Local Bus |
| A13 | VDATA 31 | VMEbus |
| A14 | VDATA 26 | VMEbus |
| A15 | VDATA 24 | VMEbus |
| A16 | VDATA 22 | VMEbus |
| A17 | VDATA 19 | VMEbus |
| B1 | $V_{DD}$ | |
| B2 | $V_{DD}$ | |
| B3 | $V_{SS}$ | |
| B4 | KADDR 28 | Local Bus |
| B5 | KADDR 19 | Local Bus |
| B6 | KADDR 16 | Local Bus |
| B7 | KADDR 18 | Local Bus |
| B8 | KADDR 11 | Local Bus |
| B9 | TESTMODE | Reset, Clock & Mode |
| B10 | KADDR 05 | Local Bus |
| B11 | KADDR 06 | Local Bus |
| B12 | KADDR 00 | Local Bus |
| B13 | VDATA 29 | VMEbus |
| B14 | VDATA 25 | VMEbus |
| B15 | $V_{DD}$ | |
| B16 | $V_{DD}$ | |
| B17 | VDATA 15 | VMEbus |
| C1 | KFC1 | Local Bus |
| C2 | KFC0 | Local Bus |
| C3 | KFC2 | Local Bus |
| C4 | KADDR 31 | Local Bus |
| C5 | KADDR 26 | Local Bus |
| C6 | KADDR 25 | Local Bus |
| C7 | KADDR 20 | Local Bus |
| C8 | $V_{DD}$ | |
| C9 | KADDR 12 | Local Bus |
| C10 | KADDR 08 | Local Bus |
| C11 | KADDR 04 | Local Bus |
| C12 | KADDR 01 | Local Bus |
| C13 | $V_{DD}$ | |
| C14 | VDATA 30 | VMEbus |
| C15 | VDATA 23 | VMEbus |
| C16 | VDATA 17 | VMEbus |
| C17 | VDATA 10 | VMEbus |
| D1 | KDATA 29 | Local Bus |
| D2 | $\overline{\text{LMINT}}$ | Reset, Clock & Mode |
| D3 | $\overline{\text{VMEINT}}$ | Reset, Clock & Mode |
| D4 | $V_{SS}$ | |
| D5 | KADDR 30 | Local Bus |
| D6 | KADDR 22 | Local Bus |
| D7 | $V_{DD}$ | |
| D8 | $V_{SS}$ | |
| D9 | KADDR 10 | Local Bus |
| D10 | $V_{DD}$ | |
| D11 | KADDR 03 | Local Bus |
| D12 | $V_{SS}$ | |
| D13 | VDATA 27 | VMEbus |
| D14 | VDATA 21 | VMEbus |
| D15 | VDATA 20 | VMEbus |
| D16 | VDATA 11 | VMEbus |
| D17 | VDATA 08 | VMEbus |
| E1 | KDATA 28 | Local Bus |
| E2 | KDATA 25 | Local Bus |
| E3 | KDATA 27 | Local Bus |
| E4 | $V_{DD}$ | |
| E5 | N/C | (Keying Pin) |
| E7 | KADDR 23 | Local Bus |
| E8 | KADDR 15 | Local Bus |
| E9 | $V_{SS}$ | |
| E10 | $V_{SS}$ | |
| E11 | VDATA 28 | VMEbus |
| E14 | VDATA 18 | VMEbus |
| E15 | VDATA 16 | VMEbus |
| E16 | VDATA 14 | VMEbus |
| E17 | VDATA 04 | VMEbus |
| F1 | KDATA 24 | Local Bus |
| F2 | KDATA 26 | Local Bus |
| F3 | $V_{SS}$ | |
| F4 | KDATA 31 | Local Bus |

**Table 1 : DARF64 PGA PINOUT CON'T**

| Pin | Signal | Signal Group |
|---|---|---|
| F14 | VDATA 13 | VMEbus |
| F15 | $V_{SS}$ | |
| F16 | VDATA 06 | VMEbus |
| F17 | $V_{DD}$ | |
| G1 | KDATA 23 | Local Bus |
| G2 | $V_{DD}$ | |
| G3 | KDATA 22 | Local Bus |
| G4 | KDATA 30 | Local Bus |
| G14 | VDATA 12 | VMEbus |
| G15 | VDATA 07 | VMEbus |
| G16 | VDATA 09 | VMEbus |
| G17 | VDATA 01 | VMEbus |
| H1 | KDATA 20 | Local Bus |
| H2 | KDATA 21 | Local Bus |
| H3 | KDATA 17 | Local Bus |
| H4 | KDATA 19 | Local Bus |
| H5 | $V_{SS}$ | |
| H13 | VDATA 05 | VMEbus |
| H14 | VDATA 03 | VMEbus |
| H15 | VDATA 02 | VMEbus |
| H16 | $\overline{KWR}$ | Local Bus |
| H17 | $\overline{VDS1}$ | VMEbus |
| J1 | KDATA 18 | Local Bus |
| J2 | $\overline{KHALT}$ | Local Bus |
| J3 | $V_{DD}$ | |
| J4 | KDATA 15 | Local Bus |
| J5 | $V_{SS}$ | |
| J13 | $V_{SS}$ | |
| J14 | $\overline{VDS0}$ | VMEbus |
| J15 | VDATA 00 | VMEbus |
| J16 | ADLY | Reset, Clock & Mode |
| J17 | AOUT | Reset, Clock & Mode |
| K1 | KDATA 16 | Local Bus |
| K2 | KDATA 14 | Local Bus |
| K3 | KDATA 12 | Local Bus |
| K4 | KDATA 10 | Local Bus |
| K5 | $V_{SS}$ | |
| K13 | $V_{SS}$ | |
| K14 | BOUT | Reset, Clock & Mode |
| K15 | BDLY | Reset, Clock & Mode |
| K16 | $\overline{VDTKDLY}$ | VMEbus |
| K17 | $\overline{KRMC}$ | Local Bus |
| L1 | KDATA 13 | Local Bus |
| L2 | $V_{DD}$ | |
| L3 | KDATA 07 | Local Bus |
| L4 | KDATA 02 | Local Bus |
| L14 | $V_{SS}$ | |
| L15 | $\overline{VMEGR}$ | VMEbus |
| L16 | $\overline{KDS}$ | Local Bus |
| L17 | $V_{DD}$ | |
| M1 | KDATA 11 | Local Bus |
| M2 | KDATA 08 | Local Bus |
| M3 | KDATA 04 | Local Bus |
| M4 | KDATA 03 | Local Bus |
| M14 | $\overline{VIACK}$ | VMEbus |
| M15 | $\overline{LBGR}$ | Local Bus |
| M16 | $\overline{VAS}$ | VMEbus |
| M17 | $\overline{VMERQ}$ | VMEbus |
| N1 | KDATA 09 | Local Bus |
| N2 | $V_{SS}$ | |
| N3 | $\overline{VDSDLY}$ | VMEbus |
| N4 | $\overline{DARFCS}$ | Local Bus |
| N7 | $V_{SS}$ | |
| N8 | $V_{SS}$ | |
| N9 | $V_{SS}$ | |
| N10 | VADDR 10 | VMEbus |
| N11 | VADDR 01 | VMEbus |
| N14 | $\overline{VDTACKI}$ | VMEbus |
| N15 | $\overline{VIACKRQ}$ | VMEbus |
| N16 | $\overline{VBERRI}$ | VMEbus |
| N17 | $\overline{VLWORD}$ | VMEbus |
| P1 | KDATA 06 | Local Bus |
| P2 | KDATA 01 | Local Bus |
| P3 | $\overline{VDTACKO}$ | VMEbus |
| P4 | $\overline{VBERRO}$ | VMEbus |
| P5 | $\overline{VSBSEL}$ | VMEbus |
| P6 | BIMODE | Reset, Clock & Mode |
| P7 | VADDR 25 | VMEbus |
| P8 | VADDR 19 | VMEbus |
| P9 | $\overline{KAS}$ | Local Bus |
| P10 | $V_{DD}$ | |
| P11 | VADDR 03 | VMEbus |
| P12 | $V_{SS}$ | |
| P13 | $\overline{VECTEN}$ | VMEbus |
| P14 | VAM 04 | VMEbus |
| P15 | $\overline{VWR}$ | VMEbus |

**Table 1 : DARF64 PGA PINOUT CON'T**

| Pin | Signal | Signal Group |
|---|---|---|
| P16 | VAM 05 | VMEbus |
| P17 | $\overline{\text{VRMC}}$ | VMEbus |
| Q1 | KDATA 05 | Local Bus |
| Q2 | $\overline{\text{RAMSEL}}$ | Local Bus |
| Q3 | $\overline{\text{KDSACK1}}$ | Local Bus |
| Q4 | VADDR 30 | VMEbus |
| Q5 | $V_{DD}$ | |
| Q6 | VADDR 27 | VMEbus |
| Q7 | VADDR 23 | VMEbus |
| Q8 | VADDR 17 | VMEbus |
| Q9 | VADDR 14 | VMEbus |
| Q10 | VADDR 12 | VMEbus |
| Q11 | VADDR 05 | VMEbus |
| Q12 | VDATAOUT | VMEbus |
| Q13 | VSTRBOUT | VMEbus |
| Q14 | VAM 00 | VMEbus |
| Q15 | VAM 02 | VMEbus |
| Q16 | VAM 01 | VMEbus |
| Q17 | VAM 03 | VMEbus |
| R1 | KDATA 00 | Local Bus |
| R2 | $V_{DD}$ | |
| R3 | $V_{DD}$ | |
| R4 | KSIZE1 | Local Bus |
| R5 | VADDR 31 | VMEbus |
| R6 | VADDR 28 | VMEbus |
| R7 | VADDR 21 | VMEbus |
| R8 | VADDR 22 | VMEbus |
| R9 | VADDR 16 | VMEbus |
| R10 | VADDR 15 | VMEbus |
| R11 | VADDR 07 | VMEbus |
| R12 | VADDR 09 | VMEbus |
| R13 | VADDR 06 | VMEbus |
| R14 | $\overline{\text{LBRQ}}$ | Local Bus |
| R15 | VADDROUT | VMEbus |
| R16 | $V_{DD}$ | |
| R17 | $V_{DD}$ | |
| S1 | $\overline{\text{VASDLY}}$ | VMEbus |
| S2 | $\overline{\text{VMEOUT}}$ | VMEbus |
| S3 | $\overline{\text{KDSACK0}}$ | Local Bus |
| S4 | KSIZE0 | Local Bus |
| S5 | VADDR 29 | VMEbus |
| S6 | VADDR 26 | VMEbus |
| S7 | VADDR 24 | VMEbus |
| S8 | VADDR 20 | VMEbus |
| S9 | VADDR 18 | VMEbus |
| S10 | KCLK | Reset, Clock & Mode |
| S11 | VADDR 13 | VMEbus |
| S12 | VADDR 11 | VMEbus |
| S13 | VADDR 08 | VMEbus |
| S14 | VADDR 04 | VMEbus |
| S15 | VADDR 02 | VMEbus |
| S16 | $\overline{\text{KBERR}}$ | Local Bus |
| S17 | $\overline{\text{BIREL}}$ | Reset, Clock & Mode |

### Pin Definitions

The pins of the CA91C064 are briefly described here, grouped into the general categories of Local VMEbus, and Control and Status signals. All inputs are CMOS with TTL thresholds, while output cell drive strength has been selected according to the load that a card design would place on it. The $\overline{\text{VDTACKI}}$ and $\overline{\text{VBERRI}}$ inputs have hysteresis, allowing then to be connected directly to the VMEbus.

### Table 2a : LOCAL BUS SIGNALS

The local bus signals are those used to gain access to, or perform data transfers on the local CPU bus. The DARF is designed for parallel connection with a 68020 or 68030 CPU.

| Symbol | Pin(s) | Type | Name and Function |
|---|---|---|---|
| $\overline{\text{DARFCS}}$ | N4 | I | DARF internal registers chip select, input |
| KADDR 31 – 00 | C4, D5, A1, B4, A2, C5, C6, A3, E7, D6, A4, C7, B5, B7, A5, B6, E8, A6, A7, C9, B8, D9, A8, C10, A9, B11, B10, C11, D11, A12, C12, B12 | I/O | Address bus bits 31 through 00, input/output |
| $\overline{\text{KAS}}$ | P9 | I/O | Address strobe, input/output |
| $\overline{\text{KBERR}}$ | S16 | I/O | Data transfer failure, input/output |
| KDATA 31 – 00 | F4, G4, D1, E1, E3, F2, E2, F1, G1, G3, H2, H1, H4, J1, H3, K1, J4, K2, L1, K3, M1, K4, N1, M2, L3, P1, Q1, M3, M4, L4, P2, R1 | I/O | Data bus bits 31 through 00, input/output |
| $\overline{\text{KDS}}$ | L16 | I/O | Data strobe, input/output |
| $\overline{\text{KDSACK1}}$ – $\overline{\text{KDSACK0}}$ | Q3, S3 | I/O | Transfer and size acknowledge, input/output |
| KFC2 – KFC0 | C3, C1, C2 | I/O | Function code indicator bits, input/output |
| $\overline{\text{KHALT}}$ | J2 | I/O | CPU halt or retry, input/output |
| $\overline{\text{KRMC}}$ | K17 | I/O | Read-modify-write lock signal, input/output |
| KSIZE1 – KSIZE0 | R4, S4 | I/O | Data transfer size bits, input/output |
| $\overline{\text{KWR}}$ | H16 | I/O | Write signal, input/output |
| $\overline{\text{LBGR}}$ | M15 | I | Local bus grant, input |
| $\overline{\text{LBRQ}}$ | R14 | O | Local bus request, output |
| $\overline{\text{RAMSEL}}$ | Q2 | O | Local memory enable signal, output |

**Table 2b : VMEbus SIGNALS**

The VMEbus signals are those involved in gaining access to and using the VMEbus. The DARF does not connect directly to the VMEbus; rather, external buffers and transceivers are used for VMEbus control signals and addresses.

| Symbol | Pin(s) | Type | Name and Function |
|---|---|---|---|
| VADDR 31 – 01 | R5, Q4, S5, R6, Q6, S6<br>P7, S7, Q7, R8, R7, S8<br>P8, S9, Q8, R9, R10, Q9<br>S11, Q10, S12, N10<br>R12, S13, R11, R13<br>Q11, S14, P11, S15, N11 | I/O | Address bits |
| VADDROUT | R15 | O | Address transceiver direction control |
| VAM 05 – VAM 00 | P16, P14, Q17,<br>Q15, Q16, Q14 | I/O | Address modifier bits |
| $\overline{\text{VAS}}$ | M16 | I/O | Address strobe |
| $\overline{\text{VASDLY}}$ | S1 | I | Delayed address strobe |
| $\overline{\text{VBERRI}}$ | N16 | I | BERR* |
| $\overline{\text{VBERRO}}$ | P4 | O | BERR* |
| VDATA 31 – 00 | A13, C14, B13, E11, D13<br>A14, B14, A15, C15, A16<br>D14, D15, A17, E14, C16<br>E15, B17, E16, F14, G14<br>D16, C17, G16, D17, G15<br>F16, H13, E17, H14, H15<br>G17, J15 | I/O | Data bits |
| VDATAOUT | Q12 | O | Data transceiver direction control |
| $\overline{\text{VDS1}}$ – $\overline{\text{VDS0}}$ | H17, J14 | I/O | Data strobes |
| $\overline{\text{VDSDLY}}$ | N3 | I | Delayed data strobe |
| $\overline{\text{VDTACKI}}$ | N14 | I | DTACK* |
| $\overline{\text{VDTACKO}}$ | P3 | O | DTACK* |
| $\overline{\text{VDTKDLY}}$ | K16 | I | Delayed DTACK* |
| $\overline{\text{VECTEN}}$ | P13 | I | Respond to VMEbus IACK cycle request |
| $\overline{\text{VIACK}}$ | M14 | I/O | IACK* signal |
| $\overline{\text{VIACKRQ}}$ | N15 | I | VMEbus IACK cycle request to DARF |
| $\overline{\text{VLWORD}}$ | N17 | I/O | Long-word signal |
| $\overline{\text{VMEGR}}$ | L15 | I | VMEbus grant input from the ACC |
| $\overline{\text{VMEOUT}}$ | S2 | I | Off-card data transfer bus select |
| $\overline{\text{VMERQ}}$ | M17 | O | VMEbus request output to the ACC |
| $\overline{\text{VRMC}}$ | P17 | I/O | Read-modify-write signal |
| $\overline{\text{VSBSEL}}$ | P5 | O | Auxilliary data transfer bus select |
| VSTRBOUT | Q13 | O | Address and data strobe transceiver direction |
| $\overline{\text{VWR}}$ | P15 | I/O | Write signal |

**Table 2c : RESET, CLOCK and MODE SIGNALS**

| Symbol | Pin(s) | Type | Name and Function |
|---|---|---|---|
| ADLY | J16 | I | Delay circuit A input from delay line |
| AOUT | J17 | O | Delay circuit A output to delay line |
| BDLY | K15 | I | Delay circuit B input from delay line |
| BIMODE | P6 | I | BI-mode™ signal |
| $\overline{\text{BIREL}}$ | S17 | O | BI-mode™ release |
| BOUT | K14 | O | Delay circuit B output to delay line |
| KCLK | S10 | I | Clock input, same as the CPU clock |
| $\overline{\text{LMINT}}$ | D2 | O | Location Monitor FIFO interrupt |
| $\overline{\text{RESET}}$ | A10 | I | Reset input |
| TESTMODE | B9 | I | Chip test mode input; for chip fabrication only |
| $\overline{\text{VMEINT}}$ | D3 | O | VMEbus related events interrupt |



## TERMINOLOGY

Signals on the VMEbus and those within the circuit card may be active high or active low. Active low signals are defined as being true or asserted when they are at a low voltage, and conversely for active high signals. VMEbus active low signals are indicated by the * suffix, while on-card active low signals that do not connect directly to the VMEbus are indicated with $\overline{\text{OVERBARS}}$.

Where there is a need to clarify whether a signal is a VMEbus or local signal, a V may be prefixed for VMEbus signals, an L for general local signals, or a K for signals only connecting to the local CPU.

The output type abbreviations used in Tables 3 and 9 are defined in this section. They have both a letter code and a number suffix which indicates their current rating.

For example, the VDATA 31-00 signals are shown as input type CTTL, which are CMOS inputs with normal TTL voltage thresholds, and output type TS4 SR, which are tri-stateable 4 mA sink and source current outputs with slew rate limiting.

| | |
|---|---|
| TP | Totem pole output |
| TS | Tri-state totem pole output |
| OD | Open drain output |
| SR | Slew rate limited output |
| CTTL | CMOS input with TTL thresholds |
| CTTL PD | CMOS input, TTL thresholds, integral pull down |
| CTTL PU | CMOS input, TTL thresholds, integral pull up |
| CMOS | CMOS input with CMOS thresholds |

**Table 3 : INPUT AND OUTPUT TYPE GENERAL CLASSIFICATION**

| Signal | Input | Output |
|---|---|---|
| ADLY | CTTL | |
| AOUT | | TP4 |
| BDLY | CTTL | |
| BIMODE | CTTL | |
| $\overline{\text{BIREL}}$ | | TP2 |
| BOUT | | TP4 |
| $\overline{\text{DARFCS}}$ | CTTL | |
| $\overline{\text{DTACKDLY}}$ | CTTL | |
| KADDR 31 – 00 | CTTL | TS6 |
| $\overline{\text{KAS}}$ | CTTL | TS8 |
| $\overline{\text{KBERR}}$ | CTTL | OD8 |
| KCLK | CMOS | |
| KDATA 31 – 00 | CTTL PU | TS6 |
| $\overline{\text{KDS}}$ | | TS8 |
| $\overline{\text{KDSACK1}}$ – $\overline{\text{KDSACK0}}$ | CTTL | TS8 |
| $\overline{\text{KFC 1}}$ | | TS6 |
| $\overline{\text{KFC 2,0}}$ | CTTL | TS6 |
| $\overline{\text{KHALT}}$ | | OD12 |
| $\overline{\text{KRMC}}$ | CTTL | TS8 |
| KSIZE1 – KSIZE0 | CTTL | TS8 |
| $\overline{\text{KWR}}$ | CTTL | TS8 |
| $\overline{\text{LBGR}}$ | CTTL | |
| $\overline{\text{LBRQ}}$ | | TP2 |
| $\overline{\text{LMINT}}$ | | TP2 |
| $\overline{\text{RAMSEL}}$ | | TP4 |
| $\overline{\text{RESET}}$ | CTTL | |

| Signal | Input | Output |
|---|---|---|
| TESTMODE | CTTLz | |
| VADDR 31-01 | CTTL | TS2 |
| VADDROUT | CTTL | TS4 |
| VAM 05 – VAM 00 | CTTL | TS4 |
| $\overline{\text{VAS}}$ | CTTL | TS4 |
| $\overline{\text{VASDLY}}$ | CTTL | |
| $\overline{\text{VBERRI}}$ | CTTL | |
| $\overline{\text{VBERRO}}$ | | TP4 |
| VDATA 31 – 00 | CTTL | TS4 SR |
| VDATAOUT | | TP4 |
| $\overline{\text{VDS1}}$ – $\overline{\text{VDS0}}$ | CTTL | TS4 |
| $\overline{\text{VDSDLY}}$ | CTTL | |
| $\overline{\text{VDTACKI}}$ | CTTL | |
| $\overline{\text{VDTACKO}}$ | | TP4 |
| $\overline{\text{VECTEN}}$ | CTTL | |
| $\overline{\text{VIACK}}$ | CTTL | TS4 |
| $\overline{\text{VIACKRQ}}$ | CTTL | |
| $\overline{\text{VLWORD}}$ | CTTL | TS4 |
| $\overline{\text{VMEGR}}$ | CTTL | |
| $\overline{\text{VMEINT}}$ | | TP2 |
| $\overline{\text{VMEOUT}}$ | CTTL | |
| $\overline{\text{VMERQ}}$ | | TP2 |
| $\overline{\text{VRMC}}$ | CTTL | TS4 |
| $\overline{\text{VSBSEL}}$ | | TP4 |
| VSTRBOUT | | TP4 |
| $\overline{\text{VWR}}$ | CTTL | TS4 |

**Table 4 : AC CHARACTERISTICS (DARF LOCAL BUS MASTERSHIP)**
**(Commercial $T_A$ = 0° to +70°C, $V_{DD}$ = 5V ± 5%, Military $T_A$ = –55° to +125°C, $V_{DD}$ = 5V ± 10%)**

| Symbol | Description | Clk Count | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| | | | | Com | Mil | |
| | Clock frequency | | - | 25 | 20 | MHz |
| $t_1$ | KCLK cycle time | - | 40/50 | | | ns |
| $t_2$ | KCLK pulse width low | - | 17/22 | - | - | ns |
| $t_3$ | KCLK pulse width high | - | 17/22 | - | - | ns |
| $t_{4,5}$ | KCLK rise and fall times | - | | 5 | 5 | ns |
| $t_6$ | KCLK high to address valid | - | 5 | 34 | 40 | ns |
| $t_7$ | KCLK high to address tri-state | - | 5 | 30 | 35 | ns |
| $t_8$ | KCLK high to address invalid | - | 5 | - | - | ns |
| $t_9$ | KCLK low to $\overline{KAS}$, $\overline{KDS}$ asserted | - | 3 | 21 | 23 | ns |
| $t_{9A}$ | $\overline{KAS}$ to $\overline{KDS}$ skew (read) (Note 1) | - | –15 | 10 | 15 | ns |
| $t_{9B}$ | $\overline{KAS}$ asserted to $\overline{KDS}$ (write) | 1.0 | –5 | - | - | ns |
| $t_{11}$ | Address valid to $\overline{KAS}$ asserted | - | 5 | - | - | ns |
| $t_{12}$ | $\overline{KCLK}$ low to $\overline{KAS}$, $\overline{KDS}$ negated | - | 3 | 18 | 23 | ns |
| $t_{13}$ | $\overline{KAS}$ negated to address invalid (Note 3) | 0.5 | –2 | - | - | ns |
| $t_{14}$ | $\overline{KAS}$ width asserted (Note 3) | 2.0 | –5 | - | - | ns |
| $t_{14A}$ | $\overline{KDS}$ width asserted (write) (Note 3) | 1.0 | –5 | - | - | ns |
| $t_{14B}$ | $\overline{KAS}$ width asserted | 2.0 | –5 | - | - | ns |
| $t_{15}$ | $\overline{KAS}$ & $\overline{KDS}$ width negated (Note 3) | 1.0 | –5 | - | - | ns |
| $t_{16}$ | KCLK high to $\overline{KAS}$ tri-state | - | 4 | 25 | 30 | ns |
| $t_{17}$ | $\overline{KAS}$, $\overline{KDS}$ high to $\overline{KWR}$ invalid (Note 3) | 0.5 | –2 | - | - | ns |
| $t_{18}$ | KCLK high to $\overline{KWR}$ high | - | 4 | 22 | 28 | ns |
| $t_{20}$ | KCLK high to $\overline{KWR}$ low | - | 4 | 26 | 32 | ns |
| $t_{21}$ | $\overline{KWR}$ high to $\overline{KAS}$ asserted (Note 3) | 0.5 | –5 | - | - | ns |
| $t_{22}$ | $\overline{KWR}$ low to $\overline{KDS}$ asserted (Notes 3 & 6) | 1.5 | 0 | - | - | ns |
| $t_{23}$ | KCLK high to data out valid | - | 5 | 26 | 30 | ns |
| $t_{24}$ | Data out valid to $\overline{KAS}$ negated | 2.5 | T62 | - | - | ns |
| $t_{25}$ | $\overline{KDS}$ high to data out invalid (Notes 3 & 6) | 0.5 | 0 | - | - | ns |
| $t_{26}$ | Data out valid to $\overline{KDS}$ low (Notes 3 & 6) | 0.5 | –7 | - | - | ns |
| $t_{27}$ | Data in valid to KCLK low | - | 5 | - | - | ns |
| $t_{28}$ | $\overline{KDSACK}$ high to next KCLK low | - | 5 | - | - | ns |
| $t_{29}$ | $\overline{KDS}$ high to data hold time | - | 0 | - | - | ns |
| $t_{31}$ | $\overline{KDSACK}$ low to data in valid (Notes 2 & 3) | 1.0 | - | 2 | 5 | ns |

*Notes : See next page*

**Table 4 : AC CHARACTERISTICS (DARF LOCAL BUS MASTERSHIP) CON'T**
**(Commercial $T_A$ = 0° to +70°C, $V_{DD}$ = 5V ± 5%, Military $T_A$ = –55° to +125°C, $V_{DD}$ = 5V ± 10%)**

| Symbol | Description | Clk Count | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| | | | | Com | Mil | |
| $t_{46}$ | $\overline{KWR}$ width low (Note 3) | 4.0 | –5 | - | - | ns |
| $t_{46A}$ | Read/write width law (Synchronous) | 4.0 | –5 | - | - | ns |
| $t_{47A}$ | Asynchronous input setup time (Note 5) | - | 2 | - | - | ns |
| $t_{47B}$ | Asynchronous input hold time (Note 5) | - | 5 | - | - | ns |
| $t_{53}$ | Data out hold from KCLK high | - | 3 | - | - | ns |
| $t_{60}$ | KDSACK1 setup to KCLK rising (Synchronous) | - | 8 | - | - | ns |
| $t_{61}$ | KDSACK1 hold from KCLK rising (Synchronous) | - | 8 | - | - | ns |
| $t_{62}$ | Data hold from KCLK rising (Synchronous write) | - | - | 45 | 55 | ns |
| $t_{77}$ | KCLK high to RAMSEL low, VMEin | | 4 | 21 | 26 | ns |
| $t_{78}$ | KCLK high to RAMSEL high, VMEin | | 3 | 20 | 24 | ns |

Notes:

1. This number can be reduced to 2 ns if strobes have equal loads.
2. If the asynchronous setup time ($t_{47}$) requirements are met, the $\overline{KDSACKn}$ low to data setup time ($t_{31}$) can be ignored. The data must only satisfy the data-in to clock low setup time ($t_{27}$) for the following clock cycle, $\overline{KBERR}$ must only satisfy the later KBERR/ low to clock high setup time ($t_{27A}$) for the following clock cycle.
3. This timing parameter is the sum of the number listed and the product of the CLK COUNT times the period of the CPU clock.
   eg: $t_{21} = -5 + (0.5 \times t_{KCLK})$ ns
4. This specification applies to the first $\overline{KDSACKn}$ signal asserted. In the absence of $\overline{KDSACKn}$, $\overline{KBERR}$ is an asynchronous input using the asynchronous input setup time ($t_{47A}$). Timing paramter $t_{27A}$ must also be met for a late $\overline{KBERR}$.
5. This timing parameter applies for all asynchronous inputs: $\overline{KDSACK0}$, $\overline{KDSACK1}$, $\overline{KBERR}$, $\overline{LBGR}$ and $\overline{VMEGR}$.
6. Actual value depends on the clock input waveform.

**Table 5 : AC CHARACTERISTICS (DARF BUS ARBITRATION)**
**(Commercial $T_A$ = 0° to +70°C, $V_{DD}$ = 5V ± 5%, Military $T_A$ = –55° to +125°C, $V_{DD}$ = 5V ± 10%)**

| Symbol | Description | Clk Count | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| | | | | Com | Mil | |
| $t_{90}$ | KCLK low to $\overline{LBRQ}$ asserted | - | 3 | 20 | 25 | ns |
| $t_{91}$ | KCLK low to $\overline{LBRQ}$ negated | - | 3 | 20 | 25 | ns |
| $t_{92}$ | KCLK low to $\overline{VMERQ}$ asserted | - | 3 | 20 | 25 | ns |
| $t_{93}$ | KCLK low to $\overline{VMERQ}$ negated | - | 3 | 20 | 25 | ns |
| $t_{94}$ | KCLK high to KADDR, $\overline{KFC}$, $\overline{KSIZE}$ buses driven | - | 5 | - | - | ns |
| $t_{95}$ | $\overline{LBGR}$ low to DARF KCLK (Note 1) | 3.5/4.5 | - | - | - | $t_{KCLK}$ |

Notes:

1. This timing parameter is the sum of the number listed and product of the CLK COUNT times the period of the CPU clock.
   eg: $t_{21} = -5 + (0.5 \times t_{KCLK})$ ns

**Figure 3 : INPUT CLOCK WAVEFORM TIMING**

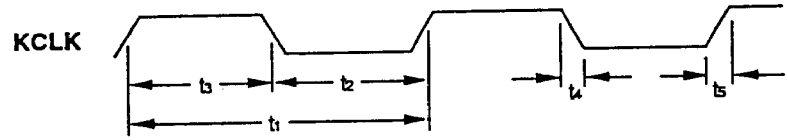



**Figure 4a : DARF 64 LOCAL MASTER INTERFACE, (READ)**

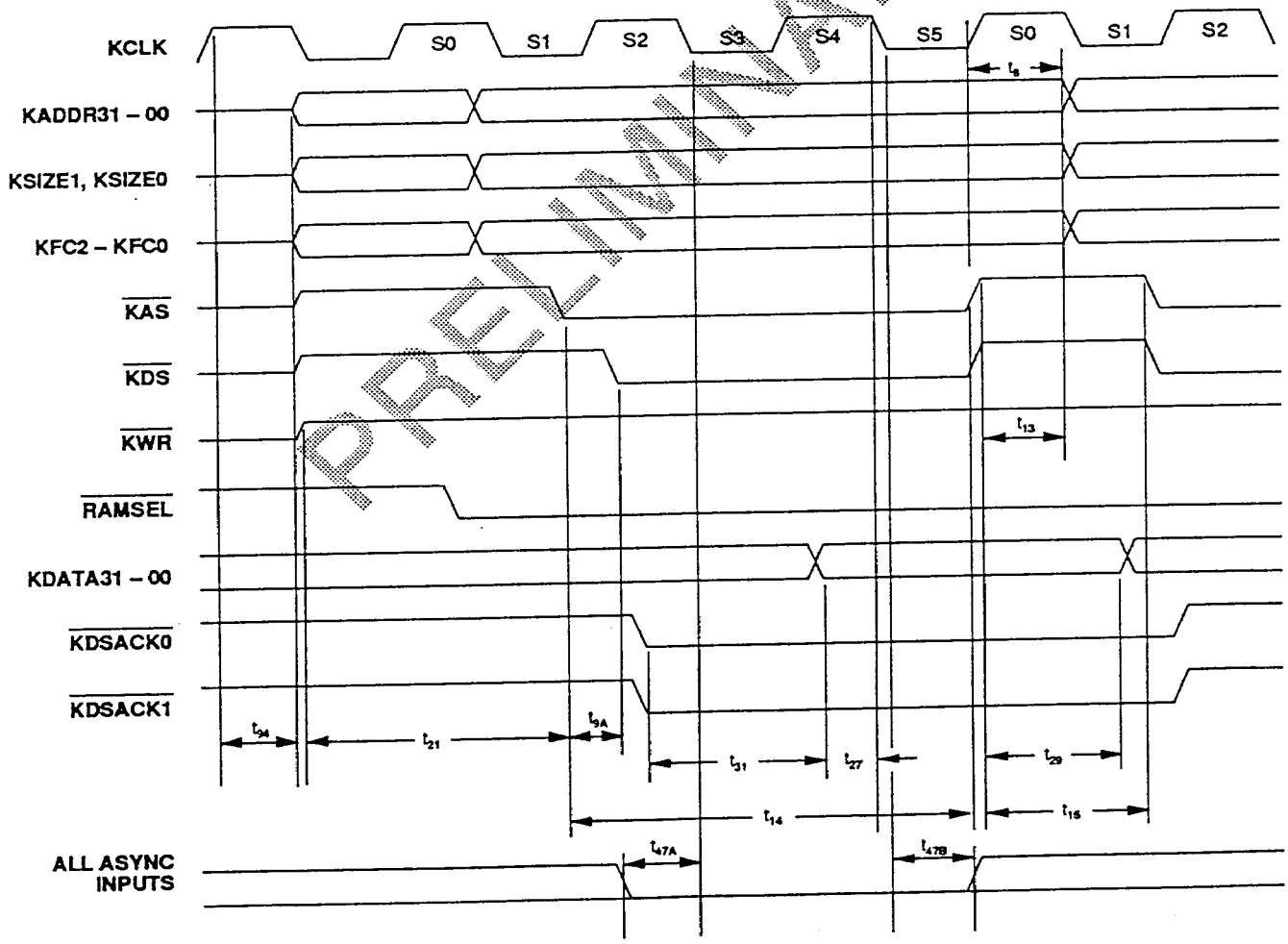


**Figure 4b : DARF 64 LOCAL MASTER INTERFACE, (WRITE)**

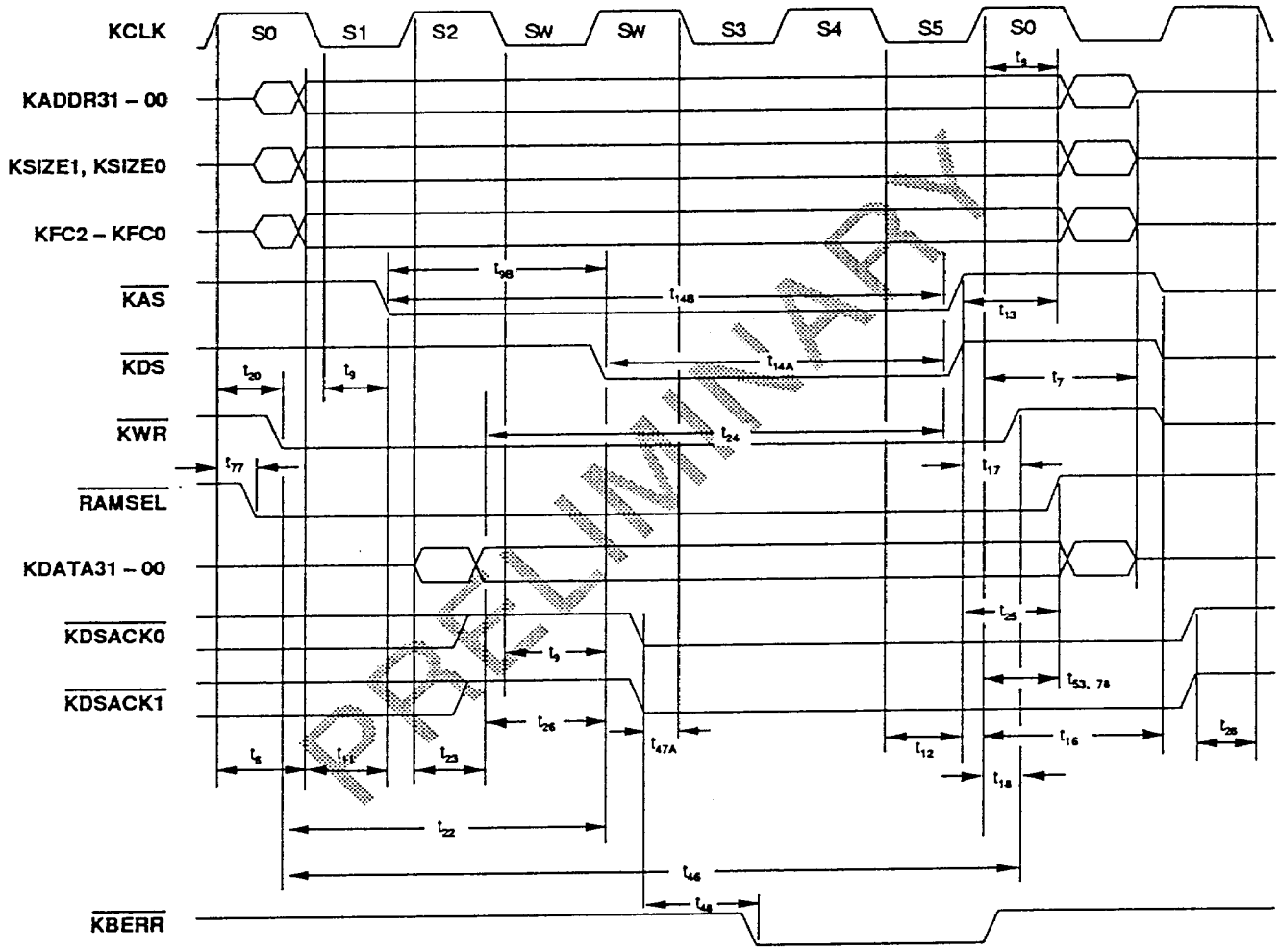
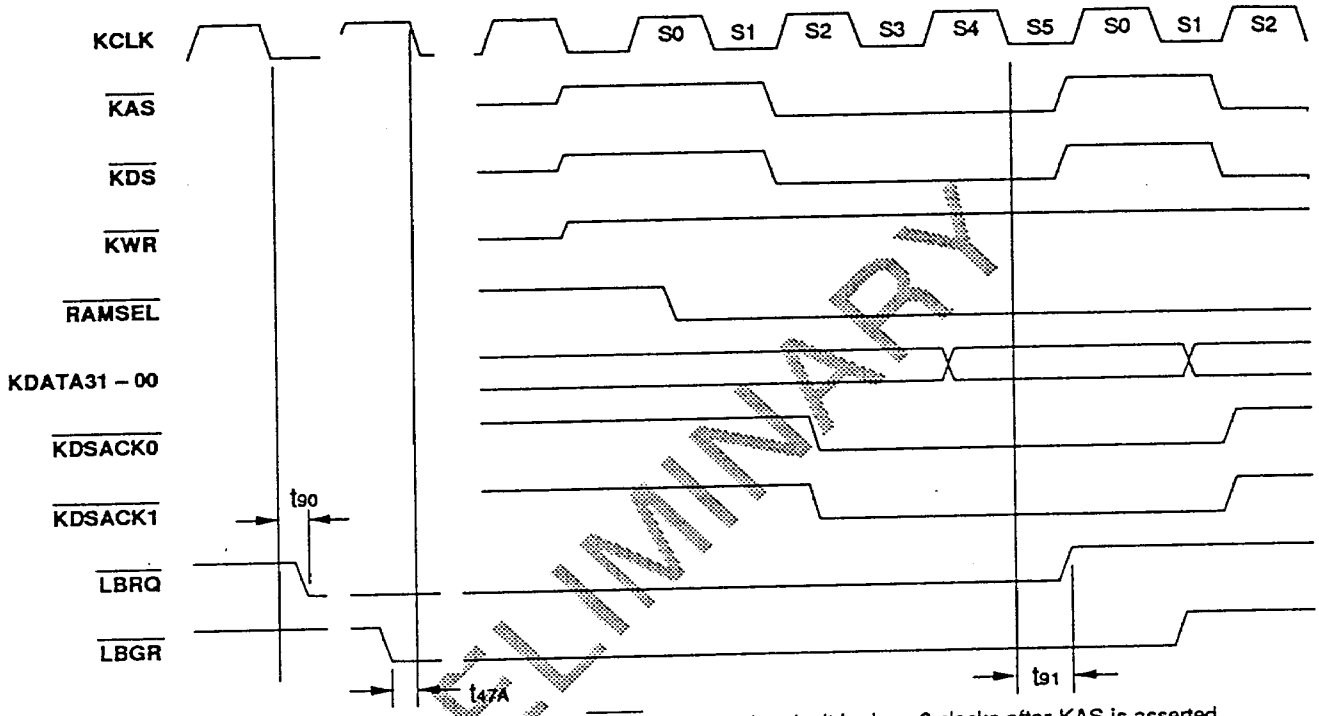


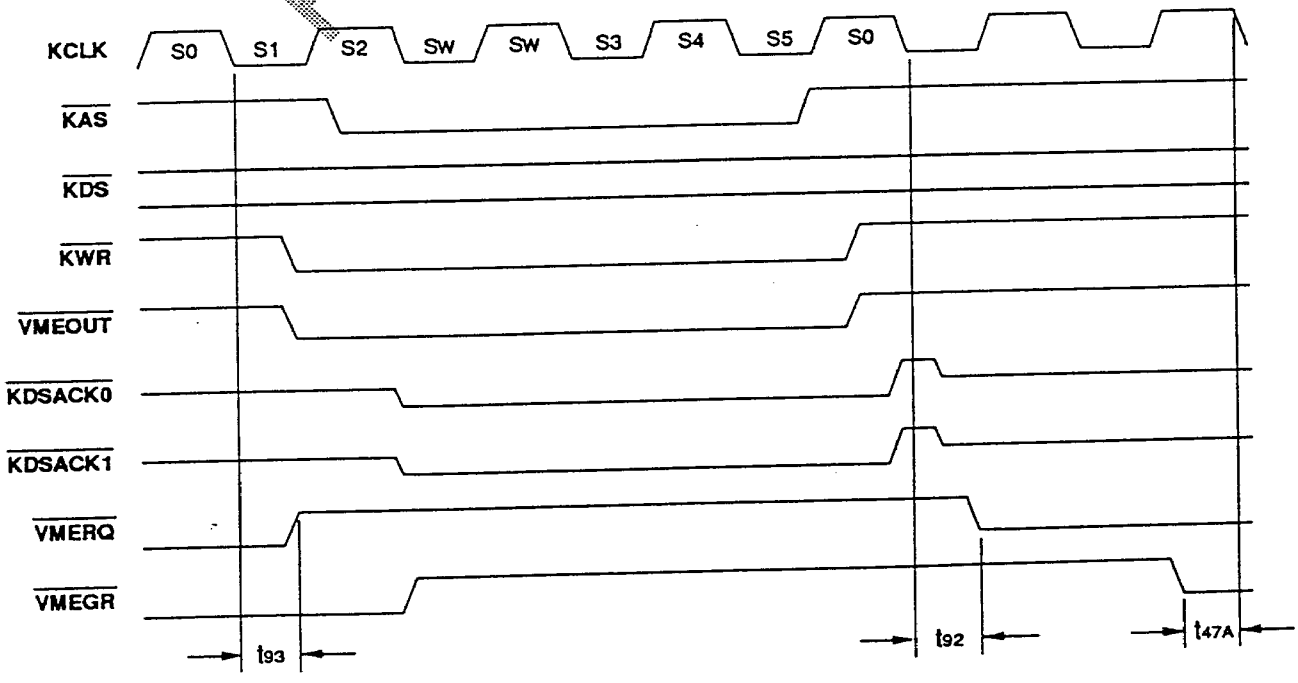
**Figure 5 : DARF BUS ARBITRATION, CPU BUS REQUEST**




Note: LBRQ is only released if another cycle is not pending. If LBRQ is released early, it is done 2 clocks after KAS is asserted.



**Figure 6 : DARF BUS ARBITRATION, CPU BUS REQUEST**




Note: VMEREQ is shown negated here for timing purposes only.

**Table 6 : AC CHARACTERISTICS (DARF LOCAL BUS SLAVE INTERFACE)**
**(Commercial $T_A$ = 0° to +70°C, $V_{DD}$ = 5V ± 5%, Military $T_A$ = –55° to +125°C, $V_{DD}$ = 5V ± 10%)**

| Symbol | Description | Clk Count | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| | | | | Com | Mil | |
| $t_{160}$ | $\overline{KWR}$, KFCn, KSIZEn and KADDRn valid to KCLK low (Note 1) | - | - | 20 | 35 | ns |
| $t_{161}$ | $\overline{KAS}$ setup to KCLK low | - | 5 | - | - | ns |
| $t_{161A}$ | $\overline{KAS}$ delay from KCLK low | - | 3 | - | - | ns |
| $t_{162}$ | KCLK low to data valid (read) | - | 5 | 31 | 37 | ns |
| $t_{163}$ | KCLK low to $\overline{KDSACKn}$ asserted | - | 5 | 29 | 35 | ns |
| $t_{164}$ | KCLK high to address invalid | - | 0 | - | - | ns |
| $t_{165}$ | $\overline{KWR}$, KFCn, KSIZEn and KADDRn valid to KCLK low (Note 1) | - | - | 20 | 35 | ns |
| $t_{166}$ | KCLK low to $\overline{KAS}$ high | - | 0 | - | - | ns |
| $t_{167}$ | $\overline{KAS}$ high to $\overline{KDSACKn}$ high | - | 3 | 20 | 25 | ns |
| $t_{168}$ | KCLK low to $\overline{KDSACKn}$ tri-state | - | 4 | 23 | 28 | ns |
| $t_{169}$ | $\overline{KAS}$ high to data tri-state (read) | - | 5 | 33 | 38 | ns |
| $t_{170}$ | $\overline{KAS}$ high to $\overline{KWR}$ invalid (Note 1) | - | - | 6 | 7 | ns |
| $t_{171}$ | Data setup time to KCLK low | - | 0 | - | - | ns |
| $t_{172}$ | $\overline{KAS}$ high to KFC[2–0] invalid | - | 0 | - | - | ns |
| $t_{173}$ | $\overline{KAS}$ high to $\overline{KSIZE[1–0]}$ invalid (Note 1) | - | - | 6 | 7 | ns |
| $t_{174}$ | KAS high to data invalid (read) | - | 4 | 20 | 24 | ns |



Note:
1. This timing parameter is actually a *minimum* time which must be provided for the given operation condition.

**Figure 7a : DARF SLAVE INTERFACE, CPU REGISTER READ**

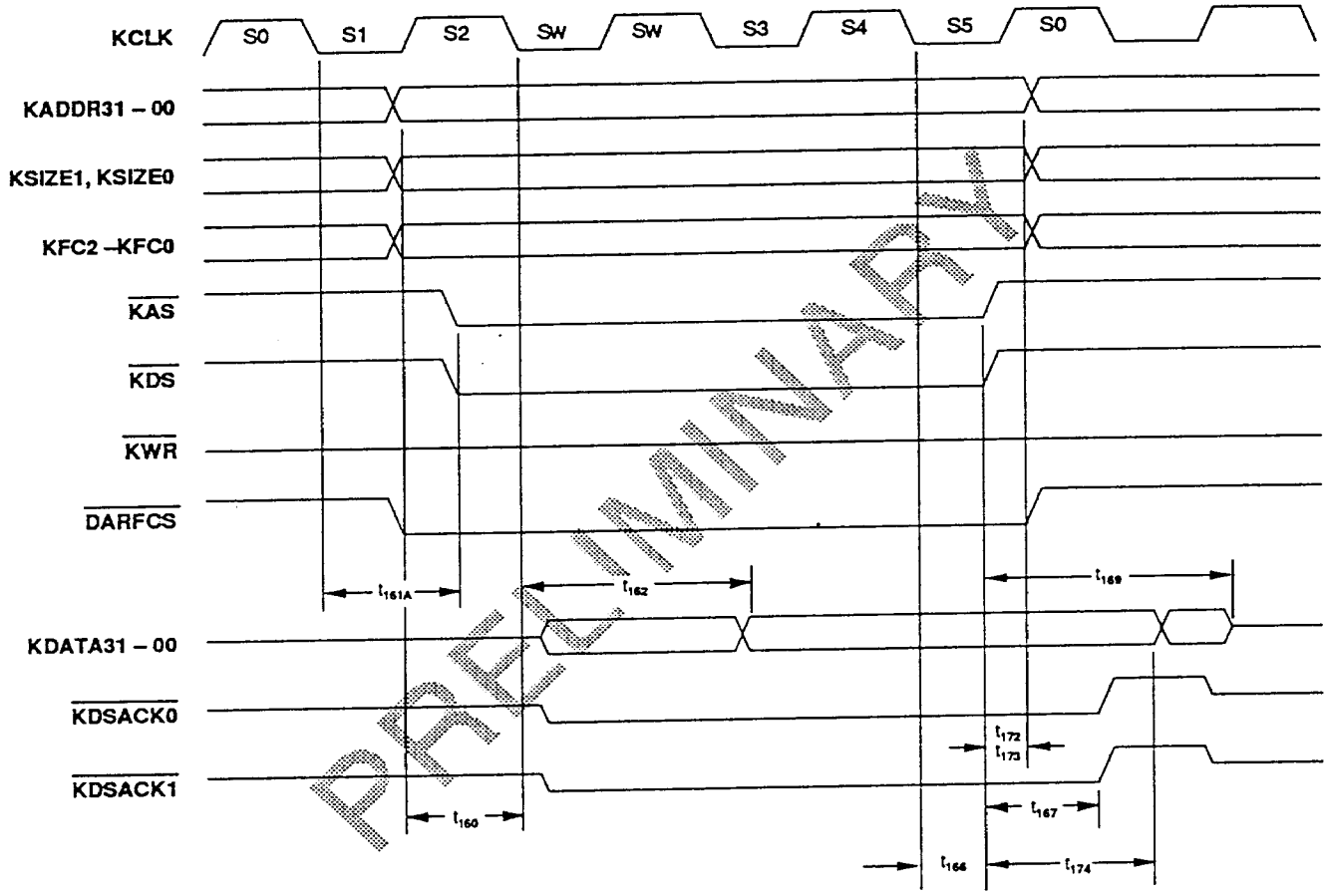


**Figure 7B : DARF SLAVE INTERFACE, CPU REGISTER WRITE**

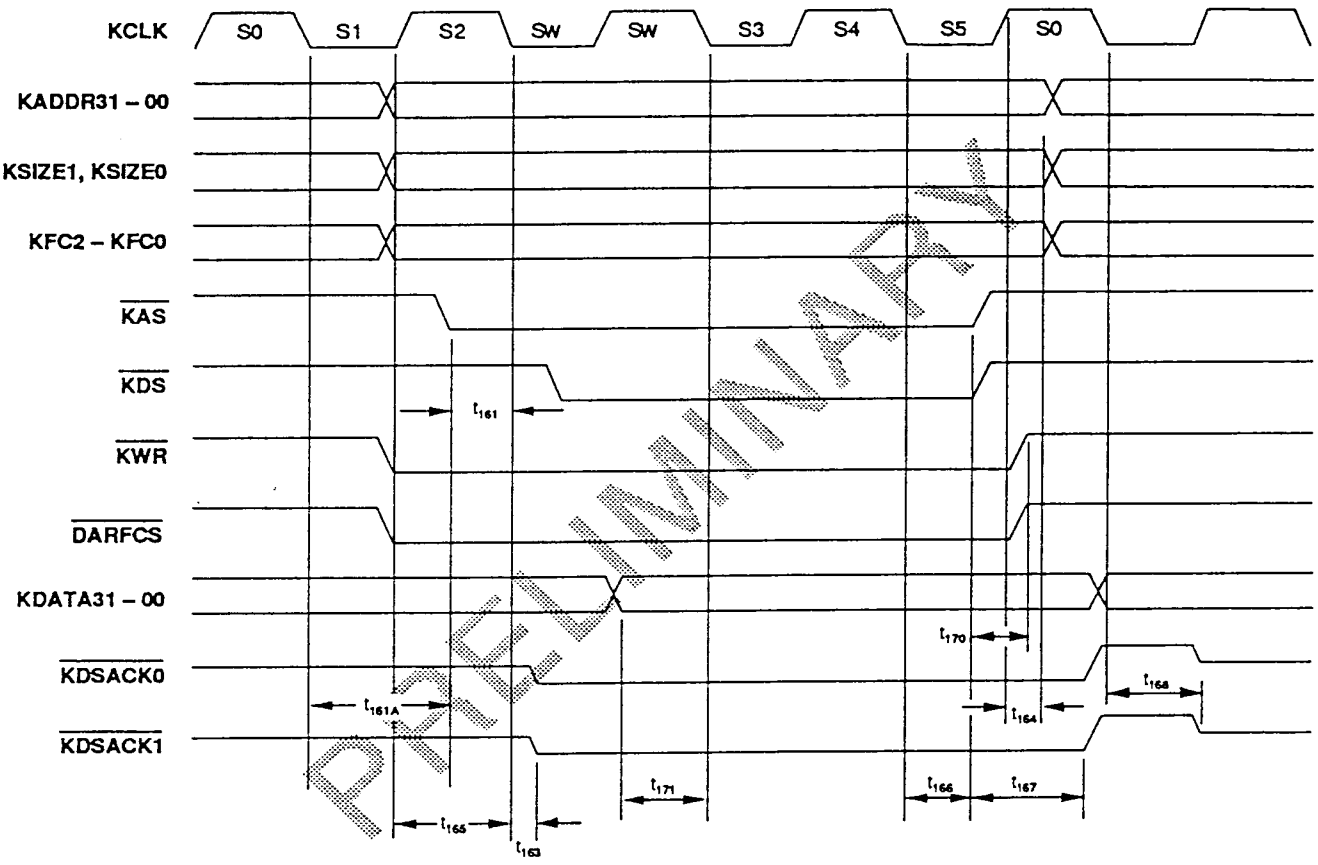
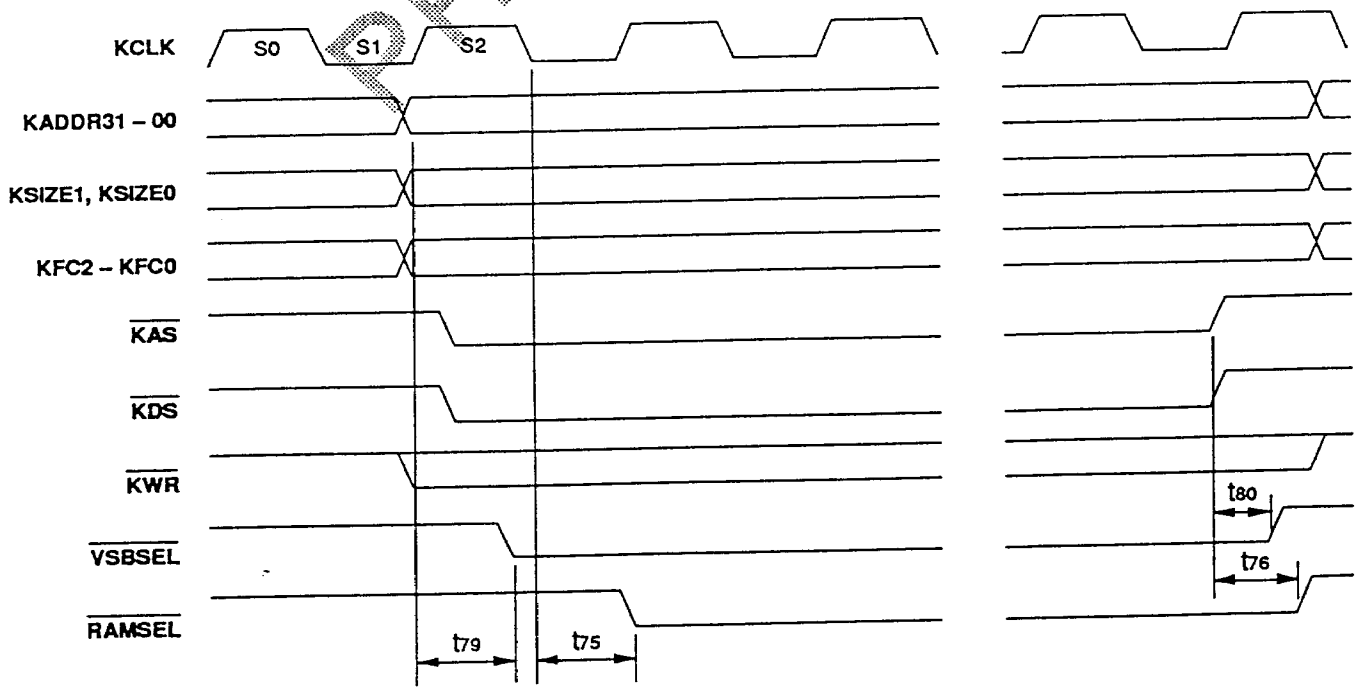


**Table 6A : AC CHARACTERISTICS (DARF LOCAL BUS SLAVE INTERFACE)**
**(Commercial $T_A$ = 0° to +70°C, $V_{DD}$ = 5V ± 5%, Military $T_A$ = –55° to +125°C, $V_{DD}$ = 5V ± 10%)**

| Symbol | Description | Clk Count | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| | | | | Com | Mil | |
| $t_{75}$ | KCLK low to $\overline{\text{RAMSEL}}$ low, VMEout | - | 4 | 24 | 29 | ns |
| $t_{76}$ | $\overline{\text{KAS}}$ high to $\overline{\text{RAMSEL}}$ high, VMEout | - | 3 | 19 | 23 | ns |
| $t_{79}$ | Address valid to VSBSEL low | - | 4 | 18 | 22 | ns |
| $t_{80}$ | $\overline{\text{KAS}}$ high to $\overline{\text{VSBSEL}}$ high | - | 2 | 14 | 17 | ns |
| $t_{81}$ | KCLK low to $\overline{\text{LMINT}}$ low | - | 6 | 30 | 40 | ns |
| $t_{82}$ | KCLK low to $\overline{\text{BIREL}}$ low | - | 3 | 20 | 25 | ns |
| $t_{83}$ | KCLK low to $\overline{\text{BIREL}}$ high | - | 3 | 20 | 25 | ns |

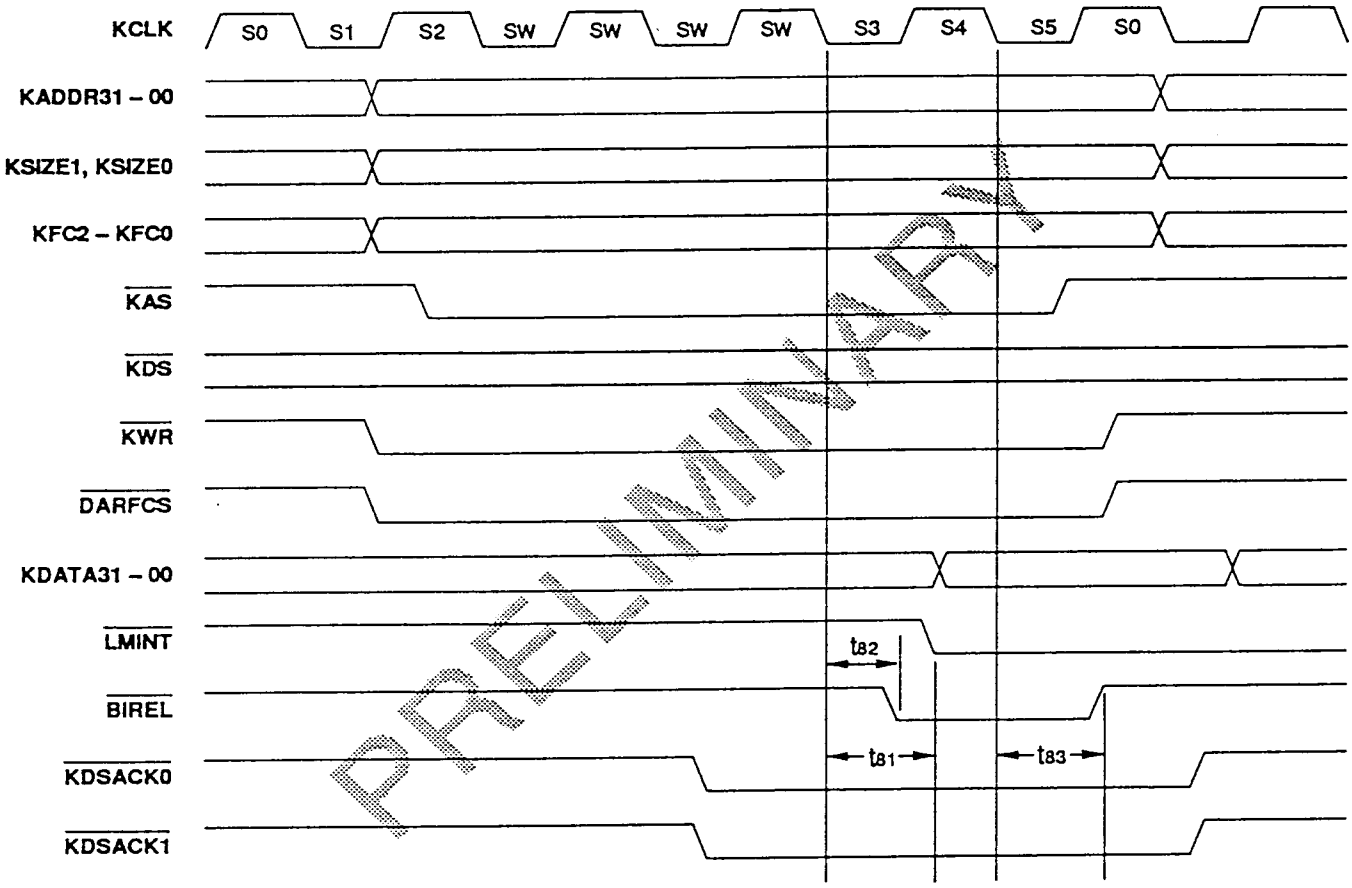


**Figure 8 : DARF SLAVE INTERFACE, VSB and $\overline{\text{RAMSEL}}$ DECODING**




Note: $\overline{\text{RAMSEL}}$ and $\overline{\text{VSBSEL}}$ will not be asserted on the same cycle. Both are shown here for illustration only.

**Figure 9 : DARF SLAVE INTERFACE, CPU LOCATION MONITOR WRITE**






Note:

This diagram assumes that the CPU is allowed access to the Location Monitor without waiting for the VMEbus to finish a write cycle.

If the VMEbus is writing to the FIFO, a minimum of two wait states are added, depending on the DSB* release time of the VME master.

If the LM FIFO is full, wait states are added indefinitely.

**Table 7 : AC CHARACTERISTICS (DARF VMEbus MASTERSHIP)**
**(Commercial $T_A$ = 0° to +70°C, $V_{DD}$ = 5V ± 5%, Military $T_A$ = –55° to +125°C, $V_{DD}$ = 5V ± 10%)**

| Symbol | Description | Clk Count | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| | | | | Com | Mil | |
| $t_{100}$ | KCLK clock low to $\overline{VMERQ}$ asserted (Note 3) | 4 | 3 | 20 | 25 | ns |
| $t_{101}$ | VADDR, VAM valid to $\overline{VAS}$ asserted | - | 35 | - | - | ns |
| $t_{102}$ | $\overline{VWR}$ valid to $\overline{VDSa}$ asserted (Note 3) | 1 | 30 | - | - | ns |
| $t_{103}$ | VDATA valid to $\overline{VDSa}$ asserted | - | 43 | - | - | ns |
| $t_{104}$ | $\overline{VAS}$ asserted to $\overline{VDSa}$ asserted | - | 2 | - | - | ns |
| $t_{105}$ | $\overline{VDTACKI}$ low to VDSb negated, Decoupled VME access | - | 13 | 27 | 31 | ns |
| $t_{105A}$ | $\overline{VDTACKI}$ low to $\overline{VDSb}$ negated, Atomic VME access (Note 4) | - | 45 | 64 | 69 | ns |
| $t_{106}$ | $\overline{VDTACKI}$ low to $\overline{VAS}$ negated, Decoupled VME access with cycle pending | - | 15 | 33 | 38 | ns |
| $t_{107}$ | $\overline{VDTACKI}$ low to VAS negated, Decoupled VME access without cycle pending | - | 15 | 110 | 156 | ns |
| $t_{107A}$ | $\overline{VDTACKI}$ low to $\overline{VAS}$ negated, Atomic VME access (Note 4, 5 & 6) | - | 88 | 99 | 120 | ns |
| $t_{108}$ | VME buffers tri-state to $\overline{VAS}$ negated | - | 3 | 15 | 19 | ns |
| $t_{109}$ | VADDROUT low to VADDR and VAM tri-state | - | 0 | 2 | 2 | ns |
| $t_{110}$ | VDATAOUT low to VDATA tri-state | - | 0 | 0 | 2 | ns |
| $t_{111}$ | $\overline{VMEGR}$ low to VADDROUT, VDATAOUT asserted (Note 3) | 2/3 | 4 | 20 | 30 | ns |
| $t_{112}$ | VADDROUT asserted to $\overline{VAS}$ low (Note 3) | 1 | 44 | 65 | 77 | ns |
| $t_{113}$ | $\overline{VAS}$, $\overline{VDSn}$ minimum high time (Note 4) | - | 45 | - | - | ns |
| $t_{114}$ | VME cycle time, $\overline{VDSn}$ to $\overline{VDSn}$ (Note 1) | - | 90 | 130 | 135 | ns |
| $t_{114A}$ | VME cycle time, $\overline{VDSa}$ to $\overline{VDSn}$ (Block transfers) | - | 90 | 130 | 135 | ns |
| $t_{115}$ | $\overline{VDTACKI}$ high to $\overline{VDSa}$ asserted | - | 5 | - | - | ns |
| $t_{116}$ | $\overline{VDSa}$ low to $\overline{VDTACKI}$ asserted | - | 20 | - | - | ns |
| $t_{117}$ | $\overline{VDSa}$ low to $\overline{VDSb}$ low (Note 7) | - | 0 | 5 | 7 | ns |
| $t_{118}$ | $\overline{VDTACKI}$ low to $\overline{KDSACKn}$ asserted (Note 2, 4) | - | 46 | 69 | 75 | ns |
| $t_{119}$ | $\overline{VMEGR}$ low to $\overline{VAS}$ asserted (Note 3, 4 & 8) | 3/4 | 50 | 85 | 96 | ns |
| $t_{120}$ | AOUT edge to ADLY edge | - | 37 | 43 | 43 | ns |
| $t_{121}$ | BOUT high to BDLY high | - | 37 | 43 | 43 | ns |
| $t_{122}$ | $\overline{VDTACKI}$ low to $\overline{VDTKDLY}$ low | - | 35 | 45 | 45 | ns |

*Notes: see next page*

Notes:

1. This cycle time applies only to the DARF operating in loopback mode. This time represents the maximum obtainable transfer rate under *ideal* conditions.
2. This parameter applies to Atomic VME accesses only.
3. This timing parameter is the sum of the number listed and the product of the CLK COUNT times the period of the CPU clock.
   eg: $t_{21} = -5 + (0.5 \times t_{KCLK})$ ns
4. This parameter assumes that a 40ns delay line is used to generate ADLY, BDLY, $\overline{VDSDLY}$, and $\overline{VDTKDLY}$.
5. In the case of RMW cycles, the release time of $\overline{KRMC}$ controls the release of $\overline{VAS}$ when the TASCON bit is set. The release of $\overline{KRMC}$ controls the release of VADDR, VAM, and $\overline{VRMC}$ regardless of the state of the TASCON bit.
6. The minimum low time for VAS is ($3 \times t_{KCLK} - 5$ns) and may override this parameter, depending on the Slave Response time.
7. If the loading on the two outputs is equal, the skew can be reduced to 2ns.
8. This parameter assumes that previous VMEbus cycle is complete and that VMEbus ownership can be taken without further delay.

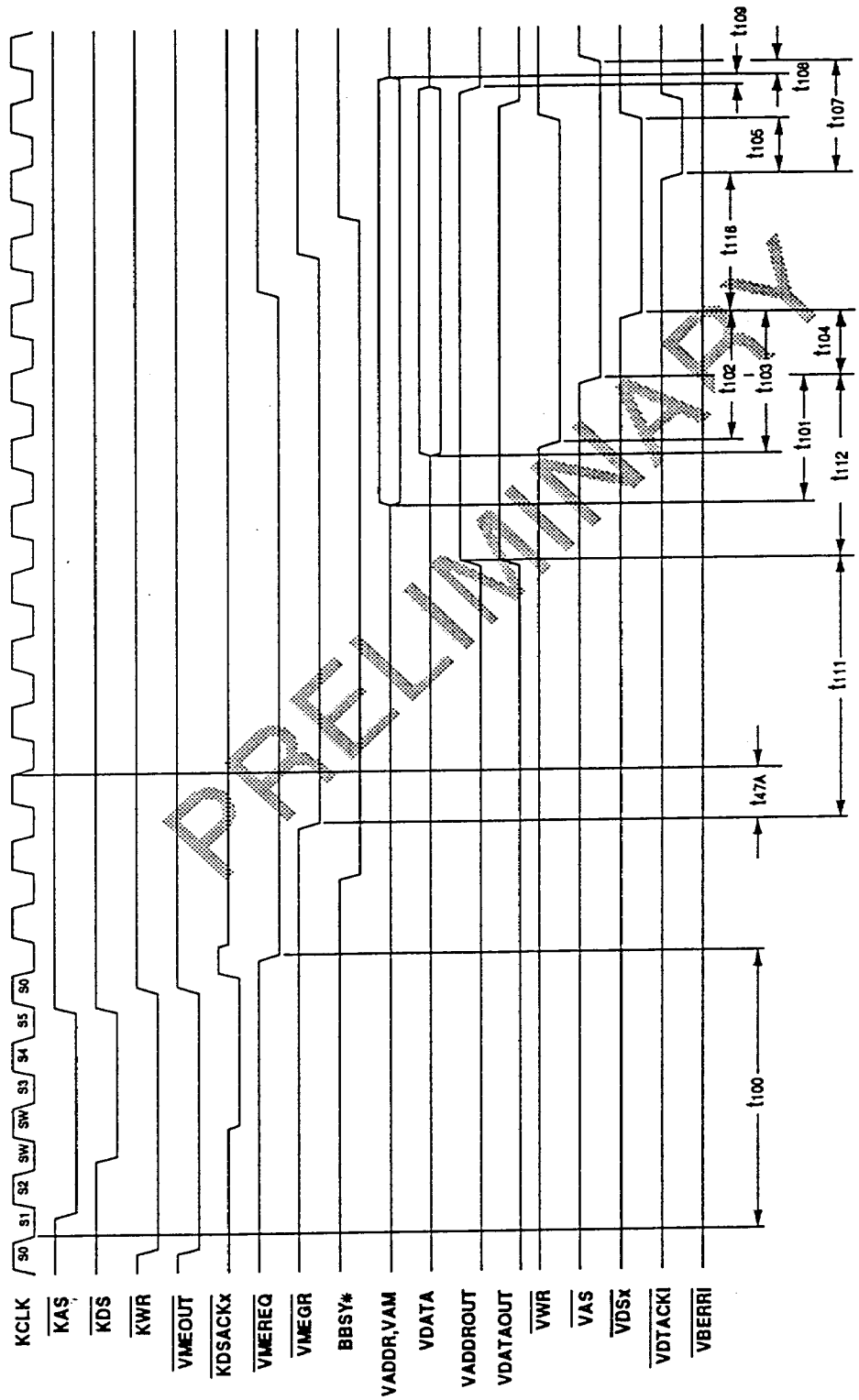





Figure 10a : DARF VME MASTER INTERFACE, SINGLE DECOUPLED WRITE

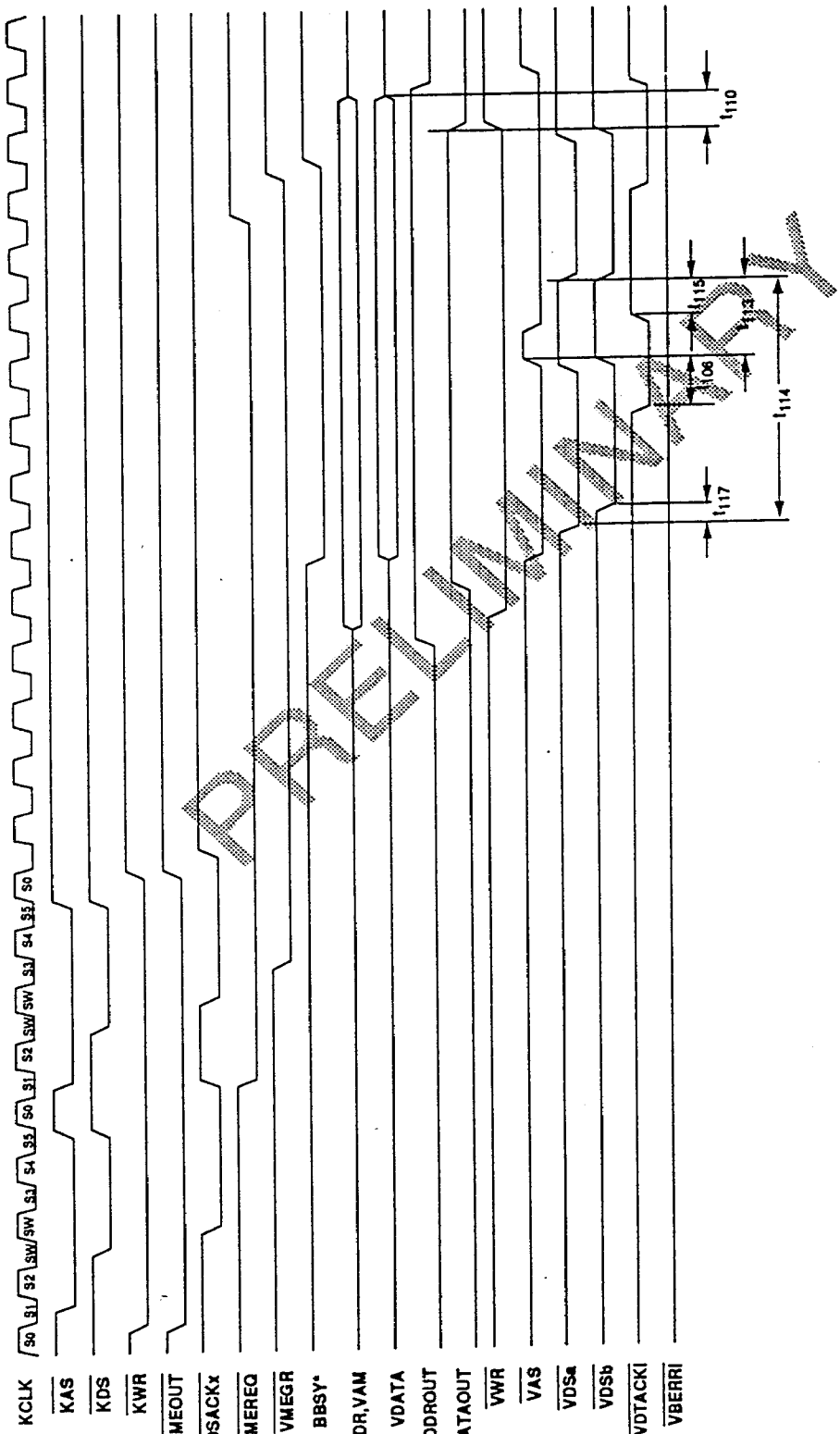



Figure 10b : DARF VME MASTER INTERFACE, MULTIPLE DECOUPLED WRITE

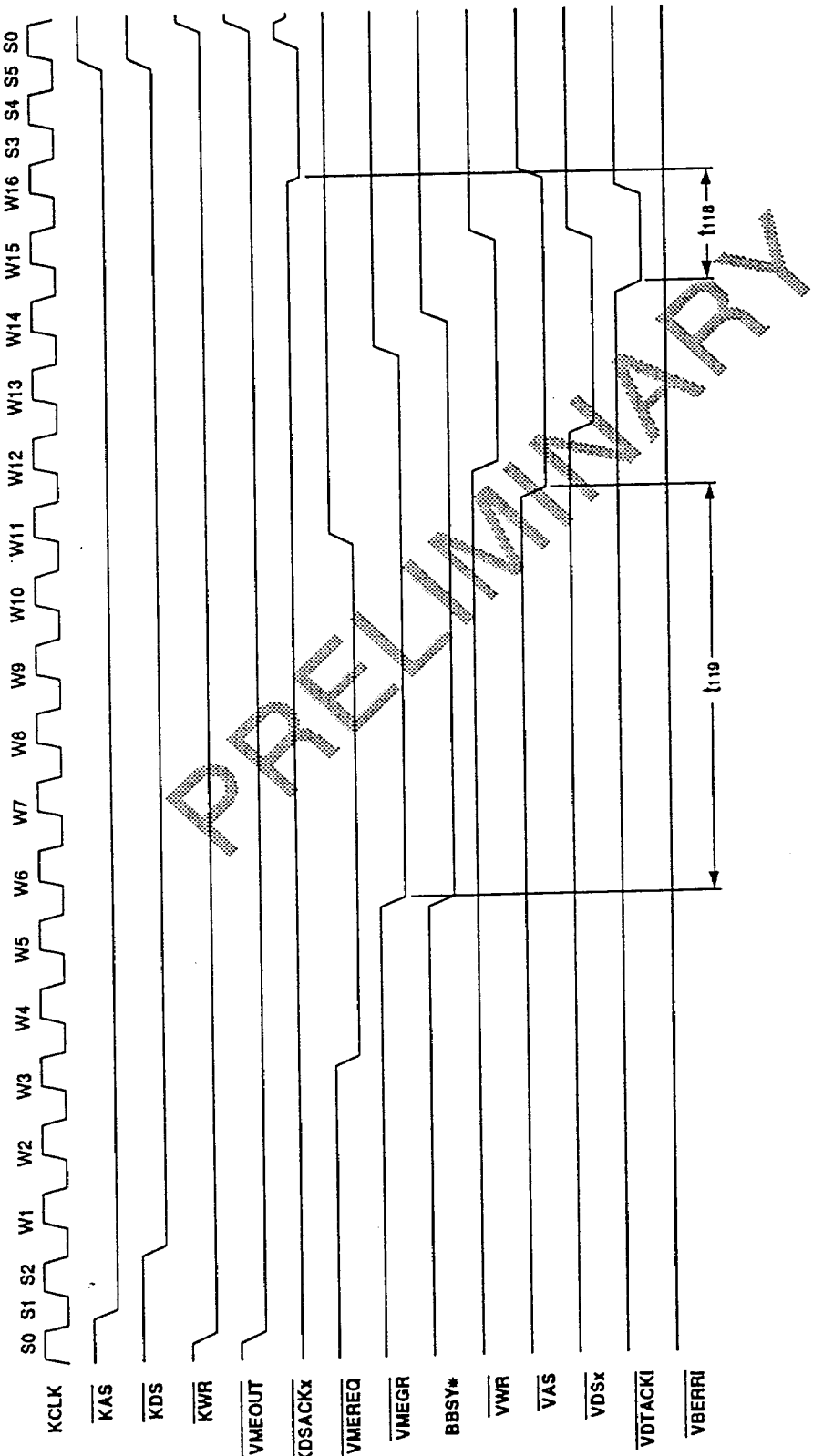





Figure 11 : DARF VME MASTER INTERFACE, ATOMIC WRITE

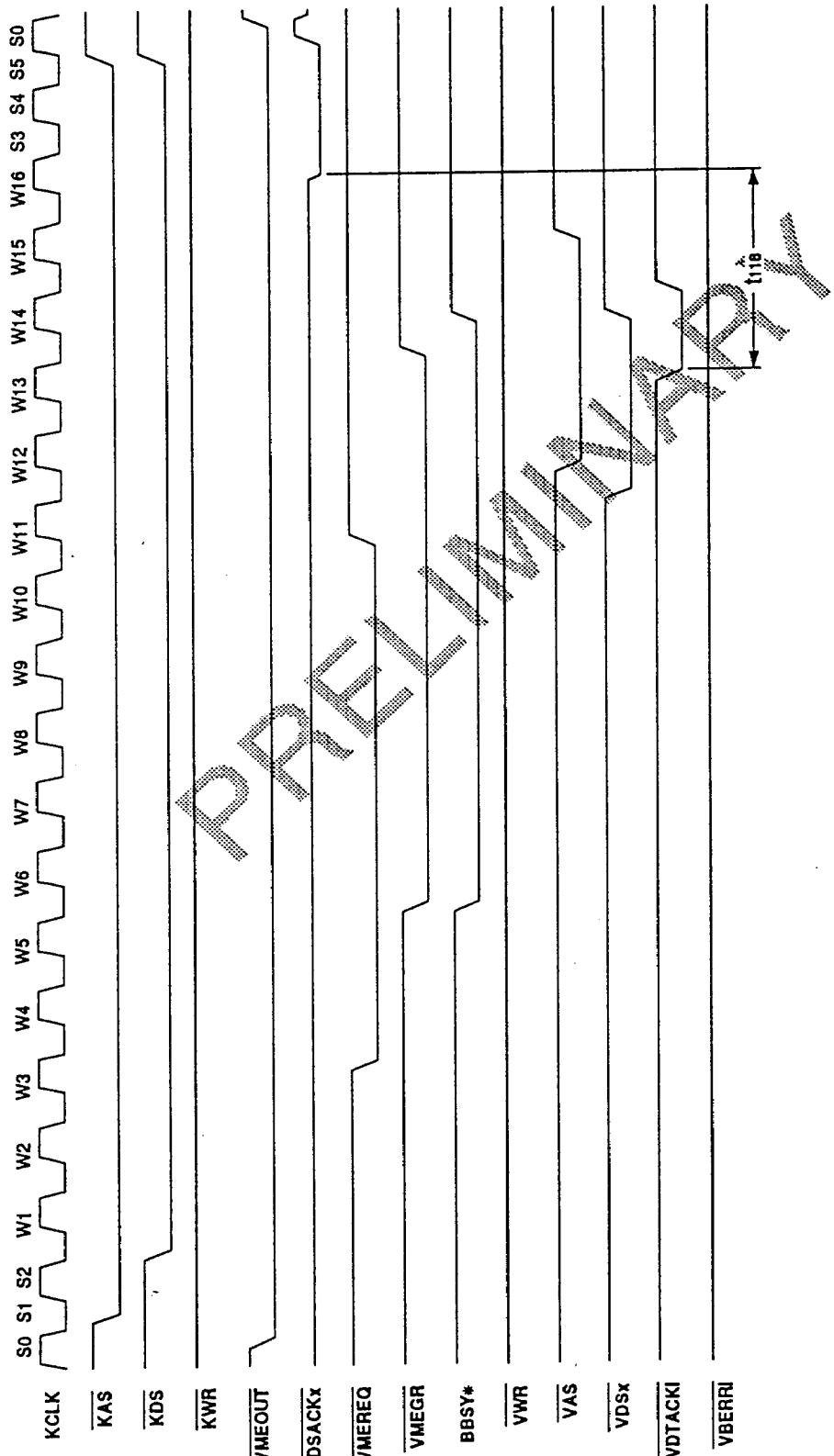





**Figure 12 : DARF VME MASTER INTERFACE, SINGLE READ**

**Figure 13 : DARF DELAY LINE TIMING, VMEbus MASTER CYCLES**

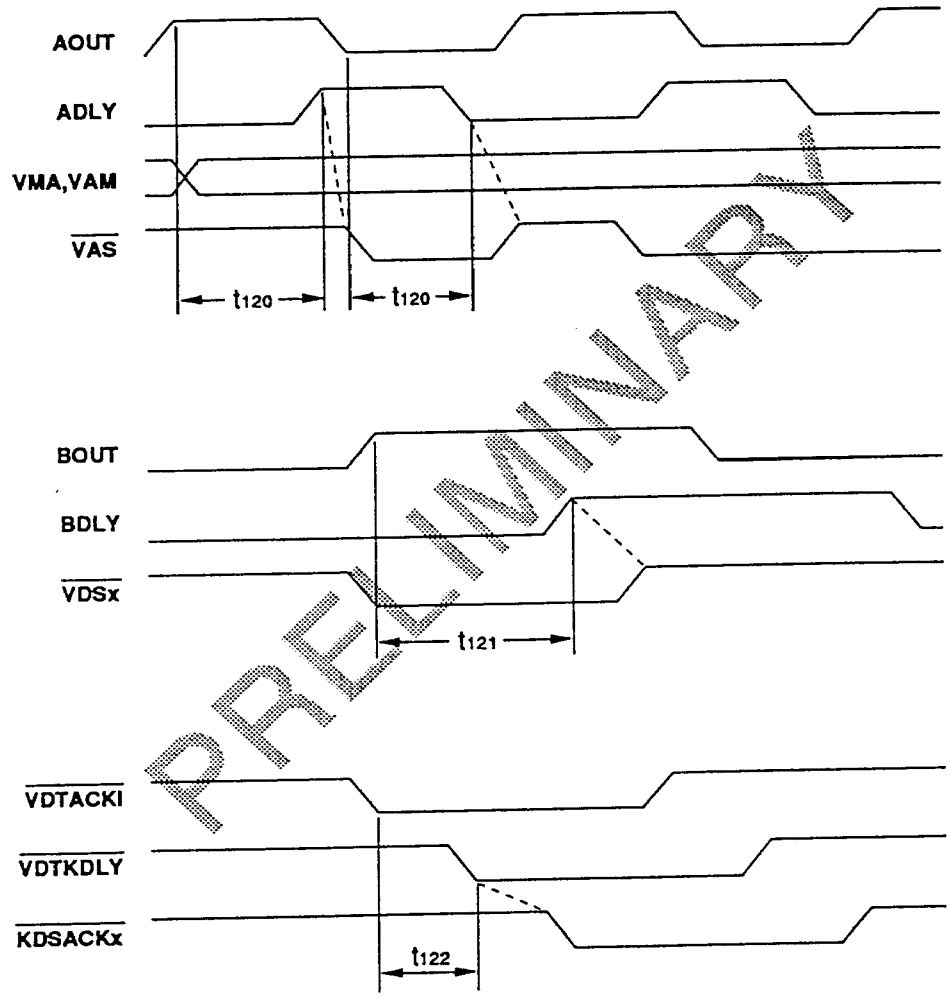


**Figure 14 : DARF MASTER INTERFACE, VMEbus Iack CYCLE**

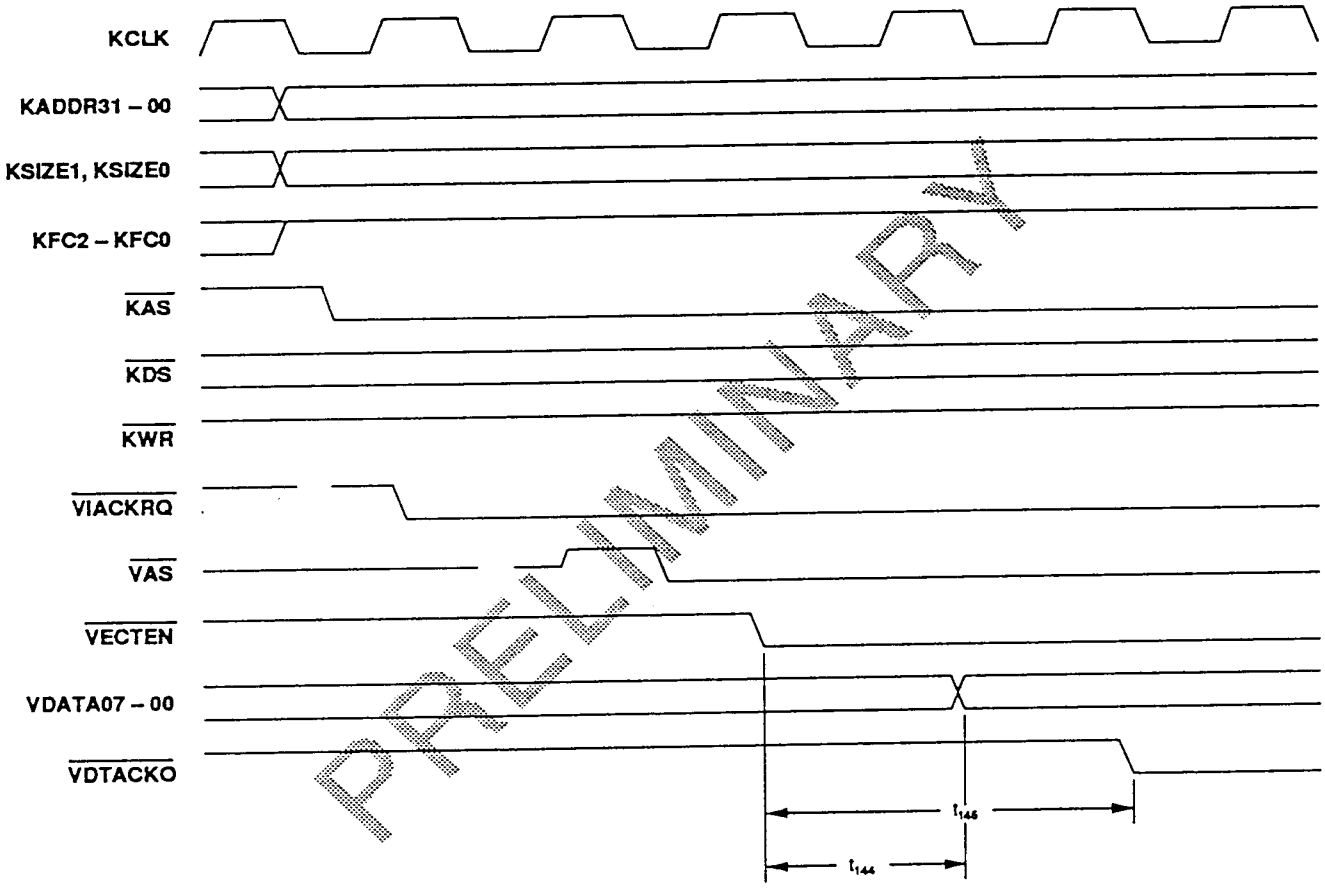


**Table 8 : AC CHARACTERISTICS (DARF VMEbus SLAVE INTERFACE)**
**(Commercial $T_A$ = 0° to +70°C, $V_{DD}$ = 5V ± 5%, Military $T_A$ = –55° to +125°C, $V_{DD}$ = 5V ± 10%)**

| Symbol | Description | Clk Count | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| | | | | Com | Mil | |
| $t_{48}$ | $\overline{KDSACK}$ asserted to KBERR low (Notes 3, 8) | 2.5 | - | 0 | 0 | ns |
| $t_{130}$ | VADDR, VAM, $\overline{VLWORD}$, $\overline{VIACK}$ setup to $\overline{VAS}$ low | - | 5 | - | - | ns |
| $t_{131}$ | $\overline{VAS}$ low to $\overline{VASDLY}$ low | - | 15 | 25 | 25 | ns |
| $t_{132}$ | VDATA, $\overline{VWR}$ setup to $\overline{VDSa}$ low | - | 5 | - | - | ns |
| $t_{133}$ | $\overline{VDSn}$ edge to $\overline{VDSDLY}$ edge | - | 35 | 45 | 45 | ns |
| $t_{134}$ | VME slave response, RXFIFO write, FIFO space available (Note 4) | 3/4 | 45 | 65 | 70 | ns |
| $t_{135}$ | VME slave response, LM write, FIFO space available (Note 4) | | 50 | 75 | 80 | ns |
| $t_{136}$ | VME slave response, LM write, FIFO full (Note 4) | 6/7 | 50 | 75 | 80 | ns |
| $t_{137}$ | VME slave response, Atomic (minimum) (Note 5) | 11.5/12.5 | 4 | 35 | 40 | ns |
| $t_{138}$ | $\overline{VDSa}$ low to $\overline{LMINT}$ asserted (Note 1 & 4) | 1.5/2.5 | 50 | 85 | 90 | ns |
| $t_{139}$ | $\overline{VDSa}$ low to $\overline{VBERRO}$ asserted, illegal VMEin cycle (Note 2, 4 & 6) | - | 45 | 65 | 70 | ns |
| $t_{140}$ | $\overline{VDSb}$ high to $\overline{VDTACKO}$ negated, VMEbus write cycle to DARF | - | 5 | 30 | 35 | ns |
| $t_{140A}$ | $\overline{VDSb}$ high to $\overline{VDTACKO}$ negated, VMEbus read cycle to DARF (Note 4) | - | 45 | 70 | 75 | ns |
| $t_{141}$ | VDATAOUT negated to $\overline{VDTACKO}$ negated | - | –1 | 0 | 1 | ns |
| $t_{142}$ | VADDR, VAM, $\overline{VLWORD}$, $\overline{VIACK}$ hold time from $\overline{VDTACKO}$ low | - | 0 | - | - | ns |
| $t_{143}$ | $\overline{VDSn}$ low to $\overline{LBRQ}$ asserted, | 2/3 | 3 | 20 | 25 | ns |
| $t_{144}$ | $\overline{VECTEN}$ low to VDATA asserted (Note 3) | 0.5/1.5 | 6 | 35 | 40 | ns |
| $t_{145}$ | $\overline{VECTEN}$ low to VDTACKO asserted (Note 3) | 2/3 | 3 | 20 | 25 | ns |
| $t_{146}$ | $\overline{VDSDLY}$ low to $\overline{VDTACKO}$ asserted, Decoupled VMEin cycle (Note 1) | - | 4 | 24 | 27 | ns |
| $t_{147}$ | $\overline{KDSACKn}$ low to $\overline{VDTACKO}$ asserted BERRCHK = 0 (Note 3) | 1.5/2.5 | 6 | 32 | 39 | ns |
| $t_{147A}$ | $\overline{KDSACKn}$ low to $\overline{VDTACKO}$ asserted BERRCHK = 1 (Note 3) | 2.5/3.5 | 6 | 32 | 39 | ns |
| $t_{148}$ | KCLK high to $\overline{VBERRO}$ or $\overline{VDTACKO}$ asserted, Atomic VMEin cycle | - | 6 | 32 | 39 | ns |
| $t_{149}$ | Pulse width, late $\overline{KBERR}$ width (Note 7) | - | 10 | $t_{CLK}$ | $t_{CLK}$ | ns |

*Notes: see next page*

Notes:

1. This parameter assumes that there is space in the Message/Receive FIFO to receive the data.
2. This parameter applies only to accesses to protected memory and Message FIFO read cycles.
3. This timing parameter is the sum of the number listed and product of the CLK COUNT times the period of the CPU clock.

   eg: $t_{21} = -5 + (0.5 \times t_{KCLK})$ ns
4. This parameter assumes that a 40ns delay line is used to generate ADLY, BDLY, $\overline{VDSDLY}$, and $\overline{VDTKDLY}$.
5. This slave response parameter assumes that the $\overline{LBGR}$ is returned in time to be sampled on the next falling edge of KCLK after $\overline{LBRa}$ is asserted. Additional clocks will have to be added to account for bus arbitration time.
6. This parameter applies when an illegal access to the DARF is attempted by the VMEbus, i.e, read access to the location monitor or illegal access to protected memory.
7. When $\overline{KBERR}$ is received late, it is latched internally for the DARF's use. $\overline{KBERR}$ needs to be negated before the next local bus cycle starts.
8. This specification applies to the first KDSACKn signal asserted. In the absence of KDSACKn, KBERR is an asynchronous input using the asynchronous input setup time ($t_{47}$). Timing paramter $t_{27A}$ must also be met for a late KBERR.

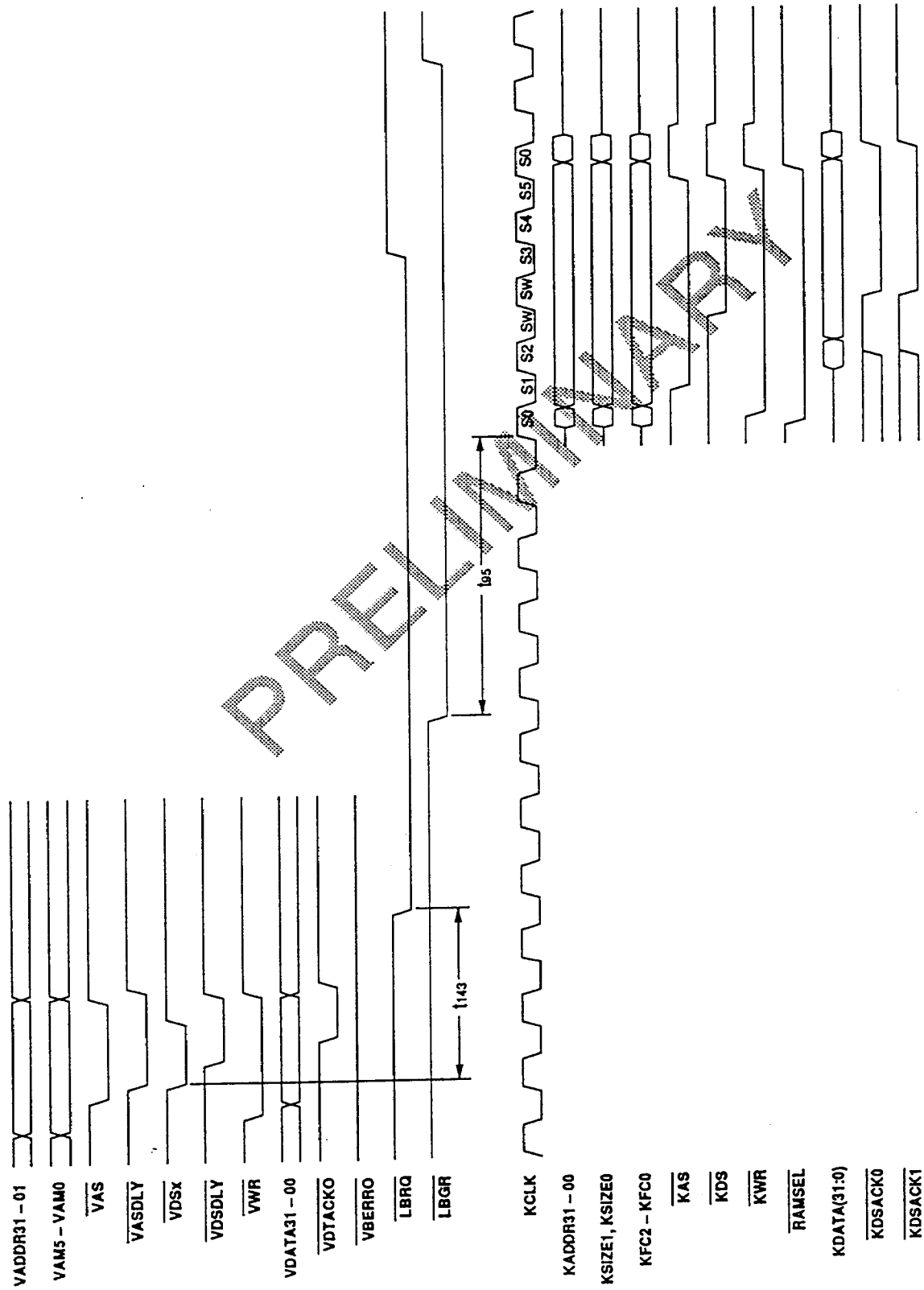



Figure 15 : DARF SLAVE INTERFACE, VME DECOUPLED WRITE

**Figure 16 : DARF VME SLAVE INTERFACE, DECOUPLED WRITE**

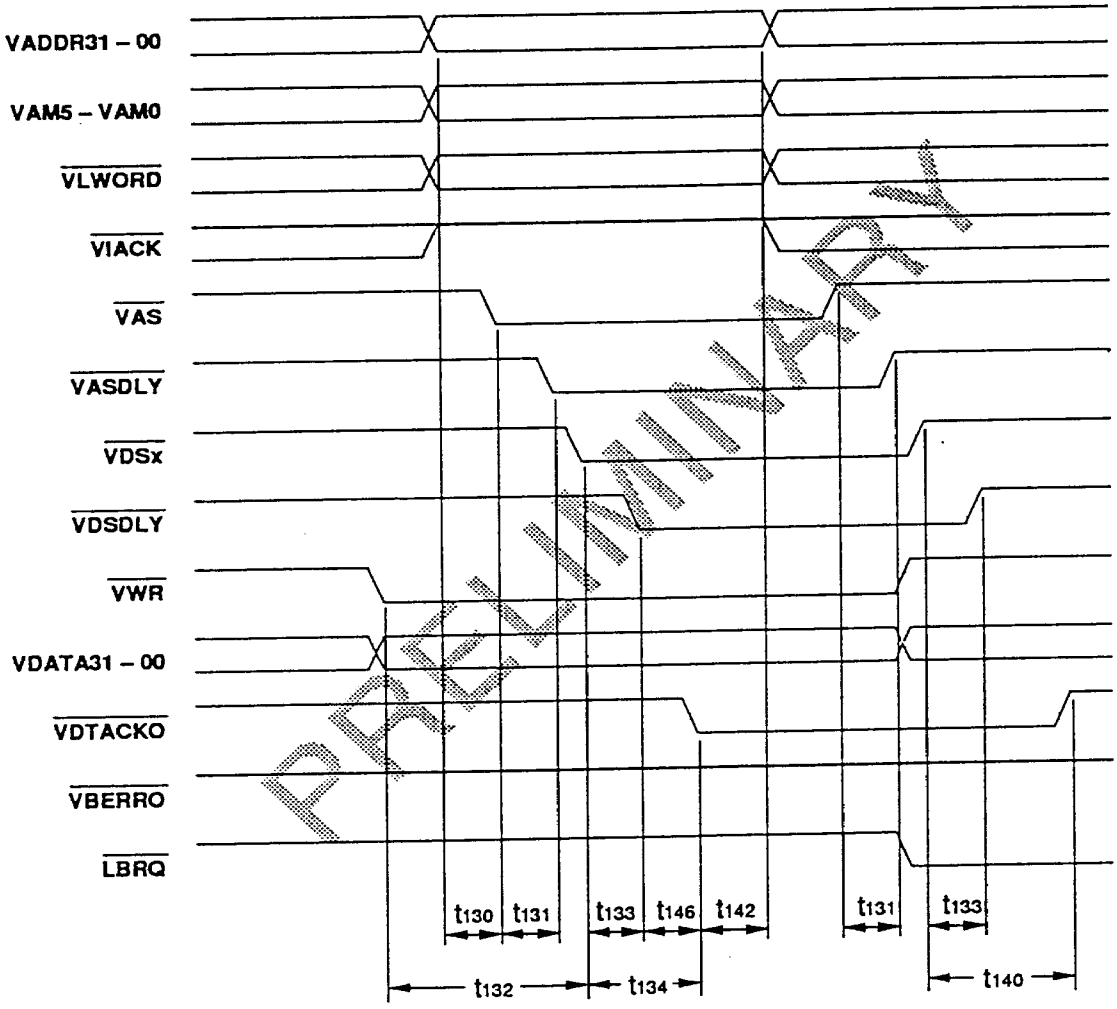
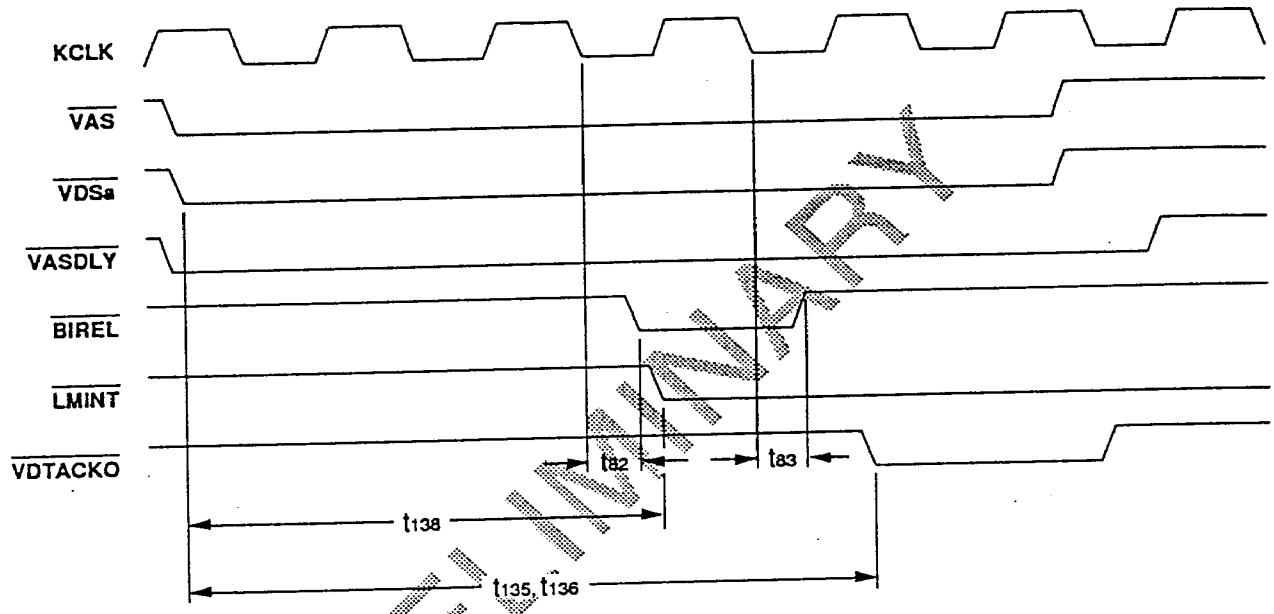


**Figure 17 : VMEbus SLAVE INTERFACE, LOCATION MONITOR WRITE**




Note:
The Slave Response time for Location Monitor writes is extended an additional 3 clocks if the CPU is writing to the FIFO when the VMEin cycle occurs.

**Figure 18a : DARF SLAVE INTERFACE, MEMORY READ with BERRCHK CLEARED**

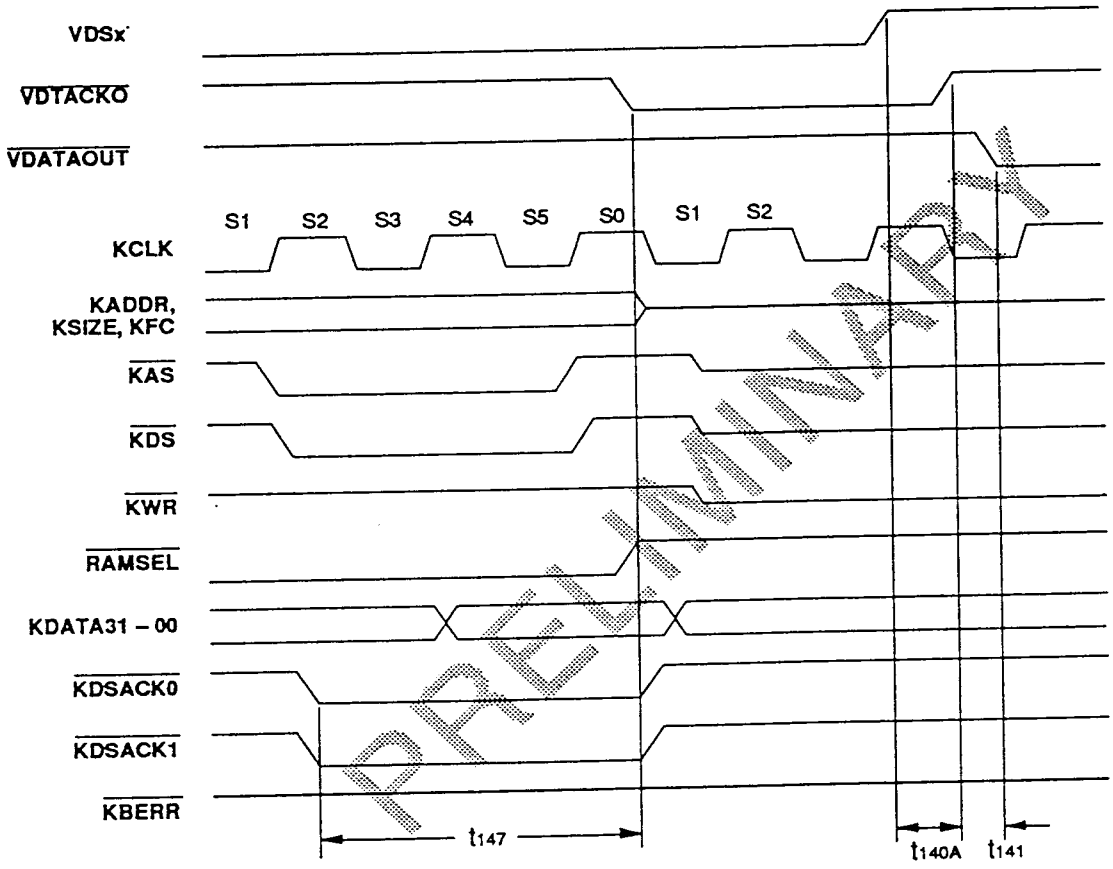


**Figure 18b : DARF SLAVE INTERFACE, MEMORY READ with BERRCHK SET**

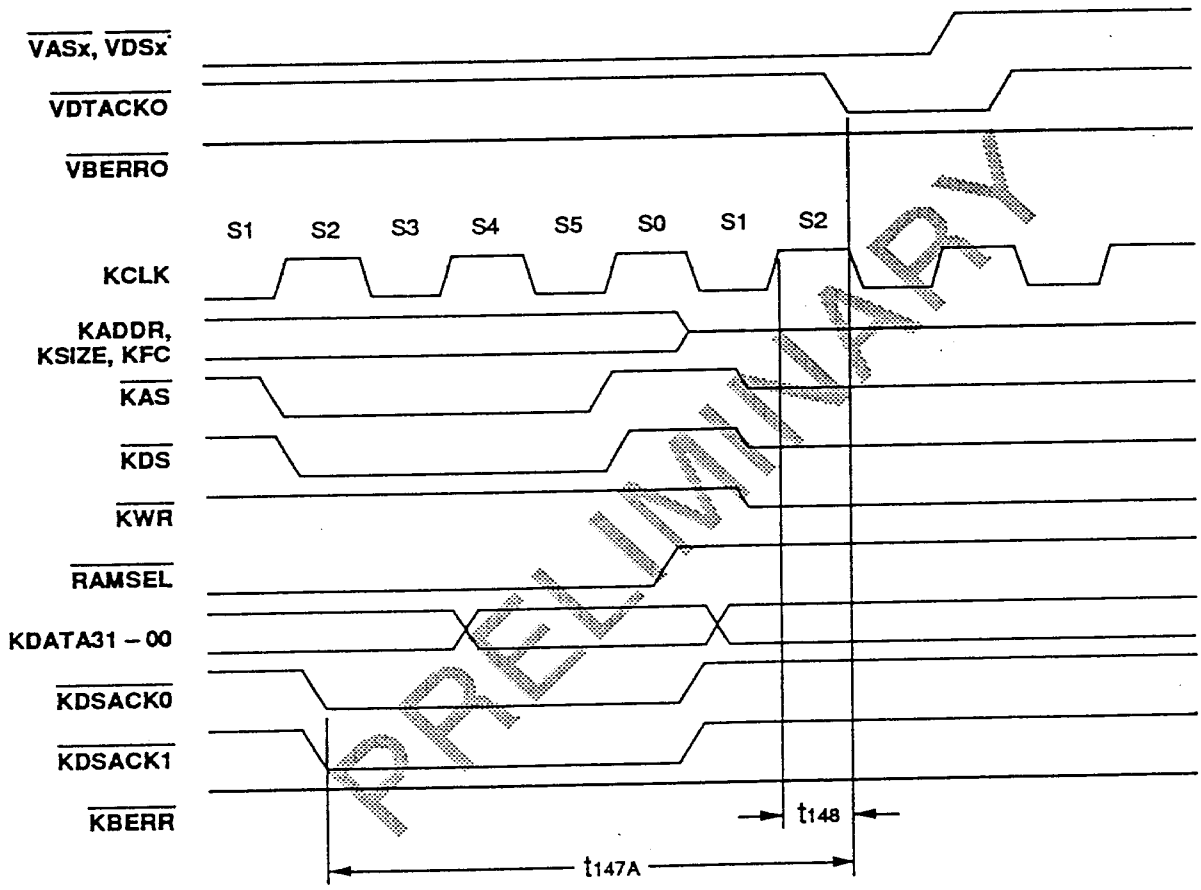


**Figure 19 : DARF SLAVE INTERFACE, MEMORY READ with LATE KBERR**

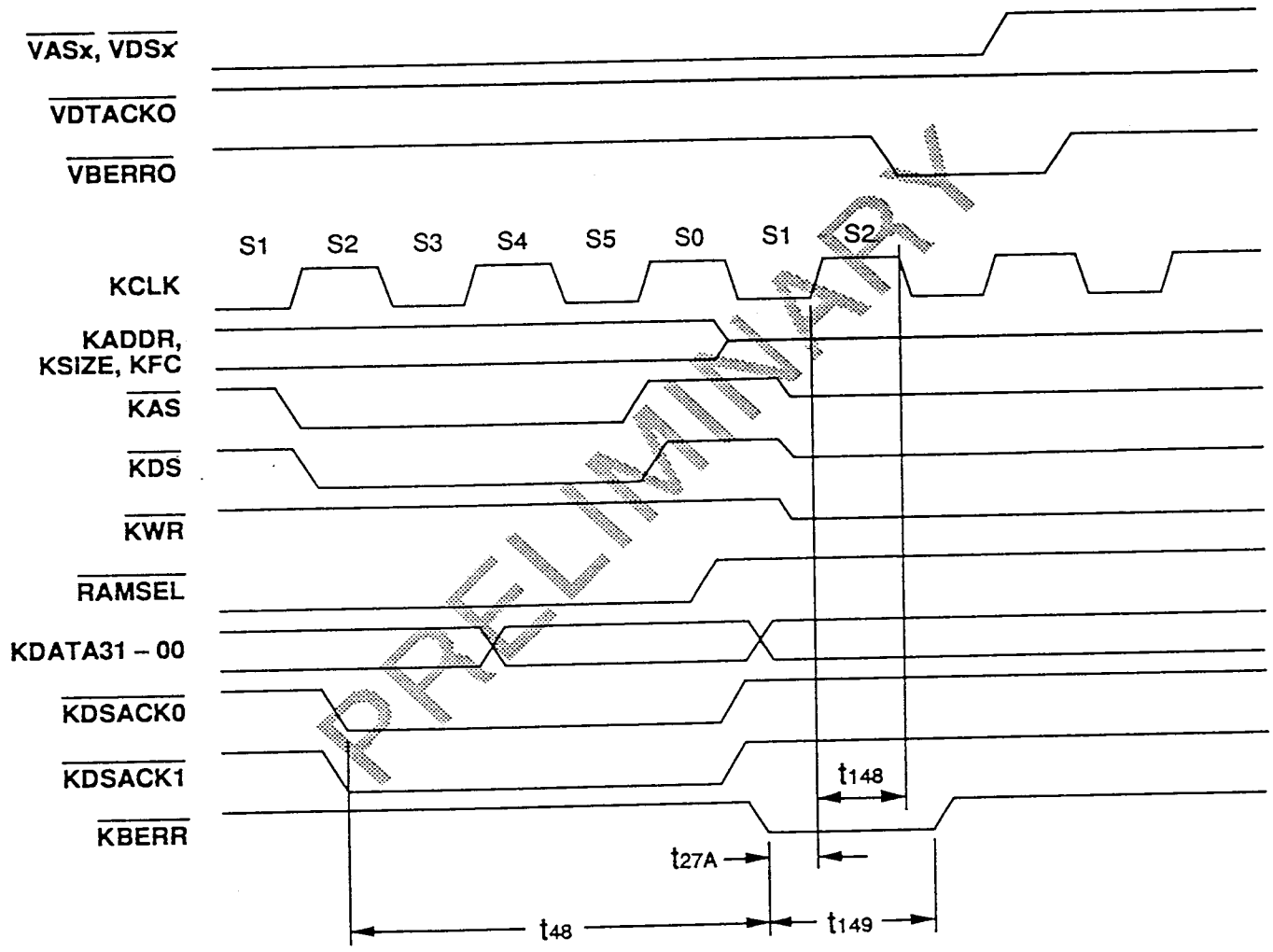
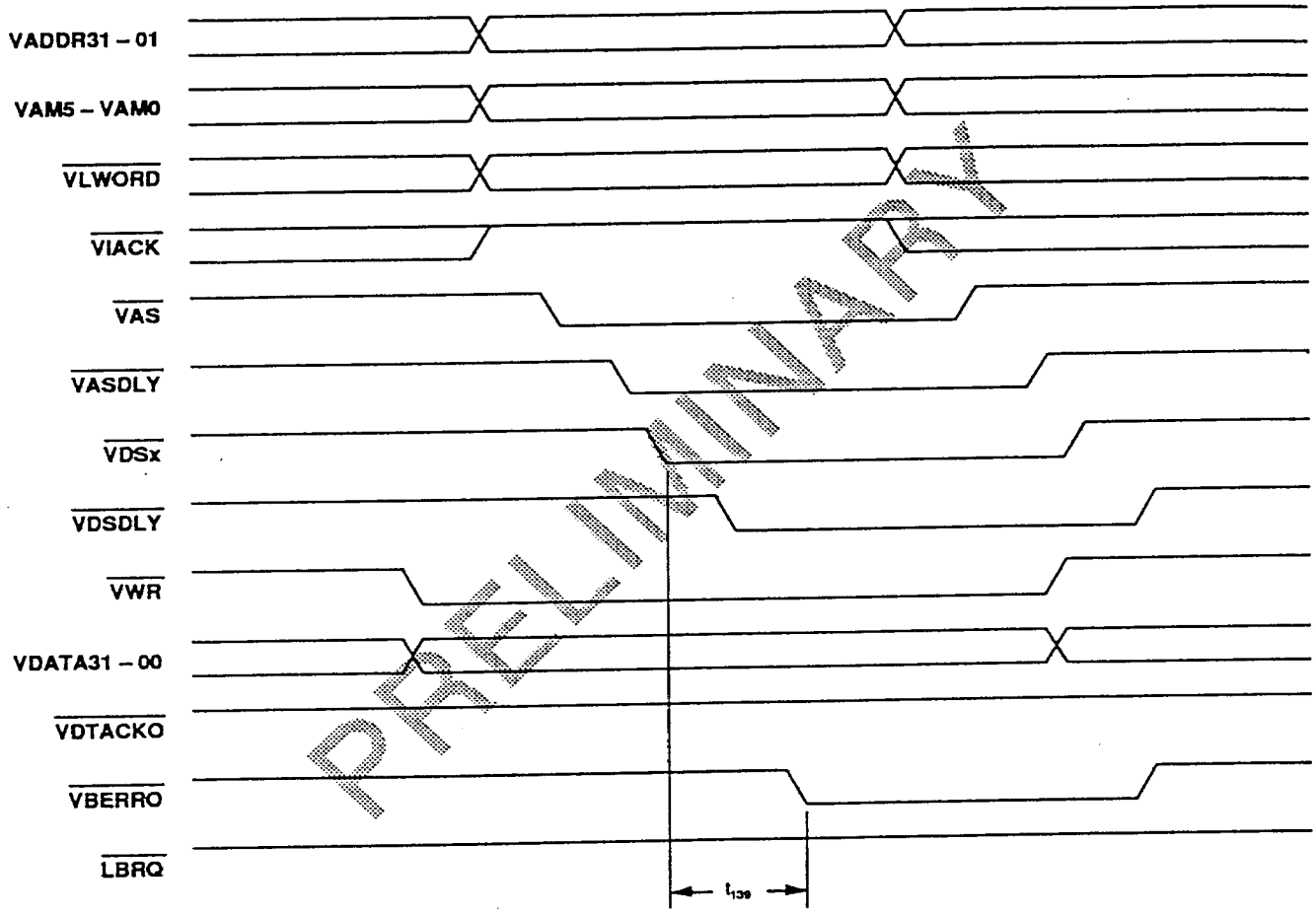


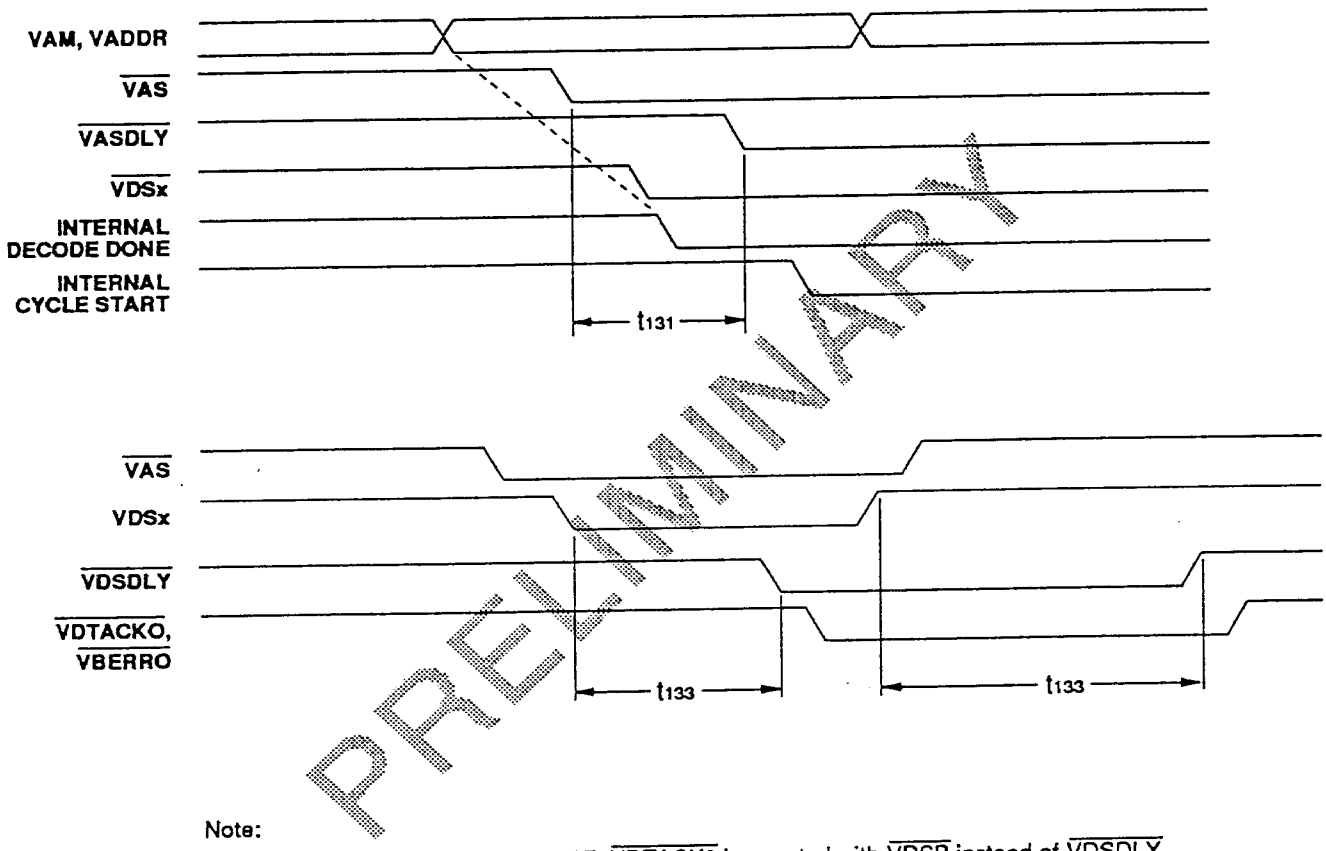
**Figure 20 : DARF VME SLAVE INTERFACE, ILLEGAL ACCESS**






Note:
This timing applies to VMEbus attempts to read the Location Monitor or to illegally access protected memory.

**Figure 21 : DARF DELAY LINE TIMING, VMEbus SLAVE CYCLES**






Note:
On VMEbus write cycles to the DARF, $\overline{\text{VDTACK0}}$ is negated with $\overline{\text{VDSB}}$ instead of $\overline{\text{VDSDLY}}$.

**Table 9 : AC CHARACTERISTICS (DARF64 BLOCK TIMING – Start, Data Phase and Address Boundary)**
**(Commercial $T_A$ = 0° to +70°C, $V_{DD}$ = 5V ± 5%, Military $T_A$ = –55° to +125°C, $V_{DD}$ = 5V ± 10%)**

| Symbol | Description | Clk Count | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| | | | | Com | Mil | |
| $t_{150}$ | $\overline{VAS}$ asserted to $\overline{VDSa}$ asserted (Note 1) | - | 0 | 5 | | ns |
| $t_{151}$ | $\overline{VDTACKI}$ low to $\overline{VDSb}$ negated, All atomic cycles (Note 5) | - | 45 | 70 | | ns |
| $t_{152}$ | $\overline{VDTACKI}$ low to $\overline{VDSb}$ negated, All decoupled cycles | - | 5 | 25 | | ns |
| $t_{153}$ | $\overline{VDTACKI}$ low to $\overline{VAS}$ negated, decoupled | - | 5 | 35 | 40 | ns |
| $t_{154}$ | $\overline{VDTACKI}$ low to $\overline{VAS}$ negated, atomic (Note 5) | - | 55 | 125 | | ns |
| $t_{155}$ | $\overline{VMEGR}$ low to VADDROUT, VDATAOUT high | 2/3 | 4 | 25 | | ns |
| $t_{157}$ | VADDROUT high to VAS low | 0/1 | 41 | 75 | | ns |
| $t_{158}$ | $\overline{VAS}$, $\overline{VDSn}$ high time: Preceding data cycle | - | 45 | 70 | - | ns |
| | Preceding BLT, MBLT address cycle | 2/4 | 45 | 100 | | ns |
| $t_{159}$ | $\overline{VDTACKI}$ high to $\overline{VDSa}$ asserted | - | 5 | 25 | - | ns |
| $t_{160}$ | $\overline{VDSa}$ low to $\overline{VDTACKI}$ asserted (Note 2) | - | 30 | | - | ns |
| $t_{161}$ | $\overline{VDSa}$ low to $\overline{VDSb}$ low | - | 0 | 5 | 7 | ns |
| $t_{162}$ | $\overline{VMEGR}$ low to $\overline{VAS}$ low | 3/4 | 50 | 100 | | ns |
| $t_{163}$ (Note 3) | $\overline{VDSa}$ low to $\overline{VDTACKO}$ low All decoupled writes, all decoupled BLT address phase and all MBLT address phase | - | 44 | 64 | | ns |
| | Atomic non-block and BLT writes, non-block and BLT reads (given $\overline{LBGR}$ is $1t_C$ after $\overline{LBRQ}$ and zero wait state RAM) | 8/11 | 0 | 50 | | ns |
| | MBLT atomic reads and writes (given $\overline{LBGR}$ is $1t_C$ after $\overline{LBRQ}$ and zero wait state RAM) | 11/14 | 0 | 50 | | ns |
| $t_{164}$ | $\overline{VDSa}$ low to $\overline{VDTACKO}$ low, atomic | 11.5/12.5 | 4 | 35 | | ns |
| $t_{165}$ | $\overline{VDSa}$ high to $\overline{VDTACKO}$ high, decoupled | - | 5 | 30 | | ns |
| $t_{166}$ | $\overline{VDSa}$ high to $\overline{VDTACKO}$ high, atomic (Note 5) | - | 45 | 70 | | ns |
| $t_{167}$ | $\overline{VDSa}$ low to $\overline{VDTACKO}$ low, decoupled writes | (Note 4) | 4 | 24 | | ns |
| $t_{168}$ | Time for ACC to issue VMEbus grant to DARF64 | - | | | | ns |
| $t_{169}$ | Buffer delay time | - | | | | ns |
| $t_{170}$ | Control signal buffer time | - | | | | ns |
| $t_{171}$ | DS1*, DS0* receiver time | - | | | | ns |
| $t_{172}$ | DS* delay line and DS1*, DS0* OR | - | | | | ns |
| $t_{173}$ | Delay time through VMEbus buffer | - | | | | ns |

*Notes: see next page*

Notes:

1. This time guarantees that $\overline{VDS}$ will not be asserted before $\overline{VAS}$, except for possible skew through the VAS and VDS buffer.
2. Any assertion before this range of times is ignored. This threshold is set using the same delay line used to set DS* high and low times
3. This parameter can vary depending upon whether the block is a read or write, and whether the slave is in atomic or decoupled mode.
4. This parameter is a combination of $t_{163}$ and a 40ns DSDLY line. Use $t_{163}$ for a system specification and $t_{167}$ for a DARF64 specification.
5. Slave reads in blockmode are atomic.



**Figure 22 : BLOCK START TIMING**

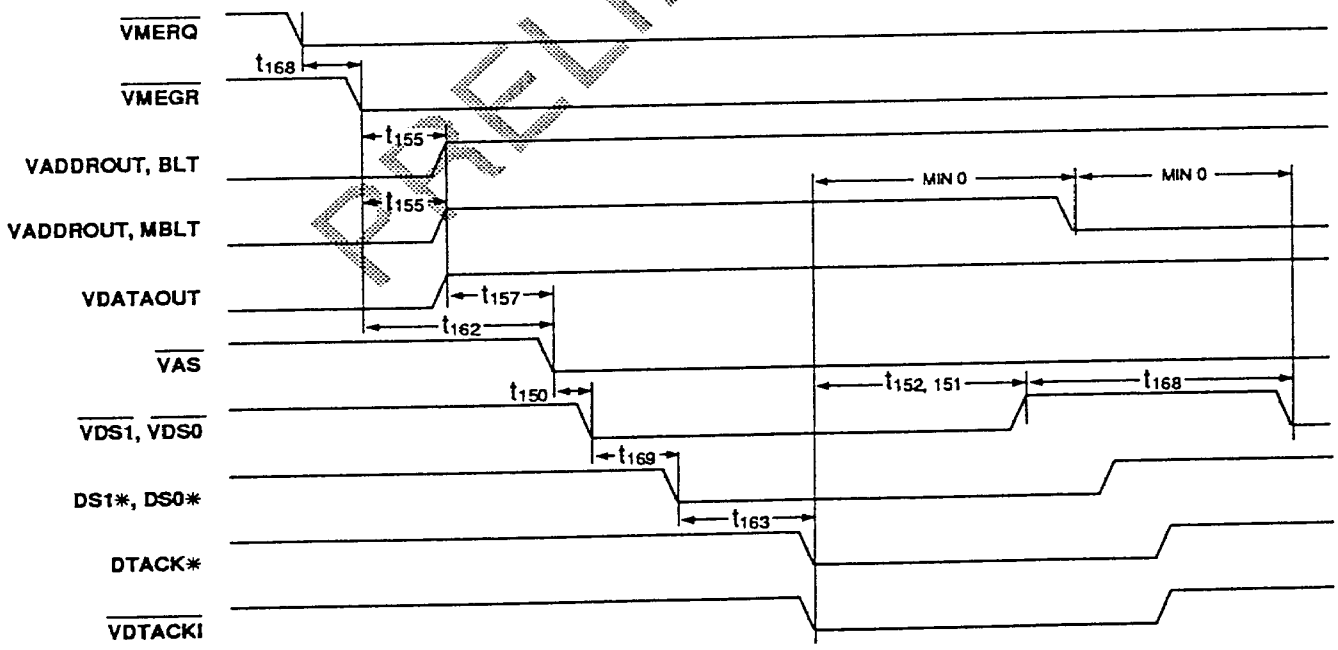


**Figure 23 : BLOCK DATA PHASE TIMING**

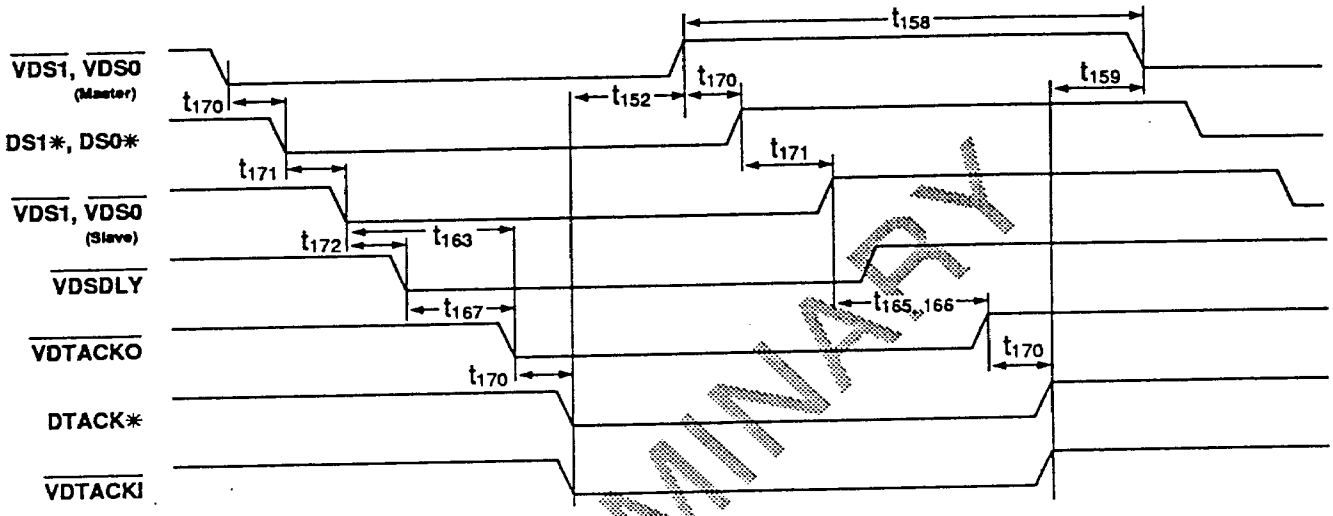





**Figure 24 : BLOCK ADDRESS BOUNDARY TIMING**

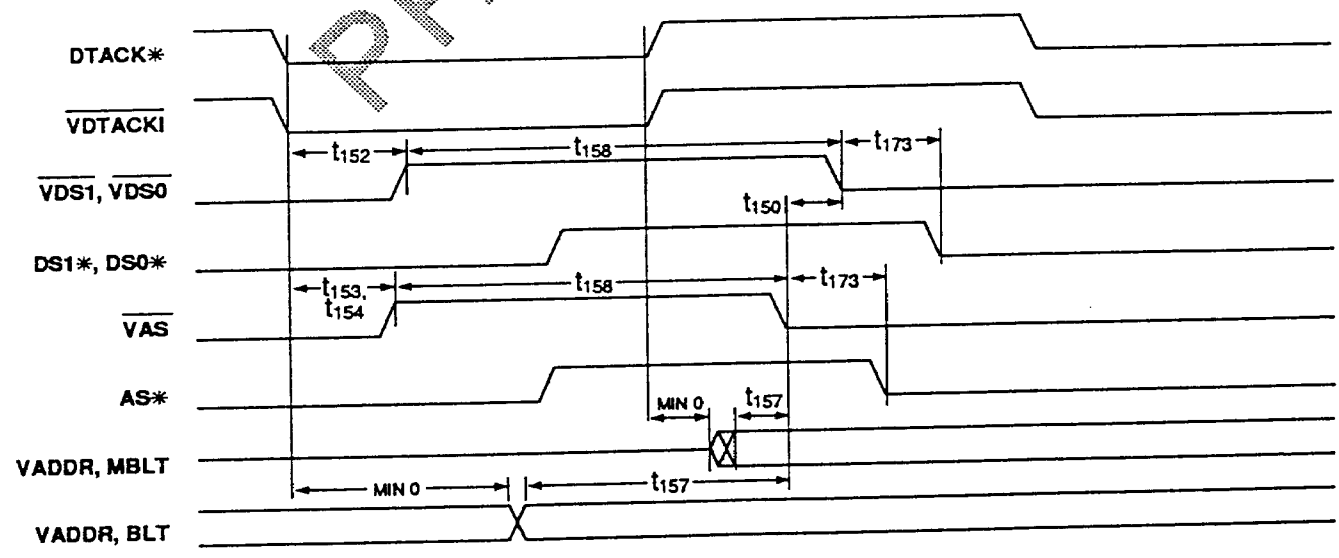


**Table 10 : DC CHARACTERISTICS**
**(Commercial $T_A$ = 0° to +70°C, $V_{DD}$ = 5V ± 5%, Military $T_A$ = –55° to +125°C, $V_{DD}$ = 5V ± 10%)**

| Symbol | Parameter | Test Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $I_{IH}$ | Input HIGH Current | $V_{IN} = V_{DD}$ | | | | |
| | CTTL | | - | 1 | 10 | µA |
| | CTTL PU | | - | - | 40 | µA |
| $I_{IL}$ | Input LOW Current | $V_{IN}=V_{SS}$ | | | | |
| | CTTL | | - | –1 | –10 | µA |
| | CTTL PU | | –5 | –30 | –100 | µA |
| $I_{OZ}$ | Tri-state Output Leakage Current | | –10 | ±1 | 10 | µA |
| $V_{IL}$ | Input LOW Voltage | | | | | |
| | CTTL | | - | - | 0.8 | V |
| | CTTL PU | | - | - | 0.8 | V |
| | CMOS | –55° to +125°C | | - | 0.3VDD | V |
| $V_{IH}$ | Input HIGH voltage | | | | | |
| | CTTL | 0° to 70°C | 2.0 | - | - | V |
| | CTTL PU | 0° to 70°C | 2.0 | - | - | V |
| | CTTL | –55° to +125°C | 2.25 | - | - | V |
| | CTTL PU | –55° to +125°C | 2.25 | - | - | V |
| | CMOS | –55° to +125°C | 0.7VDD | - | - | V |
| $V_{OH}$ | Voltage Output HIGH | 0° to 70°C | | | | |
| | TP2 | $I_{OH}$ = –2 mA | 2.4 | 4.5 | - | V |
| | TP4 | $I_{OH}$ = –4 mA | 2.4 | 4.5 | - | V |
| | TS4 | $I_{OH}$ = –4 mA | 2.4 | 4.5 | - | V |
| | TS2 SR | $I_{OH}$ = –2 mA | 2.4 | 4.5 | - | V |
| | TS4 SR | $I_{OH}$ = –4 mA | 2.4 | 4.5 | - | V |
| | TS6 | $I_{OH}$ = –6 mA | 2.4 | 4.5 | - | V |
| | TS8 | $I_{OH}$ = –8 mA | 2.4 | 4.5 | - | V |
| $V_{OH}$ | Voltage Output HIGH | –55° to 125°C | | | | |
| | TP2 | $I_{OH}$ = –1.6 mA | 2.4 | 4.5 | - | V |
| | TP4 | $I_{OH}$ = –3.2 mA | 2.4 | 4.5 | - | V |
| | TS4 | $I_{OH}$ = –3.2 mA | 2.4 | 4.5 | - | V |
| | TS2 SR | $I_{OH}$ = –1.6 mA | 2.4 | 4.5 | - | V |
| | TS4 SR | $I_{OH}$ = –3.2 mA | 2.4 | 4.5 | - | V |
| | TS6 | $I_{OH}$ = –4.8 mA | 2.4 | 4.5 | - | V |
| | TS8 | $I_{OH}$ = –6.4 mA | 2.4 | 4.5 | - | V |

**Table 10 : DC CHARACTERISTICS CON'T**
**(Commercial $T_A$ = 0° to +70°C, $V_{DD}$ = 5V ± 5%, Military $T_A$ = –55° to +125°C, $V_{DD}$ = 5V ± 10%)**

| Symbol | Parameter | Test Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{OL}$ | Voltage Output LOW | 0° to 70°C | | | | |
| | TP2 | $I_{OL}$ = 2 mA | - | 0.2 | 0.4 | V |
| | TP4 | $I_{OL}$ = 4 mA | - | 0.2 | 0.4 | V |
| | TS4 | $I_{OH}$ = 4 mA | - | 0.2 | 0.4 | V |
| | TS4 SR | $I_{OH}$ = 4 mA | - | 0.2 | 0.4 | V |
| | TS6 | $I_{OL}$ = 6 mA | - | 0.2 | 0.4 | V |
| | TS8 | $I_{OL}$ = 8 mA | - | 0.2 | 0.4 | V |
| | OD8 | $I_{OL}$ = 8 mA | - | 0.2 | 0.4 | V |
| | OD12 | $I_{OL}$ = 12 mA | - | 0.2 | 0.4 | V |
| $V_{OL}$ | Voltage Output LOW | –55° to 125°C | | | | |
| | TP2 | $I_{OL}$ = 1.6 mA | - | 0.2 | 0.4 | V |
| | TP4 | $I_{OL}$ = 3.2 mA | - | 0.2 | 0.4 | V |
| | TS4 | $I_{OH}$ = 3.2 mA | - | 0.2 | 0.4 | V |
| | TS4 SR | $I_{OH}$ = 3.2 mA | - | 0.2 | 0.4 | V |
| | TS6 | $I_{OL}$ = 4.8 mA | - | 0.2 | 0.4 | V |
| | TS8 | $I_{OL}$ = 6.4 mA | - | 0.2 | 0.4 | V |
| | OD8 | $I_{OL}$ = 6.4 mA | - | 0.2 | 0.4 | V |
| | OD8 | $I_{OL}$ = 6.4 mA | - | 0.2 | 0.4 | V |
| | OD12 | $I_{OL}$ = 9.6 mA | - | 0.2 | 0.4 | V |



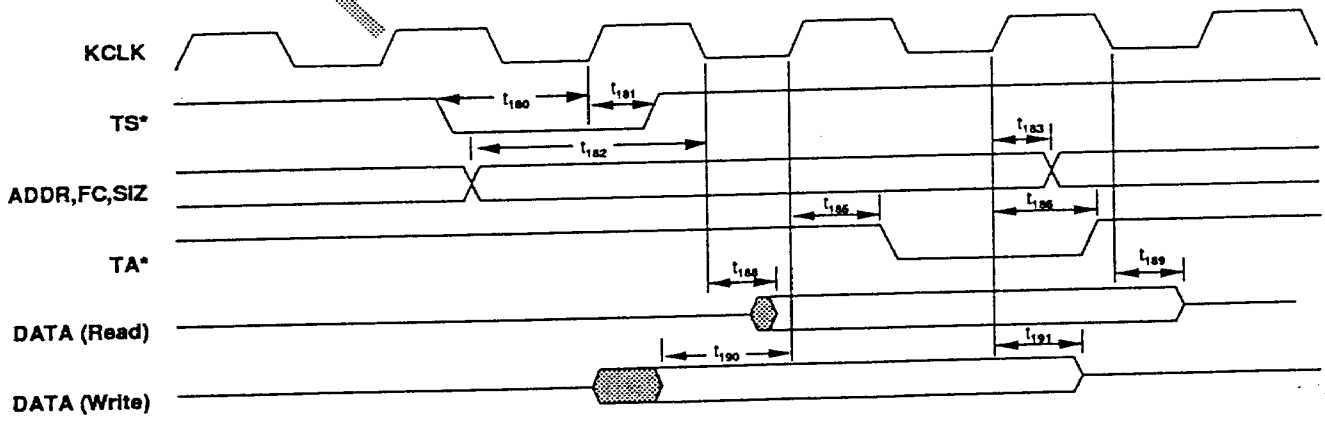
Note that the type abbreviations used above have a number suffix which indicates the current rating. The letter prefixes are defined in the Terminology section, just before Table 3.

**Table 11 : AC CHARACTERISTICS (68040 LOCAL BUS SLAVE TIMING)**
**(Commercial $T_A$ = 0° to +70°C, $V_{DD}$ = 5V ± 5%, Military $T_A$ = –55° to +125°C, $V_{DD}$ = 5V ± 10%)**

| Symbol | Description | Clk Count | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| | | | | Com | Mil | |
| $t_{180}$ | TS setup to KCLK rising | - | 10 | - | - | ns |
| $t_{181}$ | TS hold from KCLK rising | - | 10 | - | - | ns |
| $t_{182}$ | ADDR, FC, SIZ, setup to KCLK falling | - | 5 | - | - | ns |
| $t_{183}$ | KCLK rising to address hold | - | 5 | - | - | ns |
| $t_{185}$ | KCLK rising to TA asserted | - | 5 | 22 | 27 | ns |
| $t_{186}$ | KCLK rising to TA negated | - | 3 | 18 | 22 | ns |
| $t_{188}$ | KCLK falling to data valid (read) | - | - | 30 | 37 | ns |
| $t_{189}$ | KCLK falling to data high impedance (read) | - | - | 14 | 26 | ns |
| $t_{190}$ | Data setup to KCLK rising | - | - | 5 | 5 | ns |
| $t_{191}$ | Data hold from KCLK rising | - | - | 0 | 0 | ns |



**Figure 25 : 68040 LOCAL BUS SLAVE TIMING**



### Table 12 : CAPACITIVE LOADING

| Symbol | Parameter | Test Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $C_{IN}$ | Input Pin Capacitance | | - | 10 | - | pF |
| $C_{IO}$ | Bidirectional Pin Capacitance TS4, TS4 SR, TS6, TS8, OD12 | | - | 14 | - | pF |
| $C_{OUT}$ | Output Pin Capacitance TP2, TP4, OD8 | | - | 13 | - | pF |

Note that the maximum capacitive loads under recommended operating conditions for outputs driving the local bus, that is, all signals beginning with K, is 1300pF. The maximum capacitive load for all outputs is 85pF.



### Table 13 : RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| DC Supply Voltage ($V_{DD}$) | +4.5 V to +5.5 V |
| Power Dissipation ($P_{DD}$) | 1 W |
| Ambient Operating Temperature ($T_A$ Commercial) | 0° to +70°C |
| Ambient Operating Temperature ($T_A$ Military) | –55° to +125°C |

The power dissipation figure is based on typical internal logic dissipation plus the worst case set of outputs simultaneously active with maximum rated loads.

### Table 14 : ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| DC Supply Voltage ($V_{DD}$) | –0.3 to +7.0 V |
| Input Voltage ($V_{IN}$) | –0.3 to $V_{DD}$ +0.3 V |
| DC Input Current ($I_{IN}$) | –10 to +10 mA |
| Storage Temperature, ceramic ($T_{STG}$) | –65° to +150°C |
| Storage Temperature, plastic ($T_{STG}$) | –40° to +125°C |

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliablility.

## FUNCTIONAL DESCRIPTION

The DARF64 provides an address and data path to link a CPU to a VMEbus, including the logic required to perform data transfers as a master or a slave on local or VMEbus. Transmit and receive paths of the DARF64 each run in one of two operating modes: atomic or decoupled. In atomic mode, a cycle initiated on one port of the DARF64 does not finish until the DARF64 has initiated and completed that cycle on its other port. The decoupled mode allows cycles on one port to be completed and queued within the DARF64 for later dispatch to the other port. The decoupled mode has inherently higher transfer rates than the atomic mode.

### Memory Map

The DARF64 is a two port device with 32-bit addressing and 32-bit data on each port. The 4 Gbyte memory maps are different for each port. A cycle that is generated to select the VMEbus port of the DARF64 from a VMEbus master is generated on the local bus as a 68020-like bus cycle, with the data shifted to the byte lanes appropriate for the data size indicated in the VMEbus transfer.

A cycle generated by the local CPU for the VMEbus is signalled to the DARF64 by having the local logic assert the VMEOUT (device wants bus) input. This cycle is interpreted according to the memory map of Figure 25 to generate the appropriate cycle on the DARF VMEbus port.

The DARF64 treats the 4 Gbyte space viewed from the local port as 32 – 128 Mbyte pages numbered 0 through 31, starting from address 0. Accesses to VMEbus A24:D16 space are through the lowest 16 Mbytes of page 31 (default) or page 0 as determined by register selection. The same is true of A24:D32 transfers through the second 16 Mbytes of page 31 (default) or page 0. A24 can also be disabled entirely, causing these locations to generate A32:D32 VMEbus cycles in those address ranges.

The upper 64 Kbytes of page 31 causes A16:D16 cycles to be generated, if A16 mode is enabled (default). Otherwise, this area causes A32:D32 cycles.

The BUSSEL register within the DARF64 allows each of the 32 pages to be individually forced to generate a $\overline{\text{VSBSEL}}$ signal instead of a VMEbus access. This is useful whenever a major peripheral bus, like a VME Subsystem Bus (VSB), is present. The default setting is for all pages to generate VMEbus accesses.

Aside from the areas mentioned above, accesses with $\overline{\text{VMEOUT}}$ asserted generate A32:D32 VMEbus cycles.

### VMEbus Master

The DARF64 will request the VMEbus due to an atomic access begun by the CPU (indicated by the $\overline{\text{VMEOUT}}$ signal from its address decoder), due to the Transmit FIFO having write cycles pending completion, or due to the DMAC starting transfers. DMAC operation is discussed later in this data sheet. Atomic cycles include all read cycles, read-modify-write cycles, and interrupt acknowledge cycles. Write cycles are normally decoupled through the FIFOs, but the DARF64 can be programmed to perform them atomically.

When the CPU performs an access in the A16/D16 range, the DARF64 will respond to the CPU as a 16 bit device. The CPU must resize cycles if necessary. Similarly, in the A24/D16 space the DARF64 will request the CPU to split up cycles if needed. The A24/D32 space allows 32 bit transfers, while the A32 spaces are always 32 bits wide. The implied addressing space and the CPU function codes determine the data or program, and supervisory or nonprivileged aspects of the AM code.

Prior to accepting a CPU cycle for the VMEbus the address is checked against the VMEbus/VSB routing register. If the cycle address falls within the card slave image then it will be redirected to the local memory. The VMEbus/VSB routing register can be used to declare any of the 128 megabyte pages of the VME-out space to be VSB spaces. In those cases the DARF64 will select an external VSB interface instead of using its own VMEbus logic.

### VMEbus Slave

Independent A32 and A24 VMEbus slave images can be programmed in the DARF64, each with their own base address and size. Each image supports D32 through D08 (EO) accesses, block mode accesses, and D64 accesses in multiplexed block mode.

The A24 image can be 512K, 1M, 2M, or 4 megabytes in size and based at any multiple of its size. The A32 image can vary from 4K to 128M bytes in size, based at any 128 megabyte boundary. Access protection can be set for the A32 and A24 images, by declaring a lower section

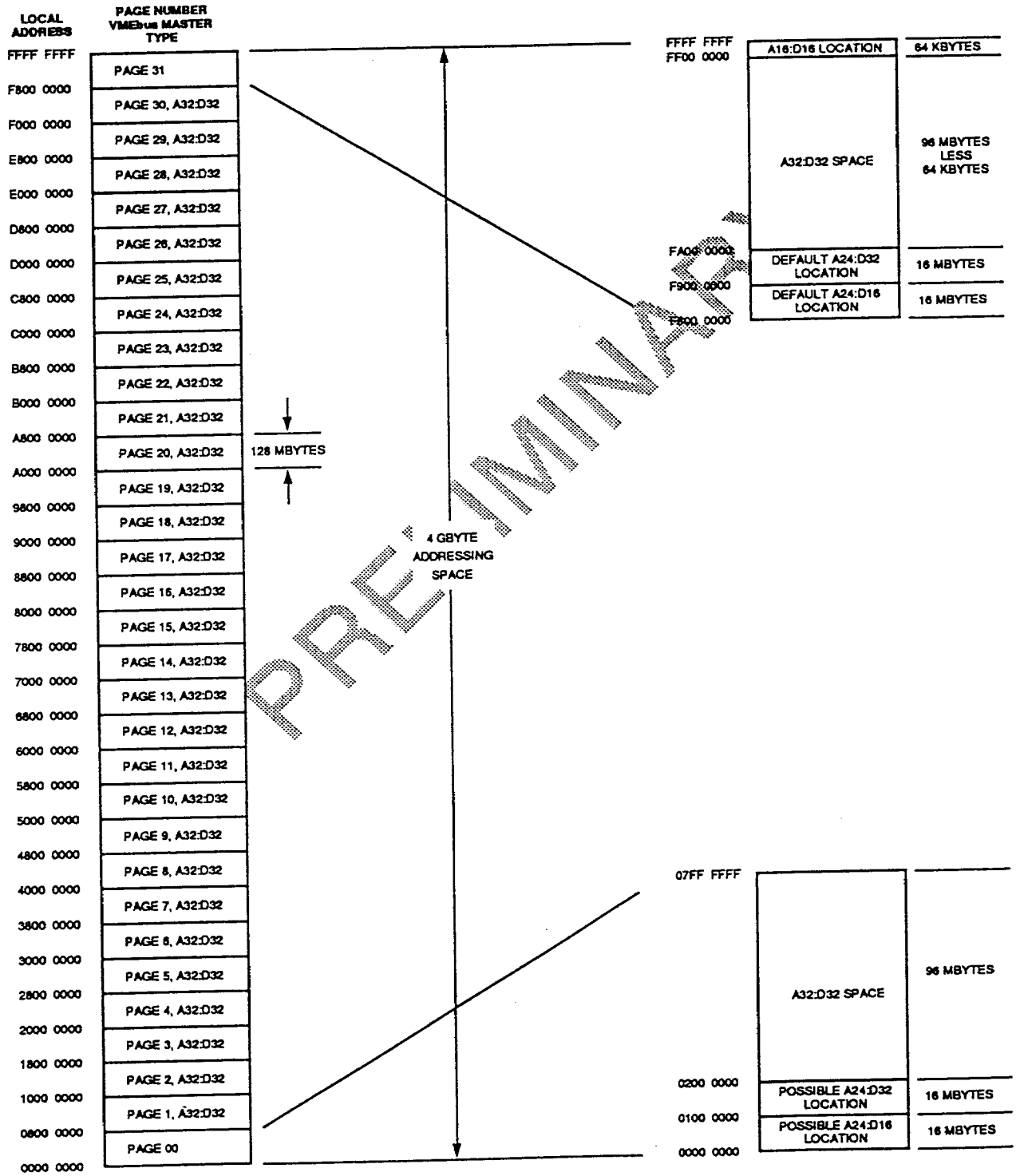





Figure 26: DARF64 MEMORY MAP

of the image to be not accessible or read-only. The protected section can vary in size from none to 128 megabytes.

An A64 image can be created at any 4 gigabyte boundary. It is 128 megabytes large, and only supports D64 multiplexed block transfers. The access protection configured for the A32 image also applies to the A64 image.

The slave images are accessible by both the VMEbus and the local CPU, so that reads or writes by a process access the same memory location independent of which card the process is running on. CPU accesses done to the card's own slave image do not consume VMEbus bandwidth.

Other slave characteristics are locking local bus ownership for the duration of VMEbus read-modify-write cycles, and optional Late Bus Error detection on the local bus during read cycles.

**DMA Controller**

The CA91C064 DMAC can perform read and write transfers between the VMEbus and local memory in several different address and data modes. It is controlled through four internal registers, for the local and VMEbus addresses, transfer length, and mode.

The DMAC can be programmed to use A64, A32, or A24 addressing, in supervisor or nonprivilege mode. Any A32 or A24 address can be programmed as the VMEbus address. In A64 mode the high 32 address bits are provided from the Master A64 Base Address Register and the Lower 32 bits are provided by the DMA VMEbus Address Register.

Data transfers can be configured to occur in discrete, block or multiplexed block (D64) mode. Discrete and block modes can be further configured as D32 or D16 widths. The DMAC can be programmed to transfer up to 4 megabytes of data. It inserts addressing phases wherever necessary on local bus and VMEbus.

In order to support the high transfer rates available in MBLT mode, the CA91C064 can be programmed to use burst mode on the local bus, with a burst length of 4, 8, 16 or 32 longwords.

In the event the CA91C064 receives a BERR while the DMAC is running, DMAC operations halt and an interrupt is sent to the CPU. The current local bus and VMEbus addresses and control information are available to the CPU via status registers.

Advanced features of the CA91C064 can be used to tune DMAC and VMEbus performance. The Transmit FIFO can be configured to begin VMEbus transfers immediately upon having data, or configured to wait until the FIFO is full. The No-Release mode bit causes the DARF64 to keep ownership of the VMEbus until either the ACC requests the DARF64 to release the bus, or until the bit is turned off. The *VMEbus Ownership Timer* in the ACC can be used in conjuction with the NOREL bit to throttle DMAC use of the VMEbus.

**Location Monitor**

Support for communication between processes is provided by the Location Monitor. It monitors the top longword address and top even word address in the A32 and A24 slave images programmed into the CA91C064. Data written to those addresses is queued in the 31 deep message FIFO. Since the slave images and Location Monitors are equally accessible by the VMEbus and the local CPU, a process does not need to know whether the process it's sending a message to is on the same card or another card.

The Location Monitor will assert an interrupt to the CPU while there are entries in the FIFO. The FIFO contents are read out through one of the CA91C064 internal registers. These entries can be used as pointers to longer data blocks in memory, or could be coded with specific meanings.

**VMEbus Interrupter**

The *Interrupter* function is implemented using both ACC and CA91C064. The ACC contains the logic to assert VMEbus interrupts and detect when they are acknowledged. The CA91C064 provides the interrupt vector and assert DTACK* when signalled to do so by the ACC.

**VMEbus Specifications**

Characteristics of the CA91C064 can be specified using standard VMEbus mnemonics, as given in Table 15.

**Table 15 : VMEbus SPECIFICATIONS**

| Characteristic | Specification | Notes |
|---|---|---|
| VMEbus master | A32,A24/D32,D16,D08 (EO);<br>A16/D16,D08(EO);<br>UAT;RMW<br><br>A32,A24/D32,D16;<br>BLT A32,A24/D64,D32,D16;<br>BLT A64/D64<br>no ADO | By CPU. D32 transfers cannot be done in the A16 space.<br><br>Unaligned cycles and read-modify-write cycles can be generated.<br>By DMAC.<br><br>Address-only cycles are not generated. |
| VMEbus slave | A32,A24/D32,D16,D08(EO)<br>BLT A32,A24/D64,D32,D16,D08(EO)<br>BLT A64/D64<br>ADO, UAT, RMW | DARF64 is not an A16 slave.<br><br>Address-only cycles ignored.<br>Unaligned cycles and read-modify-write cycles accepted. |
| Location monitor | A32,A24/D32,D16(E); | No A64 or A16 location monitor; word transfers on odd-word boundaries and byte transfers not detected; read cycles not detected. |
| Interrupt handler | IH(1-7),D08(O) | In conjunction with the ACC |
| Interrupt generator | I(1-7),D08(O),ROAK | In conjunction with the ACC |



### Decoupling

The natural mode of the CA91C064 is decoupled, in which entire write cycles (the data, address, and all relevant control signals) are immediately captured into a 15 deep queueing FIFO. One FIFO is provided for local to VMEbus writes, while another independent FIFO processes cycles received from the VMEbus. Once the write cycle is captured the originating bus is acknowledged, thereby immediately releasing it for use by another master. Whenever there are cycles pending in the FIFO, the destination end of the FIFO will request its bus and perform the cycle according to the address and control signals stored with the data. Read, read-modify-write, and interrupt acknowledge cycles are atomic, and are routed around the FIFOs. The CA91C064 can also be programmed to process write cycles in atomic mode.

When an atomic cycle occurs, the CA91C064 performs the cycle in a direct-connected mode, so that the address, data, DTACK and BERR signals are connected between the local bus and the VMEbus, and the VMEbus is in use until the local cycle ends. To preserve data integrity, atomic cycles are not performed until all write cycles queued ahead of the atomic cycle are completed.

Error recovery mechanisms are available in decoupled mode, so that if the VMEbus cycle generator receives a BERR in response to its write cycle, all information about the cycle will be stored in diagnostic registers, and an interrupt sent to the CPU. The CA91C064 will stop servicing the Transmit FIFO until the CPU has cleared the error, so that data ordering remains under control of the application.

### MBLT Transfers

The multiplexed block transfer (MBLT, or D64) mode is a newly defined capability of the VMEbus. It takes advantage of the address bus being otherwise idle during block transfer. An additional 32 bits of data is sent on the 31 address lines and the LWORD* signal so that a double longword is transferred on each data strobe – DTACK* handshake. Specific AM codes are used to identify MBLT cycles.

MBLT cycles use the same signal timing as standard block transfers, but double the bandwidth. The conversion between each D64 transfer within an MBLT block on the VMEbus and the local bus is performed by converting it to a pair of longwood local cycles, which are considered indivisible.

### Local Burst Mode

The CA91C064 provides a new burst mode on the local bus, that can be enabled and configured for 4 to 32 longword bursts in the Mode Control register. The timing is similar to that used by the 68030: the CA91C064 will begin the cycle with normal address and data strobe assertion, but will identify it as a burst by using function code 3. The memory controller can throttle the burst by using DSACK1 as the synchronous acknowledge for each transfer in the burst.

Read cycles are performed at one clock per transfer during the burst, while write cycles use two clocks each. The CA91C064 will use bursts when reading from local memory under DMAC control, and when sufficient data within a block is detected in the Receive FIFO for a write burst.

### A64 Addressing

A64 data transfers use the address and the data bus in parallel to perform a 64 bit address broadcast phase, followed by data transfer cycles. The DMAC in the CA91C064 can originate A64/D64 read or write transfers, and an A64 slave image that accepts A64/D64 blocks can also be configured.

A64 block transfers are implemented for use in distributed VMEbus or VMEbus/Futurebus+ systems, where the high 32 address bits can be used to route data blocks between appropriate subsystems. Within a subsystem, several cards can have independent A64 base addresses defining their global address.

### BI-mode

BI-mode is used to isolate a card from activity on the VMEbus. While the CA91C064 is in BI-mode, it will not respond to a CPU request for access to the VMEbus, and will not respond to any attempted VMEbus access to its slave images.

The BI-mode protocol is used to support card and system testing, parking of standby cards; and isolation of failed cards. The BIMODE input to the CA91C064 is supplied by the CA91C014 ACC, which asserts it after reset, when IRQ1* is configured as the system BI-mode line and becomes asserted, or when a local control bit is asserted.

The protocol to exit BI-mode is a write access to the CA91C064 location monitor.

### 68040 and RISC Support

The CA91C064 is also designed to work with 68040. In this mode, it will accept 68040 local bus timing and perform the data and control signal multiplexing required to interface the 68040 to the VMEbus. 68030 timing will still be used when the CA91C064 accesses local memory. When processors other than the 680x0 series are used, functions such as byte swapping logic and dynamic bus sizing can be selectively disabled if appropriate.

### 68040 Mode

The 68040 support provided by the DARF64 includes turning off dynamic bus sizing and a synchronous local bus interface that permits direct signal connection. These signals are;

1. - TS connected to AS
2. - TA to DSACK0
3. - TEA to BERR

In order to invoke this 68040 mode DS must be grounded on the local bus, this signal is sampled after the reset sequence. However, when the DARF64 becomes local bus master it generates 68030 timing.

### Test and Diagnostics

Three levels of user test support are provided in the CA91C064 : at the lowest level, a specific combination of signals asserted at the time of RESET negation will put the CA91C064 into a transparent mode. A card edge tester can then access all devices on the card's local bus, such as Flash EPROM and interrupt handlers for programming or testing.

Second level test functions allow the local CPU to test address and data paths and control logic in the CA91C064 , through use of a loopback mode, manual shifting of the Transmit and Receive FIFOs, and readback of FIFO contents.

Diagnostic functions available during system operation are a set of registers that capture the address, data, and control signals of any decoupled write cycles performed by the CA91C064 for which a Bus Error was received. The CPU is interrupted, and may read back the cycle details to retry it or determine whether the cycle was correct.

**Performance**

Performance of a VMEbus card can be defined using three standard configurations. The sustained data transfer rates the CA91C064 is targeted to achieve using MBLT mode, on a 25 MHz card with local bus burst mode, are noted below. Peak transfer rates can be higher due to FIFO activity.

1. Card under worst case conditions acting as a master with an ideal VMEbus slave.
   - 61 megabytes per second MBLT writes
   - 45 megabytes per second MBLT reads
2. Card under worst case conditions responding as a slave to an ideal master.
   - 50 megabytes per second MBLT writes
3. Write cycles between two cards under nominal conditions.
   - 50 megabytes per second

Non-multiplexed block transfer rates would be between half and two-thirds the above rates. Read cycle performance is primarily determined by the arbitration time for the VMEbus and the slave card local bus.

## DARF64 REGISTER DESCRIPTIONS

The CA91C064 contains twenty registers used to access control and status bits, DMA functions and other utilities. All registers are 32 bits wide and are only accessible as longwords, although not all bits are always used. If the value read from a register is different than the value written to, or stored in the register, then read and write values are individually described. Otherwise, no distinction is made. Bits that are not used have defined values, and may be used in future versions of the DARF64. It is recommended that such unused bits be set to zero to maximize the probability of future firmware compatibility.

Values written to read only bits have no effect. It is recommended that only zero values be written in such cases, to ensure compatibility with future versions of the DARF64 which may use these bits to provide additional features.

In the following tables:
R = Read only
U = Undefined
R/W = Read/Write



**Table 16 : DARF64 REGISTER SUMMARY**

| Offset from DARF64 Basic Address | Name | Register Function |
|---|---|---|
| 4CH | DMAVTC | DMA VMEbus transfer count register |
| 48H | LAG | Local address generator register |
| 44H | MA64BAR | Master A64 base address register |
| 40H | SA64BAR | Slave A64 base address register |
| 3CH | MODE | Mode control register |
| 38H | LMFIFO | Location monitor FIFO read port |
| 34H | TXCTL | Transmit FIFO control bits output latch |
| 30H | TXADDR | Transmit FIFO address output latch |
| 2CH | TXDATA | Transmit FIFO data output latch |
| 28H | APBR | Access protect boundary register |
| 24H | IVECT | VMEbus interrupter vector register |
| 20H | BUSSEL | VMEbus/VSB select register |
| 1CH | RXCTL | Receive FIFO control bits, for self tests |
| 18H | RXADDR | Recieve FIFO address bits, for self tests |
| 14H | RXDATA | Recieve FIFO data bits, for self tests |
| 10H | VMEBAR | VMEbus slave base address register |
| 0CH | DCSR | Control and status register |
| 08H | DMATC | DMA transfer count register |
| 04H | DMAVAR | DMA VMEbus address register |
| 00H | DMALAR | DMA local address register |

**Table 17 : DMA VMEbus TRANSFER COUNT REGISTER**

| Register Name: DMAVTC | Register Number: 4CH |
|---|---|

| Bits | Function | |
|---|---|---|
| 31 – 24 | Not Used | |
| 23 – 16 | Not Used *(4 bits)* | DMA VMEbus Transfer Count |
| 15 – 08 | DMA VMEbus Transfer Count *continued* | |
| 07 – 00 | DMA VMEbus Transfer Count *continued* | |

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| DVTC19 – 00 | R/W | U | 0 | The number of VMEbus cycles remaining to perform in the programmed DMA transfer. |



**Table 18 : LOCAL ADDRESS GENERATOR REGISTER**

| Register Name: LAG | Register Number: 48H |
|---|---|

| Bits | Function | |
|---|---|---|
| 31 – 24 | Not Used *(5 bits)* | Local Address Generator Value |
| 23 – 16 | Local Address Generator Value *continued* | |
| 15 – 08 | Local Address Generator Value *continued* | |
| 07 – 00 | Local Address Generator Value *continued* | |

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| LAG26 – 00 | R/W | U | 0 | This is the next local address to be used in block mode transfers received from the VMEbus, either as a slave or by DMAC transfers from the VMEbus to local memory. |

**Table 19 : MASTER A64 BASE ADDRESS REGISTER**

| Register Name: MA64BAR | Register Number: 44H |
|---|---|

| Bits | Function |
|---|---|
| 31 – 24 | A63 – A56 address bits for Master A64 Base Address |
| 23 – 16 | A55 – A48 address bits for Master A64 Base Address |
| 15 – 08 | A47 – A40 address bits for Master A64 Base Address |
| 07 – 00 | A39 – A32 address bits for Master A64 Base Address |

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| MA64B31 – 00 | R/W | U | 0 | A64 – A32 address bits during master A64 transfers. |



**Table 20: SLAVE A64 BASE ADDRESS REGISTER**

| Register Name: SA64BAR | Register Number: 40H |
|---|---|

| Bits | Function |
|---|---|
| 31 – 24 | A63 – A56 address bits for Slave A64 Base Address |
| 23 – 16 | A55 – A48 address bits for Slave A64 Base Address |
| 15 – 08 | A47 – A40 address bits for Slave A64 Base Address |
| 07 – 00 | A39 – A32 address bits for Slave A64 Base Address |

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| SA64B31 – 00 | R/W | U | 0 | This parameter defines the base address for slave A64 accesses. |

**Table 21 : DARF64 MODE CONTROL REGISTER**

**Register Name: MODE** **Register Offset: 3CH**

| Bits | Function | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 31 – 24 | DARFEN | Not Used | | DMABEN | RMCPIN | BUSSIZ | SWAP | 040 |
| 23 – 16 | DPRIV | NOREL | FILL | DMAA64 | MBLT | BLT | BLT32 | DMARD |
| 15 – 08 | FIFOBEN | BLEN | | RXATOM | TXATOM | A24SEVEN | DMA24 | BERRCHK |
| 07 – 00 | TASCON | A24P0 | LPBK | DISRX | A24DI | A16DI | PROT | VINEN |

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| DARFEN | R/W | 0 | | Enables DARF64 functions that operate differently in DARF32 |
| | | | 0 | Disabled |
| | | | 1 | Enabled |
| DMABEN | R/W | 0 | | DMA local bus burst enable |
| | | | 0 | Burst mode disabled for DMA |
| | | | 1 | Burst mode enabled for DMA |
| RMCPIN | R/W | 0 | | RMC pin configuration |
| | | | 0 | CPU RMC signal is configured as an output |
| | | | 1 | VMEbus RETRY signal is configured as an input |
| BUSSIZ | R/W | 0 | | Dynamic bus sizing request enable |
| | | | 1 | Enable sizing requests to CPU, implement D16 spaces |
| | | | 0 | Disable sizing requests to CPU, set VMEbus to all D32 |
| SWAP | R/W | 1 | | Word swap enable |
| | | | 0 | Disable word swapping |
| | | | 1 | Enable word swapping |
| 040 | R | 0 | | 68040 mode |
| | | | 0 | DARF64 is not in 68040 mode |
| | | | 1 | DARF64 is in 68040 mode |
| DPRIV | R/W | 1 | | DMAC privilege type for VMEbus cycles |
| | | | 0 | DMAC uses non-privileged AM codes |
| | | | 1 | DMAC uses supervisory AM codes |
| NOREL | R/W | 0 | | VMEbus no-release mode |
| | | | 0 | DARF64 will release VMERQ when done |
| | | | 1 | DARF64 will keep VMERQ asserted until VMEGR is negated or until this bit is cleared |

**Table 21: DARF64 MODE CONTROL REGISTER CON'T**

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| FILL | R/W | 0 | | Transmit FIFO fill mode |
| | | | 0 | Request VMEbus when any entries are in the FIFO |
| | | | 1 | If DMA is running, wait for FIFO full before requesting VMEbus. If DMA is not running, same as FILL=0 |
| DMAA64 | R/W | 0 | | A64 mode control for the DMA |
| | | | 0 | DMA uses DMA24 bit to set A24 or A32 mode |
| | | | 1 | DMA uses A64 mode and Master A64 Base Addr Reg |
| MBLT | R/W | 0 | | Multiplexed block transfer mode DMAC control |
| | | | 0 | DMAC does not use MBLT mode |
| | | | 1 | DMAC uses MBLT mode |
| BLT | R/W | 0 | | Non-multiplexed block transfer mode control for DMAC |
| | | | 0 | DMAC does not use BLT mode |
| | | | 1 | DMAC uses BLT mode |
| BLT32 | R/W | 1 | | Data size for DMAC in non-block and BLT block modes |
| | | | 0 | DMAC uses D16 transfers |
| | | | 1 | DMAC uses D32 transfers |
| DMARD | R/W | 0 | | DMAC read or write mode |
| | | | 0 | DMAC transfers from local memory to VMEbus |
| | | | 1 | DMAC transfers from VMEbus into local memory |
| FIFOBEN | R/W | 1 | | Receive FIFO burst enable |
| | | | 0 | Disable burst mode for receive FIFO |
| | | | 1 | Enable burst mode for receive FIFO |
| BLEN 14–13 | R/W | 0 | | Local bus maximum burst length |
| | | | 0 | 4 longwords |
| | | | 1 | 8 longwords |
| | | | 2 | 16 longwords |
| | | | 3 | 32 longwords |
| RXATOM | R/W | 0 | | Receive FIFO Atomic/Decoupled |
| | | | 0 | RX FIFOs used in decoupled mode |
| | | | 1 | RX FIFOs bypassed (Atomic mode) |
| TXATOM | R/W | 0 | | Transmit FIFO Atomic/Decoupled |
| | | | 0 | TX FIFOs used in decoupled mode |
| | | | 1 | TX FIFOs bypassed (Atomic mode) |
| A24SLVEN | R/W | 0 | | A24 slave image enable |
| | | | 0 | Image will not respond |
| | | | 1 | Image is enabled |

**Table 21 : DARF64 MODE CONTROL REGISTER CON'T**

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| DMA24 | R/W | 0 | | DMA destination address size |
| | | | 0 | DMA operates as A32 master |
| | | | 1 | DMA operates as A24 master |
| BERRCHK | R/W | 0 | | Local late bus error enable |
| | | | 0 | No extra delay inserted |
| | | | 1 | 1 clock local delay inserted to check for late BERR from RAM |
| TASCON | R/W | 0 | | AS* modifier for RMW cycles |
| | | | 0 | AS* negated between every VMEbus cycle |
| | | | 1 | AS* not negated between cycles while CPU RMC is asserted |
| A24P0 | R/W | 0 | | VMEbus A24 space address |
| | | | 0 | A24 space located at F800.0000 |
| | | | 1 | A24 space located at 0000.0000 |
| LPBK | R/W | 0 | | Loopback enable bit |
| | | | 0 | No loopback |
| | | | 1 | Loopback through FIFOs enabled |
| DISRX | R/W | 0 | | Receive FIFO disable bit |
| | | | 0 | Normal operation |
| | | | 1 | FIFO emptied by RXSHFT control bit only |
| A24DI | R/W | 0 | | Page 0 VMEbus A24 disable bit |
| | | | 0 | A24 responds per A24P0 bit |
| | | | 1 | A24 disabled if in page 0 |
| A16DI | R/W | 0 | | VMEbus A16 disable bit |
| | | | 0 | VMEbus A16 located at FFFF.0000 |
| | | | 1 | A16 space disabled |
| PROT | R/W | 0 | | Access protection type |
| | | | 0 | Write protection only |
| | | | 1 | Read and write protection |
| VINEN | R/W | 0 | | Slave images enabling |
| | | | R 0 | All slave images are disabled |
| | | | R 1 | All programmed images enabled |
| | | | W 0 | Disable all slave images |
| | | | W 1 | Enable all programmed images |

**Table 22 : LOCATION MONITOR FIFO READ PORT**

| Register Name: LMFIFO | Register Number: 38H |
|---|---|

| Bits | Function |
|---|---|
| 31 – 24 | LM (Location Monitor FIFO Output Stage Data) – Byte 3 |
| 23 – 16 | LM (Location Monitor FIFO Output Stage Data) – Byte 2 |
| 15 – 08 | LM (Location Monitor FIFO Output Stage Data) – Byte 1 |
| 07 – 00 | LM (Location Monitor FIFO Output Stage Data) – Byte 0 |

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| LM 31 – 00 | R | U | | Data at output stage of Location Monitor FIFO |

**Table 23 : TRANSMIT FIFO AM CODE and CONTROL BIT LATCH**

| Register Name: TXCTL | Register Number: 34H |
|---|---|

| Bits | Function | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 31 – 24 | Not Used | | | | | | | |
| 23 – 16 | Not Used | | | | | | | |
| 15 – 08 | Not Used | | | | | | | |
| 07 – 00 | TCTL 7 | TCTL 6 | TCTL 5 | TCTL 4 | TCTL 3 | TCTL 2 | TCTL 1 | TCTL 0 |

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| TCTL 7 | R | U | | MBLT transfer type flag |
| | | | 0 | This transfer is *not* part of an MBLT block |
| | | | 1 | This transfer is part of an MBLT block |
| TCTL 6 | R | U | | BLT transfer type flag |
| | | | 0 | This transfer is *not* part of a BLT block |
| | | | 1 | This transfer is part of a BLT block |
| TCTL 5, 4 | R | U | | Transfer size |
| | | | 0, 0 | Longword |
| | | | 0, 1 | Byte |
| | | | 1, 0 | Word |
| | | | 1, 1 | Tri-byte |
| TCTL 3, 2 | R | U | | Address space |
| | | | 0, 0 | A32 |
| | | | 0, 1 | Reserved |
| | | | 1, 0 | A16 |
| | | | 1, 1 | A24 |
| TCTL 1 | R | U | | Privilege level of transfer |
| | | | 0 | User |
| | | | 1 | Supervisor |
| TCTL 0 | R | U | | Data type: CPU Transfer / DMA Transfer |
| | | | 0 | Program / MBLT |
| | | | 1 | Data / BLT or non-block |

**Table 24 : TRANSMIT FIFO ADDRESS OUTPUT LATCH**

| Register Name: TXADDR | Register Number: 30H |
|---|---|

| Bits | Function |
|---|---|
| 31 – 24 | Transmit FIFO Address Lane Output Stage – Byte 3 |
| 23 – 16 | Transmit FIFO Address Lane Output Stage – Byte 2 |
| 15 – 08 | Transmit FIFO Address Lane Output Stage – Byte 1 |
| 07 – 00 | Transmit FIFO Address Lane Output Stage – Byte 0 |

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| TADDR 31 – 00 | R | U | | Address at transmit FIFO stage for discrete or non-block DMA transfers. D63 – D32 data during multiplexed block transfers. |



**Table 25 : TRANSMIT FIFO DATA OUTPUT LATCH**

| Register Name: TXDATA | Register Number: 2CH |
|---|---|

| Bits | Function |
|---|---|
| 31 – 24 | Transmit FIFO Data Lane Output Stage – Byte 3 |
| 23 – 16 | Transmit FIFO Data Lane Output Stage – Byte 2 |
| 15 – 08 | Transmit FIFO Data Lane Output Stage – Byte 1 |
| 07 – 00 | Transmit FIFO Data Lane Output Stage – Byte 0 |

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| TDATA 31 – 00 | R | U | | Data at transmit FIFO data lane output stage. During D64 cycles this will be D31 – D00. |

**Table 26 : ACCESS PROTECT BOUNDARY REGISTER**

| Register Name: APBR | | | | | Register Number: 28H |
|---|---|---|---|---|---|
| **Bits** | **Function** | | | | |
| 31 – 24 | Not Used | | | | |
| 23 – 16 | Not Used | | | | |
| 15 – 08 | Not Used | | | | |
| 07 – 00 | Not Used *(4 bits)* | APB03 | APB02 | APB01 | APB00 |

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| APB03 – 00 | R/W | 0 | | Access protection boundary; protection enforced below this boundary on slave VMEbus image |
| | | | 0 | No protection |
| | | | 1 | Lower 64 KB |
| | | | 2 | Lower 128 KB |
| | | | 3 | Lower 256 KB |
| | | | 4 | Lower 512 KB |
| | | | 5 | Lower 1 MB |
| | | | 6 | Lower 2 MB |
| | | | 7 | Lower 4 MB |
| | | | 8 | Lower 8 MB |
| | | | 9 | Lower 16 MB |
| | | | A | Lower 32 MB |
| | | | B | Lower 64 MB |
| | | | C | Lower 128 MB |
| | | | D | Lower 128 MB |
| | | | E | Lower 128 MB |
| | | | F | Lower 128 MB |

**Table 27 : VMEbus INTERRUPTER VECTOR REGISTER**

| Register Name: IVECT | Register Number: 24H |
|---|---|

| Bits | Function |
|---|---|
| 31 – 24 | Not Used |
| 23 – 16 | Not Used |
| 15 – 08 | Not Used |
| 07 – 00 | IVECT (Interrupt Vector) |

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| IVECT 07 – 00 | R/W | U | | VMEbus interrupt vector bits |

**Table 28 : VMEbus/VSB BUS SELECT REGISTER**

| Register Name: BUSSEL | Register Number: 20H |
|---|---|

| Bits | Function |
|---|---|
| 31 – 24 | VSBEN (VMEbus/VSB Data Transfer Cycle Routing Bits) – Byte 3 |
| 23 – 16 | VSBEN (VMEbus/VSB Data Transfer Cycle Routing Bits) – Byte 2 |
| 15 – 08 | VSBEN (VMEbus/VSB Data Transfer Cycle Routing Bits) – Byte 1 |
| 07 – 00 | VSBEN (VMEbus/VSB Data Transfer Cycle Routing Bits) – Byte 0 |

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| VSBEN31 – 00 | R/W | 0 | | VMEbus/VSB select bits, one for each of the 32 by 128 Mbyte pages (refer to Address Range Map below) |
| | | | 0 | VMEbus selected |
| | | | 1 | VSB selected |

| Bit | Address Range Mapped | Bit | Address Range Mapped |
|---|---|---|---|
| 0 | 0000.0000 – 07FF.FFFF | 16 | 8000.0000 – 87FF.FFFF |
| 1 | 0800.0000 – 0FFF.FFFF | 17 | 8800.0000 – 8FFF.FFFF |
| 2 | 1000.0000 – 17FF.FFFF | 18 | 9000.0000 – 97FF.FFFF |
| 3 | 1800.0000 – 1FFF.FFFF | 19 | 9800.0000 – 9FFF.FFFF |
| 4 | 2000.0000 – 27FF.FFFF | 20 | A000.0000 – A7FF.FFFF |
| 5 | 2800.0000 – 2FFF.FFFF | 21 | A800.0000 – AFFF.FFFF |
| 6 | 3000.0000 – 37FF.FFFF | 22 | B000.0000 – B7FF.FFFF |
| 7 | 3800.0000 – 3FFF.FFFF | 23 | B800.0000 – BFFF.FFFF |
| 8 | 4000.0000 – 47FF.FFFF | 24 | C000.0000 – C7FF.FFFF |
| 9 | 4800.0000 – 4FFF.FFFF | 25 | C800.0000 – CFFF.FFFF |
| 10 | 5000.0000 – 57FF.FFFF | 26 | D000.0000 – D7FF.FFFF |
| 11 | 5800.0000 – 5FFF.FFFF | 27 | D800.0000 – DFFF.FFFF |
| 12 | 6000.0000 – 67FF.FFFF | 28 | E000.0000 – E7FF.FFFF |
| 13 | 6800.0000 – 6FFF.FFFF | 29 | E800.0000 – EFFF.FFFF |
| 14 | 7000.0000 – 77FF.FFFF | 30 | F000.0000 – F7FF.FFFF |
| 15 | 7800.0000 – 7FFF.FFFF | 31 | F800.0000 – FFFF.FFFF |

**Table 29 : RECEIVE FIFO CONTROL REGISTER**

**Register Name: RXCTL** **Register Number: 1CH**

| Bits | Function | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 31 – 24 | Not Used | | | | | | | |
| 23 – 16 | Not Used | | | | | | | |
| 15 – 08 | Not Used | | | | | | | RCTL 8 |
| 07 – 00 | RCTL 7 | RCTL 6 | RCTL 5 | RCTL 4 | RCTL 3 | RCTL 2 | RCTL 1 | RCTL 0 |

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| RCTL 8 | R | U | | Flags the start of a block in the FIFO |
| | | | 0 | This cycle is *not* the start of a block |
| | | | 1 | This cycle is the start of a block |
| RCTL 7 | R | U | | Identifies the entry as being part of an MBLT block |
| | | | 0 | This cycle is *not* part of an MBLT block |
| | | | 1 | This cycle is part of an MBLT block |
| RCTL 6 | R | U | | Identifies the entry as being part of a BLT block |
| | | | 0 | This cycle is *not* part of a BLT block |
| | | | 1 | This cycle is part of a BLT block |
| RCTL 5, 4 | R | U | | Address bits 1, 0 for this transfer |
| | | | X, X | A01, A00 |
| RCTL 3, 2 | R | U | | Data size |
| | | | 0, 0 | Longword |
| | | | 0, 1 | Byte |
| | | | 1, 0 | Word |
| | | | 1, 1 | Tri-byte |
| RCTL 1, 0 | R | U | | Receive FIFO TC1, 0 output bits |
| | | | 0, 0 | User program space |
| | | | 0, 1 | User data space |
| | | | 1, 0 | Supervisor program space |
| | | | 1, 1 | Supervisor data space |

**Table 30 : RECEIVE FIFO ADDRESS REGISTER**

| Register Name: RXADDR | Register Number: 18H |
|---|---|

| Bits | Function |
|---|---|
| 31 – 24 | Receive FIFO Address Lane Output Stage – Byte 3 |
| 23 – 16 | Receive FIFO Address Lane Output Stage – Byte 2 |
| 15 – 08 | Receive FIFO Address Lane Output Stage – Byte 1 |
| 07 – 00 | Receive FIFO Address Lane Output Stage – Byte 0 |

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| RADDR 31 – 00 | R | U | | Receive FIFO output address, except during multiplexed block data transfers in which case D63 – D32 are provided here.<br>Upper address bits are zeroed according to the size of slave image programmed that accepted the transfer. No zeroing effect on data received during MBLT transfers. |



**Table 31 : RECEIVE FIFO DATA REGISTER**

| Register Name: RXDATA | Register Number: 14H |
|---|---|

| Bits | Function |
|---|---|
| 31 – 24 | Receive FIFO Data Lane Output Stage – Byte 3 |
| 23 – 16 | Receive FIFO Data Lane Output Stage – Byte 2 |
| 15 – 08 | Receive FIFO Data Lane Output Stage – Byte 1 |
| 07 – 00 | Receive FIFO Data Lane Output Stage – Byte 0 |

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| RDATA 31 – 00 | R | U | | Receive FIFO output data |

**Table 32 : VMEbus BASE ADDRESS REGISTER**

| Register Name: VMEBAR | Register Number: 10H |
|---|---|

| Bits | Function | | | |
|---|---|---|---|---|
| 31 – 24 | Not Used | | | |
| 23 – 16 | Not Used | A24SIZ *(2 bits)* | A24BA *(5 bits)* | |
| 15 – 08 | Not Used *(7 bits)* | | | A32SIZ |
| 07 – 00 | A32SIZ *continued (4 bits)* | | A32BA *(5 bits)* | |

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| A24SIZ | R/W | U | | Sets size of A24 slave image |
| | | | 0 | 512K |
| | | | 1 | 1M |
| | | | 2 | 2M |
| | | | 3 | 4M |
| A24BA | R/W | U | | Sets base address of A24 slave image. Programmed size of the image will force bits 17 & 16 to zero as appropriate. Bits 20 – 16 will be compared against VMEbus address bits A23 – A19. |
| A32SIZ | R/W | U | | Sets size of A32 slave image |
| | | | 0 | 4K |
| | | | 1 | 8K |
| | | | 2 | 16K |
| | | | 3 | 32K |
| | | | 4 | 64K |
| | | | 5 | 128K |
| | | | 6 | 256K |
| | | | 7 | 512K |
| | | | 8 | 1M |
| | | | 9 | 2M |
| | | | A | 4M |
| | | | B | 8M |
| | | | C | 16M |
| | | | D | 32M |
| | | | E | 64M |
| | | | F | 128M |

**Table 32 : VMEbus BASE ADDRESS REGISTER CON'T**

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| A32BA | R/W | U | | Sets base address of A32 image |
| | | | 0 | 0000.0000 |
| | | | 1 | 0800.0000 |
| | | | 2 | 1000.0000 |
| | | | 3 | 1800.0000 |
| | | | 4 | 2000.0000 |
| | | | 5 | 2800.0000 |
| | | | 6 | 3000.0000 |
| | | | 7 | 3800.0000 |
| | | | 8 | 4000.0000 |
| | | | 9 | 4800.0000 |
| | | | A | 5000.0000 |
| | | | B | 5800.0000 |
| | | | C | 6000.0000 |
| | | | D | 6800.0000 |
| | | | E | 7000.0000 |
| | | | F | 7800.0000 |
| | | | 10 | 8000.0000 |
| | | | 11 | 8800.0000 |
| | | | 12 | 9000.0000 |
| | | | 13 | 9800.0000 |
| | | | 14 | A000.0000 |
| | | | 15 | A800.0000 |
| | | | 16 | B000.0000 |
| | | | 17 | B800.0000 |
| | | | 18 | C000.0000 |
| | | | 19 | C800.0000 |
| | | | 1A | D000.0000 |
| | | | 1B | D800.0000 |
| | | | 1C | E000.0000 |
| | | | 1D | E800.0000 |
| | | | 1E | F000.0000 |
| | | | 1F | F800.0000 |

**Table 33 : CONTROL and STATUS REGISTER**

**Register Name: DCSR** **Register Number: 0CH**

| Bits | Function | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 31 – 24 | Not Used | | | | DEVICE | | | |
| 23 – 16 | Not Used | | | | | | | CERR |
| 15 – 08 | TXSHT | RETRY | RMCERR | A64BARDY | BARDY | RXSHFT | RXRST | TXRST |
| 07 – 00 | RXHD | TXHD | DLBER | LMHD | LBERR | VBERR | DONE | DMAGO |

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| DEVICE 3 – 0 | R | 1 | 0000<br>0001 | These bits indicate the device type<br>DARF32<br>DARF64 |
| CERR | R/W | U | 0<br>1 | Configuration error: asserts $\overline{\text{VMEINT}}$ while 1. Clear by writing 0 to this bit.<br>No conflicting configurations set<br>Incompatible options are set |
| TXSHFT | R/W | 0 | R<br>W 0<br>W 1 | Transmit FIFO shift<br>Clears self; always reads zero<br>No effect<br>Tx FIFO shifts one forward |
| RETRY | R/W | 0 | 0<br>1 | State of VMEbus RETRY* signal during last failed cycle<br>Not asserted<br>Asserted |
| RMCERR | R/W | 0 | 0<br>1 | RMC cycle lockup flag<br>Last $\overline{\text{BERR}}$ was *not* issued due to RMW lockup<br>Last $\overline{\text{BERR}}$ was issued due to RMW lockup |
| A64BARDY | R | 0 | 0<br>1 | A64 base address ready flag<br>MA64BAR and SA64BAR registers not programmed yet<br>Master and slave A64 base addresses are programmed |
| BARDY | R | 0 | 0<br>1 | VMEbus base address ready<br>BAR not programmed yet<br>BAR ready |
| RXSHFT | R/W | 0 | R<br>W 0<br>W 1 | Receive FIFO shift<br>Clears self; always reads zero<br>No effect<br>Rx FIFO shifts one forward |

**Table 33 : CONTROL and STATUS REGISTER CON'T**

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| RXRST | R/W | 0 | | Receive FIFO reset |
| | | | R | Clears self; always reads zero |
| | | | W 0 | No effect |
| | | | W 1 | Resets entire receive FIFO |
| TXRST | R/W | 0 | | Transmit FIFO reset |
| | | | R | Clears self; always reads zero |
| | | | W 0 | No effect |
| | | | W 1 | Resets entire transmit FIFO and any VME-out cycle in progress |
| RXHD | R | 0 | | Receive FIFO status |
| | | | 0 | Receive FIFO is empty |
| | | | 1 | Receive FIFO has entries |
| TXHD | R | 0 | | Transmit FIFO status |
| | | | 0 | Transmit FIFO is empty |
| | | | 1 | Transmit FIFO has entries |
| DLBER | R/W | 0 | | DMA Local Bus Error indicator; asserts $\overline{\text{VMEINT}}$ pin while 1 |
| | | | R 0 | No error indicated |
| | | | R 1 | DMA received a local bus error |
| | | | W 0 | Clears DLBER indicator |
| | | | W 1 | No effect |
| LMHD | R | 0 | | Location Monitor FIFO status; asserts $\overline{\text{LMINT}}$ pin while 1 |
| | | | 0 | LM FIFO is empty |
| | | | 1 | LM FIFO has entries |
| LBERR | R/W | 0 | | Local $\overline{\text{KBERR}}$ received while in decoupled mode; asserts $\overline{\text{VMEINT}}$ pin while 1 |
| | | | R 0 | No error indicated |
| | | | R 1 | Local bus error received |
| | | | W 0 | Clears LBERR indicator |
| | | | W 1 | No effect. |
| VBERR | R/W | 0 | | VMEbus BERR* received while in decoupled mode; freezes TxFIFO and asserts $\overline{\text{VMEINT}}$ pin while 1 |
| | | | R 0 | No error indicated |
| | | | R 1 | VMEbus BERR* received |
| | | | W 0 | Clears VBERR indicator |
| | | | W 1 | No effect. |

**Table 33 : CONTROL and STATUS REGISTER CONT**

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| DONE | R/W | 0 | | DMA Done indicator; asserts $\overline{\text{VMEINT}}$ pin while 1 |
| | | | R 0 | DMA not done yet |
| | | | R 1 | DMA finished or stopped by CPU; not set if stopped due to BERR* |
| | | | W 0 | Clear DONE bit |
| | | | W 1 | No effect |
| DMAGO | R/W | 0 | | DMA Go bit |
| | | | R 0 | DMA is stopped, by self or CPU |
| | | | R 1 | DMA is running |
| | | | W 0 | DMA stop request |
| | | | W 1 | Starts DMA |

**Table 34 : DMA TRANSFER COUNT REGISTER**

| Register Name: DMATC | Register Number: 08H |
|---|---|

| Bits | Function |
|---|---|
| 31 – 24 | Not Used |
| 23 – 16 | Not Used *(4 bits)* / DTC (DMA Transfer Count) |
| 15 – 08 | DTC (DMA Transfer Count) *continued* |
| 07 – 00 | DTC (DMA Transfer Count) *continued* (20 bits) |

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| DTC19 – 00 (Note 1) | R/W | U | | DMA transfer count: specifies the number of VMEbus transfers to perform, as summarized below. |

| DMA Mode | Register Value |
|---|---|
| Non-block, D16 | Words |
| Non-block, D32 | Longwords |
| BLT, D16 | Words |
| BLT, D32 | Longwords |
| MBLT | Longwords: bit 0 is read-only value 0, since MBLT VMEbus transfers are double longwords. |

Note 1 : DTC19-12 are only used when the DARFEN (Bit 31 in DARF64 Mode Control Register) is set.

**Table 35 : DMA VMEbus ADDRESS REGISTER**

| Register Name: DMAVAR | Register Number: 04H |
|---|---|

| Bits | Function | |
|---|---|---|
| 31 – 24 | DVA (DMA VMEbus Address) – Byte 3 | |
| 23 – 16 | DVA (DMA VMEbus Address) – Byte 2 | |
| 15 – 08 | DVA (DMA VMEbus Address) – Byte 1 | |
| 07 – 00 | DVA (DMA VMEbus Address) – Byte 0 | 0 |

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| DVA 31 – 01 | R/W | U | | DMA VMEbus address bits 31 – 01 |
| DVA 00 | R | 0 | 0 | DMA VMEbus address bit 00 is always 0 |



**Table 36 : DMA LOCAL ADDRESS REGISTER**

| Register Name: DMALAR | Register Number: 00H |
|---|---|

| Bits | Function | |
|---|---|---|
| 31 – 24 | Not Used *(5 bits)* | DLA (DMA Local Address) |
| 23 – 16 | DLA (DMA Local Address) – Byte 2 | |
| 15 – 08 | DLA (DMA Local Address) – Byte 1 | |
| 07 – 00 | DLA (DMA Local Address) – Byte 0 | 0 |

| Name | Type | Condition after Reset | State | Function |
|---|---|---|---|---|
| DLA 26 – 01 | R/W | U | | DMA local address bits 26 to 01 |
| DLA 00 | R | 0 | 0 | DMA local address bit 00 is always 0 |

## ADDRESS MODIFIER CODES

### Table 37 : MASTER ACCESS AM CODES

| Local Bus Function Type | KFC2-0 Code | Address Space | VME AM Code | VMEbus Address Modifier Function |
|---|---|---|---|---|
| User data | 1 | A16 | 29 | Short non-priviledged data access |
| User Program | 2 | A16 | 2A | Short non-priviledged program access |
| Supervisor Data | 5 | A16 | 2D | Short supervisory data access |
| Supervisor Program | 6 | A16 | 2E | Short supervisory program access |
| User Data | 1 | A24 | 39 | Standard non-priviledged data access |
| User Program | 2 | A24 | 3A | Standard non-priviledged program access |
| Block Transfer | 3 | A24 | 38 | Standard non-priviledged 64-bit block transfer |
| Block Transfer | 3 | A24 | 3B | Standard non-priviledged block transfer |
| Block Transfer | 3 | A24 | 3C | Standard supervisory 64-bit block transfer |
| Block Transfer | 3 | A24 | 3F | Standard supervisory block transfer |
| Supervisor Data | 5 | A24 | 3D | Standard supervisory data access |
| Supervisor Program | 6 | A24 | 3E | Standard supervisory program access |
| User data | 1 | A32 | 09 | Extended non-priviledged data access |
| User program | 2 | A32 | 0A | Extended non-priviledged program access |
| Block Transfer | 3 | A32 | 08 | Extended non-priviledged 64-bit block transfer |
| Block Transfer | 3 | A32 | 0B | Extended non-priviledged block transfer |
| Block Transfer | 3 | A32 | 0C | Extended supervisory 64-bit block transfer |
| Block Transfer | 3 | A32 | 0F | Extended supervisory block transfer |
| Supervisor Data | 5 | A32 | 0D | Extended supervisory data access |
| Supervisor Program | 6 | A32 | 0E | Extended supervisory program access |
| Block Transfer | 3 | A64 | 00 | Long non-priviledged 64-bit block transfer |
| Block Transfer | 3 | A64 | 04 | Long supervisory 64-bit block transfer |
| CPU Space | 7 | A16 | 2E | A16 mode enabled |
| | | A16 | 0E | A16 mode disabled |



### Table 38 : SLAVE ACCESS AM CODES

| Local Bus Function Type | KFC2-0 Code | Address Space | VME AM Code | VMEbus Address Modifier Function |
|---|---|---|---|---|
| User data | 1 | A24 | 39 | Standard non-priviledged data access |
| User Program | 2 | A24 | 3A | Standard non-priviledged program access |
| Block Transfer | 3 | A24 | 38 | Standard non-priviledged 64-bit block transfer |
| Block Transfer | 3 | A24 | 3B | Standard non-priviledged block transfer |
| Block Transfer | 3 | A24 | 3C | Standard supervisory 64-bit block transfer |
| Block Transfer | 3 | A24 | 3F | Standard supervisory block transfe |
| Supervisor Data | 5 | A24 | 3D | Standard supervisory data access |
| Supervisor Program | 6 | A24 | 3E | Standard supervisory program access |
| User data | 1 | A32 | 09 | Extended non-priviledged data access |
| User Program | 2 | A32 | 0A | Extended non-priviledged program access |
| Block Transfer | 3 | A32 | 08 | Extended non-priviledged 64-bit block transfer |
| Block Transfer | 3 | A32 | 0B | Extended non-priviledged block transfer |
| Block Transfer | 3 | A32 | 0C | Extended supervisory 64-bit block transfer |
| Block Transfer | 3 | A32 | 0F | Extended supervisory block transfer |
| Supervisor Data | 5 | A32 | 0D | Extended supervisory data access |
| Supervisor Program | 6 | A32 | 0E | Extended supervisory program access |
| Block Transfer | 3 | A64 | 00 | Long non-priviledged 64-bit block transfer |
| Block Transfer | 3 | A64 | 04 | Long supervisory 64-bit block transfer |

## DARF64 CONNECTIONS to VMEbus, LOCAL BUS and CA91C014 ACC

### Table 39 : DARF64 to VMEbus CONNECTIONS

The DARF64 VMEbus signals connect via buffers to the VMEbus. These signals correspond to (or are derived from) the VMEbus signals shown below.

| DARF64 | VMEbus |
|---|---|
| VADDR 31 – 01 | A 31 – 01 |
| VAM 5 – 0 | AM 5 – 0 |
| $\overline{\text{VAS}}$ | AS* |
| $\overline{\text{VASDLY}}$ | AS* |
| $\overline{\text{VBERRI}}$ | BERR* |
| $\overline{\text{VBERRO}}$ | BERR* |
| VDATA 31 – 00 | D 31 – 00 |
| $\overline{\text{VDS0}}$ | DS0* |
| $\overline{\text{VDS1}}$ | DS1* |
| $\overline{\text{VDSDLY}}$ | DS0* or DS1* |
| $\overline{\text{VDTACKI}}$ | DTACK* |
| $\overline{\text{VDTACKO}}$ | DTACK* |
| $\overline{\text{VDTKDLY}}$ | DTACK* |
| $\overline{\text{VIACK}}$ | IACK* |
| $\overline{\text{VLWORD}}$ | LWORD* |
| $\overline{\text{VRMC}}$ | RMC* |
| $\overline{\text{VWR}}$ | WRITE* |

### Table 40 : DARF64 to LOCAL BUS CONNECTIONS

The DARF64 local bus signals connect in parallel with the same signals on the local CPU, usually a 68020 or 68030.

| | |
|---|---|
| KADDR 31 – 00 | $\overline{\text{KDSACK1}}$ |
| $\overline{\text{KAS}}$ | KFC 2-0 |
| $\overline{\text{KBERR}}$ | $\overline{\text{KHALT}}$ |
| KCLK | $\overline{\text{KRMC}}$ |
| KDATA 31 – 00 | KSIZE 1 – 0 |
| $\overline{\text{KDS}}$ | $\overline{\text{KWR}}$ |
| $\overline{\text{KDSACK0}}$ | |

### Table 41 : DARF64 to ACC CONNECTIONS

| ACC | PGA | DARF64 | PGA |
|---|---|---|---|
| BIMODE | B7 | BIMODE | P6 |
| $\overline{\text{BIREL}}$ | Q11 | $\overline{\text{BIREL}}$ | S17 |
| $\overline{\text{LBGR0}}$ | Q7 | $\overline{\text{LBGR}}$ | M15 |
| $\overline{\text{LBRQ0}}$ | N10 | $\overline{\text{LBRQ}}$ | R14 |
| $\overline{\text{VECTEN}}$ | P8 | $\overline{\text{VECTEN}}$ | P13 |
| $\overline{\text{VIACK}}$ | Q8 | $\overline{\text{VIACKRQ}}$ | N15 |
| $\overline{\text{VMEGR}}$ | N8 | $\overline{\text{VMEGR}}$ | L15 |
| $\overline{\text{VMERQ}}$ | P11 | $\overline{\text{VMERQ}}$ | M17 |

Note: In addition to the above signals, the DARF64 may also connect to any two of the ACC local autovectored interrupt inputs, except for $\overline{\text{L7INMI}}$ and $\overline{\text{L7IMEM}}$. The DARF64 uses the two interrupts to signal location monitor accesses and general DARF64 service requests.

## APPLICATION NOTES

### System Configuration

In order to force the CPU to retry a VME-out cycle, the DARF must have already requested the VMEbus from the ACC. The DARF waits for the VMEbus grant, then immediately negates its request without using it so that spurious bus requests do not disrupt VMEbus operation. The DARF is then ready for a new VME-out cycle.

However, if the ACC is programmed into FAIR and ROR mode, and some other card is using the bus on the same bus request level, the CPU and DARF may thrash, forever requesting and throwing away the bus grant. Avoid this configuration by using either different request levels, or by not using both FAIR and ROR modes.

### DARF64 Initialization

Until the local CPU needs to use either the VMEbus or it's slave image of memory, the DARF does not need to be programmed. Before the DARF will perform a VMEbus cycle for the CPU, its BIMODE BI-mode signal must be deasserted. On cards using the ACC and DARF, this is accomplished by creating a VMEbus slave image using the VMEBAR register, then writing to the location monitor that exists at the top of that slave image. The DARF will assert $\overline{\text{BIREL}}$ to the ACC, which will then negate BIMODE if all other BI-mode initiator signals are negated.

For VMEbus to access dual ported memory on the card, the VMEBAR and APBR registers must be programmed, to create the slave image and initialize the access protection. The DARF must also be out of BI-mode.

The DARF defaults to decoupled mode. If the DARF receives a VMEbus BERR*, software on the card must clear the VBERR flag in the Control and Status register before further VMEbus master accesses are possible.

### CA91C015 DARF32 Compatibility

The pin assignment is the same as that of the CA91C015 DARF and signal timing is similar. Upgrading existing CA91C015 designs to take advantage of the 64 bit transfer mode and new DMAC capabilities requires a change in control of the VMEbus buffers, while new designs could exploit the local bus burst mode.

New registers have been added to provide additional control and status bits for the new features, and some of the reserved bits in existing registers have been defined. Software written for the original DARF should be updated to ensure the new control bits are not inadvertently changed.

The CA91C064 still uses the standard handshakes with the CA91C014 ACC for acquisition and use of the local and VMEbusses, and no changes are required with respect to the ACC.

### CA91C014 ACC Description

The CA91C014 ACC is the companion to the CA91C064 DARF64 and provides all the service functions required for a VMEbus interface. Utilities required on most CPU-based cards such as an interrupt handler, clock and reset generation are also provided. A brief list of CA91C014 functionality is given below.

*System Controller Functions*

- Automatic SYSCON Determination
- VMEbus Arbiter
- IACK Daisy Chain Driver
- 16 MHz SYSCLK Driver

*VMEbus Utilities*

- Auto-ID Logic
- VMEbus Requester
- VMEbus Interrupter
- VMEbus Interrupt Handler
- VMEbus Reset Generator

*Local Utilities*

- BI-mode Controller
- Local Reset Generator
- Local Interrupt Handler
- Local Bus Arbiter/Requester
- Tick and Watchdog timers
- General purpose clocks
  (1 uS, 14 uS, 14 mS, 8 MHz, 2.4615 MHz)

The VMEbus arbiter provides four arbitration modes, including round robin, priority, and mixed arbitration modes. The VMEbus requester similarly has several request, ownership, and release modes available.

The interrupt handler processes all seven VMEbus interrupts, six local general purpose interrupts, and five dedicated level seven interrupts.

### Typical Circuit using CA91C064 DARF64

Figure 26 illustrates a typical AVICS-based VMEbus card. The core of the card is the CPU with its address decoder and memory. The VMEbus interface is supplied by the ACC, DARF64, and the external buffers and delay lines used by the DARF64. The VSB interface would be selected by the DARF64 for any transfers in a VME-out space mapped as a VSB region. Application specific logic is not normally accessible to the DARF64, but is connected to the same local bus as the memory.

A CPU access to the VMEbus begins when the address decoder selects the AVICS interface for that address with the VMEOUT signal. The DARF64 will request the ACC to obtain the VMEbus, after which it will perform the read or write, controlling the direction of its buffers appropriately. If the CPU is accessing an address in its own VMEbus slave image, then the DARF64 will assert RAMSEL to the CPU address decoder to enable local memory instead of requesting the VMEbus.

Incoming cycles from the VMEbus, once recognized by the address decoding and protection logic in the DARF64, cause the local bus to be requested from the ACC. The ACC arbitrates between requests from the DARF64 and a possible second local bus requester. Once the DARF64 has been granted the bus, it will perform the pending atomic or decoupled cycles.



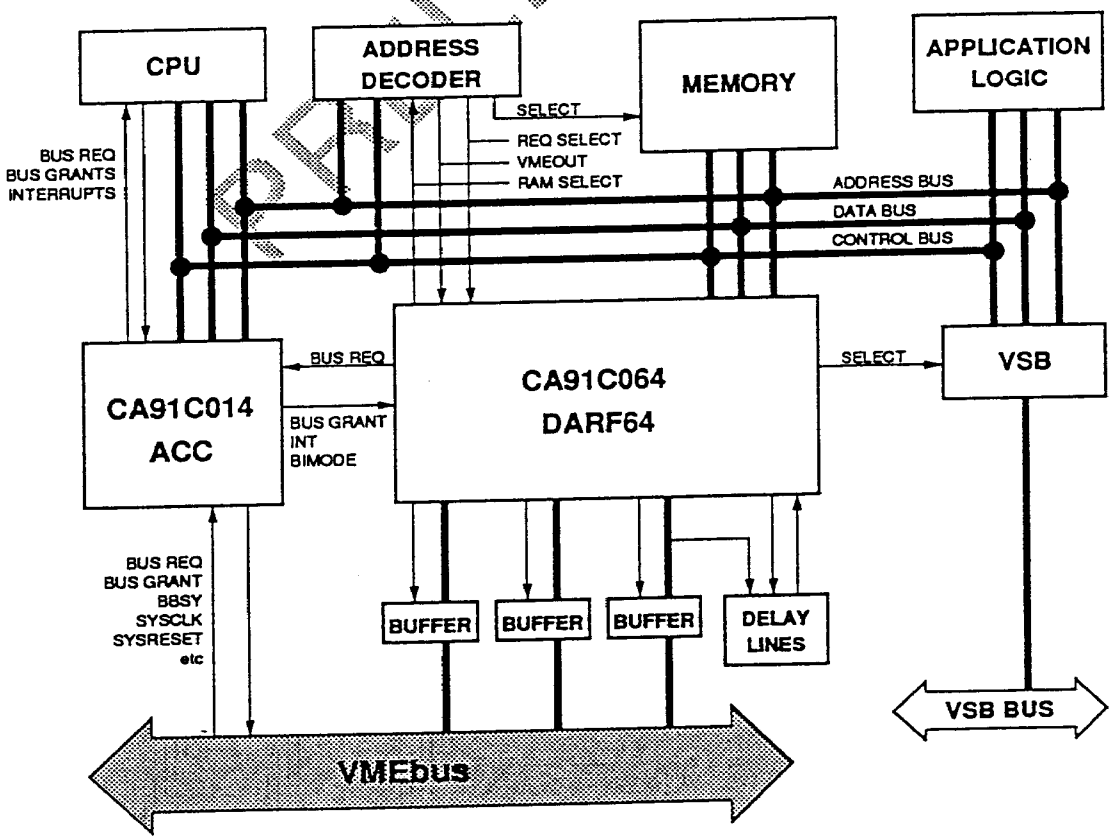
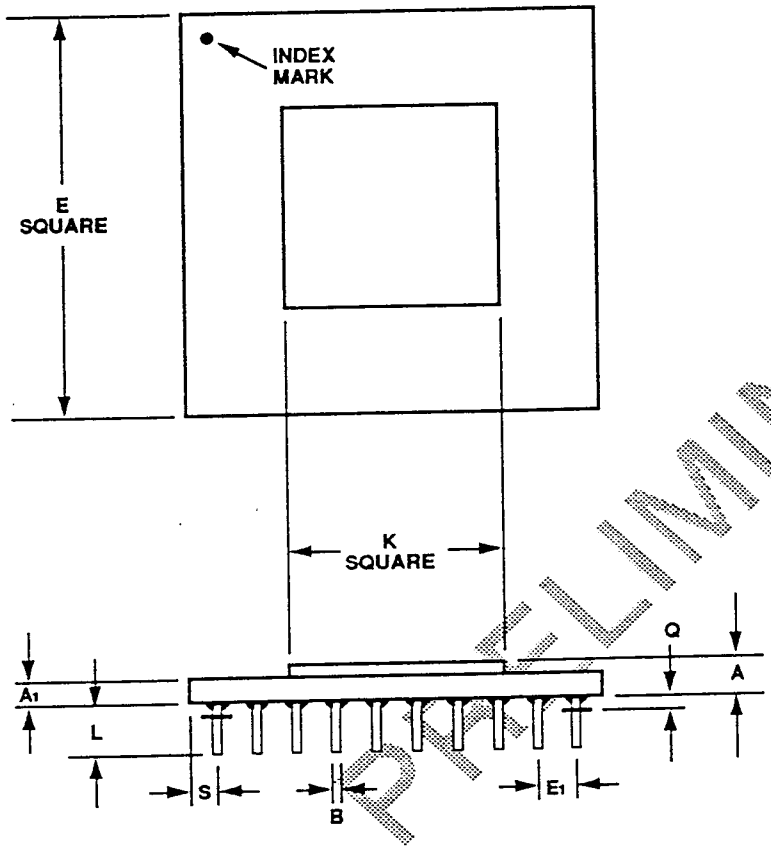



Figure 27 : CA91C064 DARF64 APPLICATION CIRCUIT

## MECHANICALS



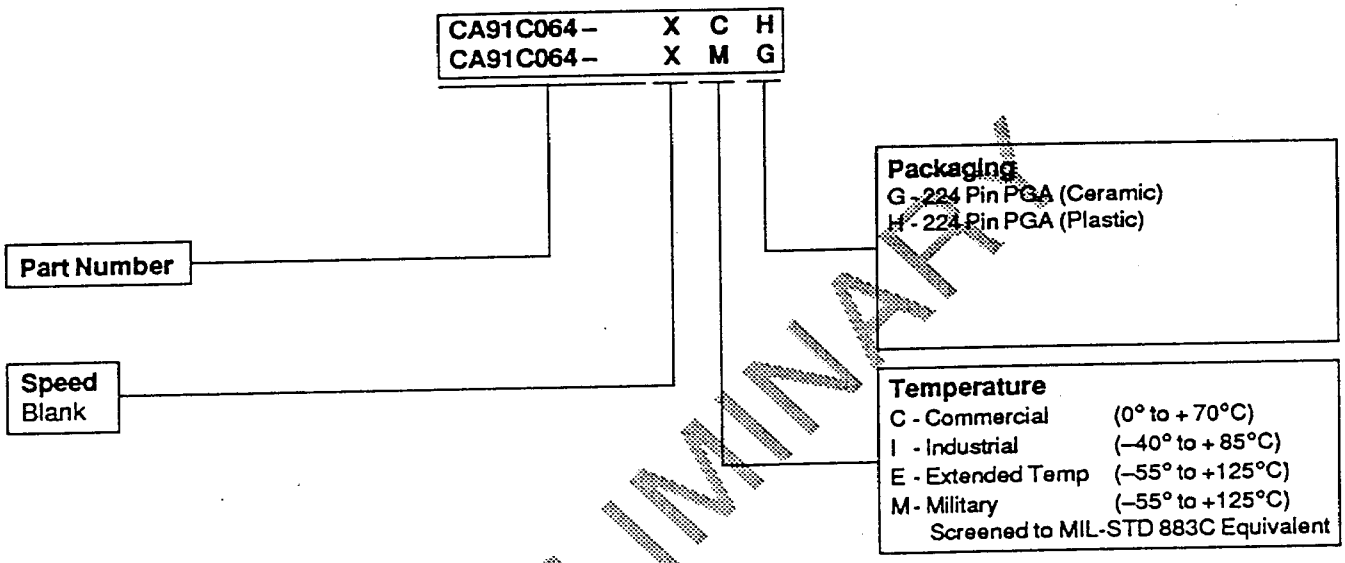

| DIMENSION | PGA 224 CERAMIC | |
|---|---|---|
| | Min | Max |
| A | .115 (2.92) | .145 (3.58) |
| A1 | .115 (2.92) | REF |
| B | .016 (0.41) | .020 (0.51) |
| E | 1.730 (43.94) | 1.780 (45.21) |
| E1 | .084 (2.13) | .116 (2.95) |
| K | .750 (19.05) | REF |
| L | .170 (4.32) | .190 (4.83) |
| Q | .050 (1.27) | REF |
| S | .075 (1.91) | REF |
| NOTES | 1, 3, 5, 7, 10 | |



Notes:

1. Gold plating 50 microinches thickness over 100 microinches nominal thickness of nickel.
2. Gold plating thickness is 20 microinches, minimum, over 200 microinches, minimum, of nickel, over 0.5oz. copper.
3. Lid may be ceramic or gold and nickel plated Kovar.
4. Lid is black anodized aluminum.
5. Base is ceramic.
6. Base is a printed circuit board (PCB).
7. Pins are Kovar or Alloy 42 plated with gold and nickel.
8. Pins are Kovar W/90/10 solder plate or hot solder dipped (increase B MAX by .003 inches (.08 mm) copper.
9. No standoff.
10. Extra pin is for alignment/polarity only.

## ORDERING INFORMATION and PRODUCT CODE






*Newbridge Microsystems* products are designated by a Product Code. When ordering, refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact our factory directly.

*® BI-mode is a registered trademark of DY-4 Systems Inc., denoting the Bus Isolation mode.*

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