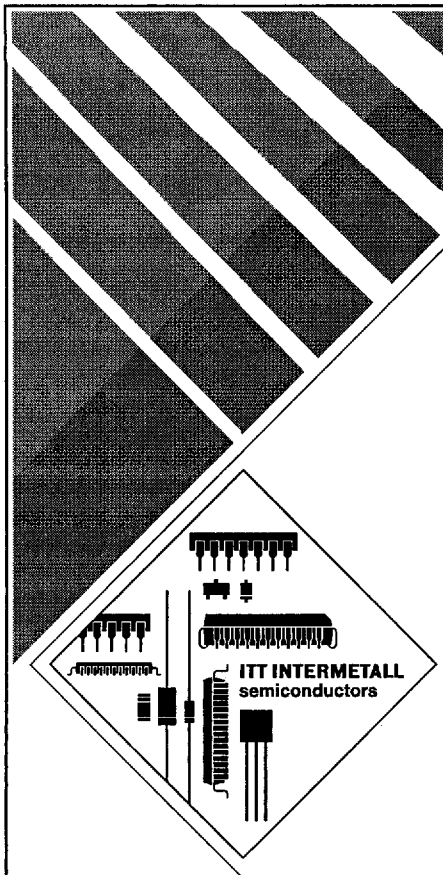

PRELIMINARY DATA SHEET

CAP 3540B, CAP 3541B Car Audio Processor Hardware

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Car Audio Processor

1. Introduction

The CAP 3540B Car Audio Processor is a new CMOS processor and represents the one-chip solution for a highly integrated AM/FM radio concept.

The CAP 3540B is designed for car radio concepts and can also be used for home stereo receivers, as well as for PC radio cards.

The CAP 3541B is especially designed for applications without digital audio sources. Digital audio input is not supported in the CAP 3541B. All other features are compatible to the CAP 3540B. In the following description, only the CAP 3540B is mentioned.

The typical application consists of the following components:

- Car Audio Processor CAP 3540B
- conventional FM tuner and FM-IF stage
- conventional AM tuner and AM-IF stage
- microcontroller
- analog and digital (only with CAP 3540B) audio sources
- power amplifiers

1.1. Features

- High-quality audio A/D converters with input selectors for several analog audio sources
- D/A converters with 8-fold oversampling filters
- Baseband audio processing (bass/treble, loudness, volume, balance and fader control)
- Stereo decoder
- Noise concealment for weak FM signals, including Automatic Separation Control, Hi-Blend and Volume-Blend function
- Ignition noise canceller: removes peak noise from the audio signal and interpolates the disturbed audio samples
- RDS processing: demodulation of the Radio Data System signal; RDS clock and data are available via hardware pins and software control bus
- Deemphasis and 19 kHz Pilot tone filter for FM
- Detection of field strength, multipath and peak noise levels
- Music search for tape player
- Freely programmable Digital Audio Interface for CD/DCC and coprocessor applications (only with CAP 3540B)
- Synthesizer with 3 current sources for fast FM/AM tuning

A more detailed overview about the integrated DSP-features is given in the additional Application Note Software CAP 3540B.

2. Functional Description

2.1. Architecture

The architecture of the CAP 3540B processor comprises three main function blocks:

2.1.1. DSP Block

The DSP block consists of a "General-Purpose16-Bit Digital Signal Processor" which handles 24 million instructions per second. The data word length is 16 bits and the hardware multiplier operates with an initial word length of 16 · 10 with a 20-bit result. The memory covers 256 · 16+256 · 10 bit RAM and 2 k instruction ROM.

2.1.2. Digital Part

A main portion consists of hardwired digital filters, such as decimation filters for the A/D converters and interpolation filters for D/A converters. The modulators for ARI/RDS and pilot tone, as well as the complete circuitry for the ignition noise canceller are realized digitally. The logical conclusion for a higher integration is the incorporation of the synthesizer for AM and FM tuning into this hardware block. Naturally, the customary serial interfaces for digital audio signals are also included.

2.1.3. Analog Part

In the analog part various input switches, A/D converters and D/A converters are combined. Five A/D converters handle the conversion of analog signals into digital signals. Two of these are specially designed for high quality, one in particular for the conversion of an independent signal path for ARI/RDS signals and the remaining two to be used for the evaluation of analog signals of a lower quality standard (information on field strength and information from potentiometers). Two D/A converters, each equipped with an eightfold oversampling filter, generate analog output signals. These two outputs can be split up and distributed into four output stages via four independently adjustable volume control switches.

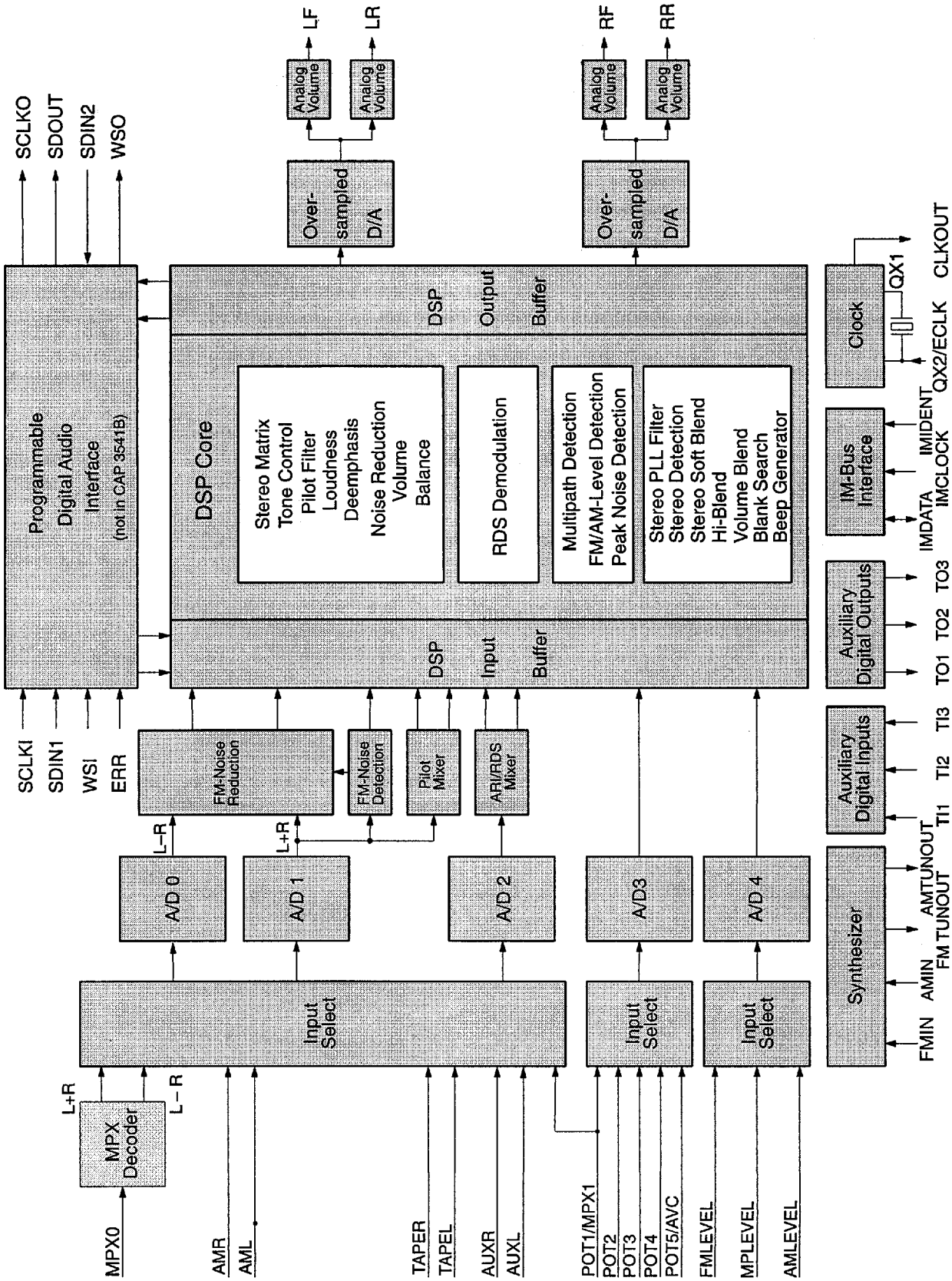


Fig. 2–1: CAP 3540B block diagram

2.1.4. Operating Modes

The CAP 3540B possesses 3 main operating modes:

1. MPX-mode

In this mode, the CAP 3540B receives the multiplex signal of an FM transmission, containing sum and difference channel, the pilot tone and the signals needed for travel information (ARI, RDS). The FM-demodulation has to take place inside the conventional tuner. The mixing of the difference band is done by an analog mixer in front of the A/D-converters in order to achieve the necessary quality for FM stereo. The ARI and RDS signals and the pilot tone are extracted digitally.

2. AF-mode

In this mode the CAP 3540B works transparently; the incoming signals are A/D-converted and then transmitted to the DSP core.

3. XDS-mode (not in CAP 3541B)

In this mode there is an external digital source (XDS, e.g. a CD player) which sends its digital data to the CAP 3540B for further processing and for the reconverting to analog signals. The CAP 3540B can be adapted to the sampling rate (32 to 44,1 kHz) prescribed by the external digital source; in addition the input systems of the CAP 3540B remain active in order to monitor the traffic and field strength information.

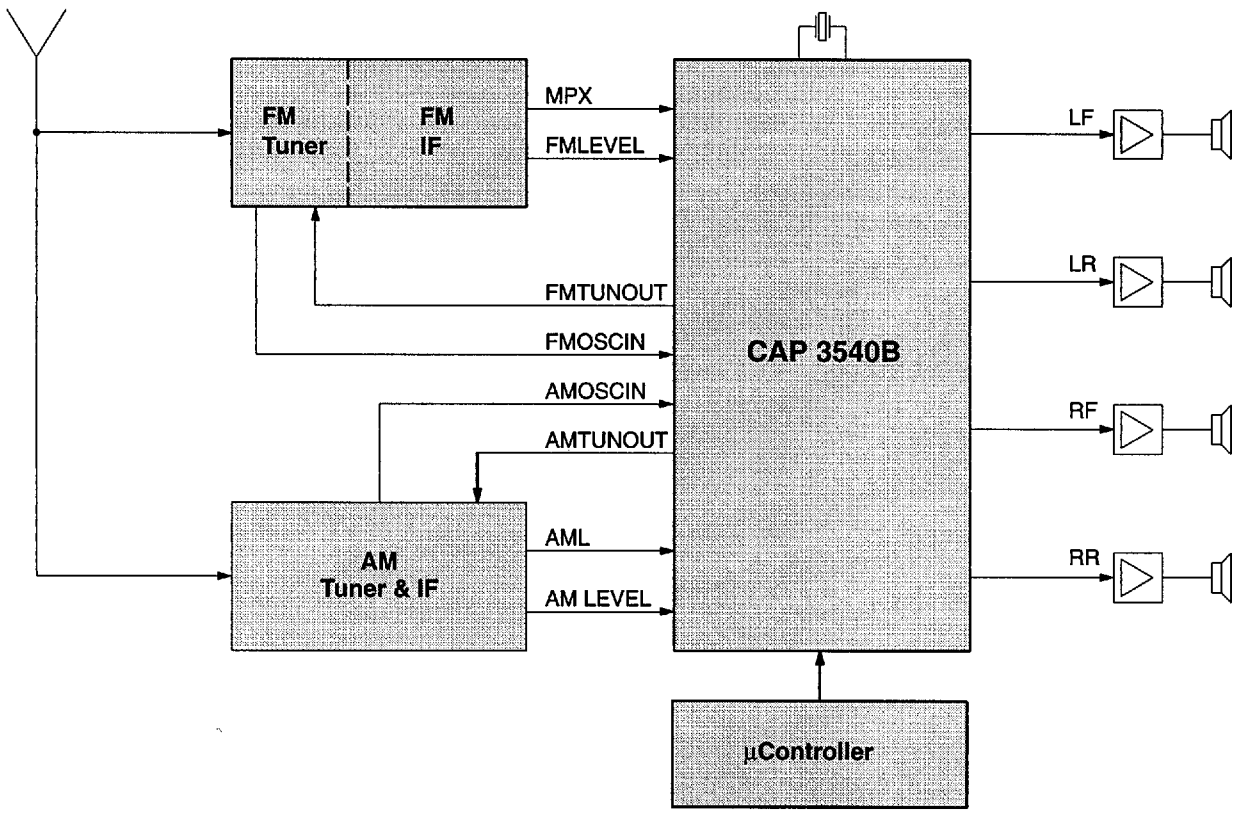


Fig. 2–2: CAP 3540B system overview

After buffering (ABUF) and switching (AMUX) in the AF-mode the signals are converted into digital form by 2 A/D converters (ADCs). Their output is 1 bit at a rate of 8.208 MHz; in each of the two channels in the CAP 3540B there is a cascade of 3 lowpass filters (LPF02, LPF23 and LPF34), which suppresses the high-frequency noise produced by the ADCs. The outputs of the filters LPF34 are 16 bits wide and are sampled with 38 kHz; these samples are transmitted via the input buffer to the DSP core. After processing in the DSP, the samples are interpolated to the eightfold sampling rate and converted into analog shape by 2 D/A converters (DACs), filtered (ALPF) and optionally attenuated (AVOL) to feed the power amplifiers which produce the signals for four loudspeakers.

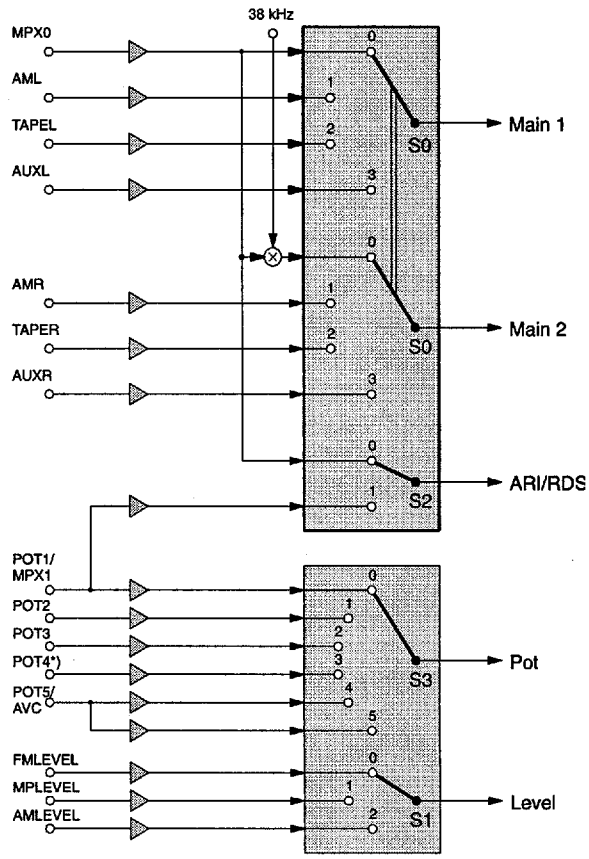
It is assumed that the process of stereo multiplexing used in radio broadcasting is known. The main FM-modulator can be modulated by the sum signal of left and right channel (in baseband), a pilot tone, the difference channel (AM-modulated, suppressed carrier), an optional ARI signal (AM-modulated, unsuppressed carrier), an optional RDS signal (AM-modulated, suppressed carrier) and optionally up to 3 SCA signals (FM-modulated). The composite signal is the so-called MPX signal. So a variety of signals ride "piggy-back" on the main carrier, which was originally assigned only for monophonic transmission. In the CAP 3540B, the SCA signals are regarded as disturbing signals while the others are regarded as useful.

In the MPX-mode there is an analog mixer AMIX in front of the ADCs. It mixes the difference band down to baseband. The sum channel and the difference channel are then treated like the other baseband signals. Digital quadrature mixers ARIMX and PILMX extract the RDS-information and the information of the pilot signal, respectively.

By means of digital mixers the pilot tone and the RDS (Radio Data System) signal are mixed down to zero intermediate frequency in quadrature representation, where their information is sampled and sent to the DSP core. The demodulation of the RDS signal is done by the DSP software. Beside these main blocks, there are other systems. The analog field strength information FS delivered by AM and FM tuners is A/D-converted; after lowpass-filtering (LPF06) the samples are sent to the DSP core, where the information could be used to control some parameters of the entire system. Other input signals, such as signals from external potentiometers are selected by an analog multiplexer, A/D-converted, lowpass-filtered and sent to the DSP or to the controller via the IM-bus interface (IMIF). The IM-bus interface is also able to receive data from the external microcontroller and to control the systems on the CAP 3540B.

2.2. Analog Input Systems

Fig. 2–3 shows all analog inputs and functions of the switches S0 to S3.



*) POT4 not available in PSDIP64 package.

Fig. 2–3: Analog input systems

2.2.1. Buffers ABUF

The analog input buffers have to adjust the individual desired input levels in order to cover the entire volume range of the A/D-converters.

The inputs can be divided into two groups: those which have to be connected via external capacitors, and those that are DC-coupled. Two of these inputs, the POT1/ MPX1 and POT5/AVC, are DC-coupled if used as POT1 resp. POT5, and AC-coupled if used as MPX1 resp. AVC.

Note: Input pins POT1 to POT5 are switchable to digital outputs via the IM-bus interface. This feature is made possible by open drain transistors and external pull-up resistors down to 1 kΩ.

2.2.2. Stereo Mixer AMIX

This analog demodulator mixes the incoming multiplex signal with the PLL-synchronized 38 kHz subcarrier in order to get the difference channel in baseband.

The phase of the mixer signal is locked to the phase of the digital pilot demodulator; the phase shift between the two signals has to be compensated by the signal processor's Stereo PLL software.

The realized modulator consists of an analog multiplexer switching among the original input signal, the inverted input signal and zero input.

The desired fundamental 38 kHz component includes an additional factor of 1.10266 which has to be taken into account in the dematrix-software of the signal processor.

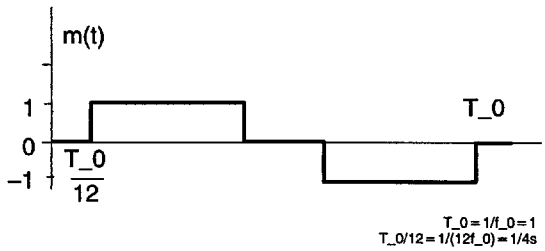


Fig. 2–4: Difference channel mixing signal

2.2.3. Multiplexers AMUX

The analog multiplexers allow the selection of one of the input signals for each signal path.

2.2.4. A/D-Converters ADC

The A/D-converters are realized as pulse density modulators (PDMs) running at a clock frequency of f_s0 = 8.208 MHz. The ADC0, ADC1 and the ADC2 are high quality double-loop PDMs with one external capacitor whereas ADC3 and ADC4 are low quality PDMs without any external capacitor.

2.2.5. Digital Signal Processing Block

2.2.5.1. Digital Filter Sections

After analog to digital conversion, the input signals are filtered by means of digital filters in order to decimate the high frequency PDM signals to an appropriate sampling rate. The second purpose of these filters is to suppress unwanted out-of-band signals and to shape the input signals to the desired response. After being processed in the DSP section, the digital samples are interpolated to a higher rate before being converted to the analog domain. The individual filter blocks can be seen in Fig. 2–5 and 2–6. Fig. 2–5 shows filter sections for the A/D side whereas in Fig. 2–6, filter blocks for the interpolation process on the D/A side can be seen. In the text of this data sheet, the filter blocks are referred to with the names indicated in the schematics.

Most of the filters are designed as multirate FIR blocks. Fig. 2–7 shows the overall (A/D to D/A) passband characteristics of the main channels in TAPE or AUX mode. The shown 3 dB bandwidth is more than 18 kHz. Fig. 2–8 shows the same for the MPX case. An additional pilot notch filter (19 kHz) suppresses higher frequencies. In case of a locked stereo PLL, the suppression is ideal.

Fig. 2–9 depicts the characteristics of the ARI/RDS bandpass. The near-by difference channel is attenuated sufficiently in order to minimize disturbing effects in the weak ARI/RDS signal. An additional lowpass with roll-off characteristics is done in the DSP software.

In order to suppress out-of-band signals, the CAP 3540B is equipped with digital interpolation filters. These filters attenuate alias frequencies of up to eight times the sampling frequency. The interpolation block consists of three cascaded linear phase FIR filters. A simple sample and hold filter serves for the interpolation to the operating rate of the D/A converter. The overall interpolation rate is therefore 32. See Fig. 2–10 for the passband characteristics of the interpolation filter (plotted for 44.1 kHz sampling rate) and Fig. 2–11 for the stopband characteristics.

2.2.6. Digital Mixing Systems

2.2.6.1. Pilot Demodulator PILMX

The entire system is synchronized with the pilot tone of the FM-stereo channel. In the pilot-demodulator 2 mixers working in quadrature are used. The quadrature mixer is the phase detector of the PLL; the other parts of the PLL (loop filter and VCO) are realized in the DSP. The inphase mixer outputs information concerning the level of the pilot tone to the DSP to allow a decision "FM-stereo" or "FM-mono". The time relation between the mixer sequences of stereo-demodulator and pilot-demodulators is fixed.

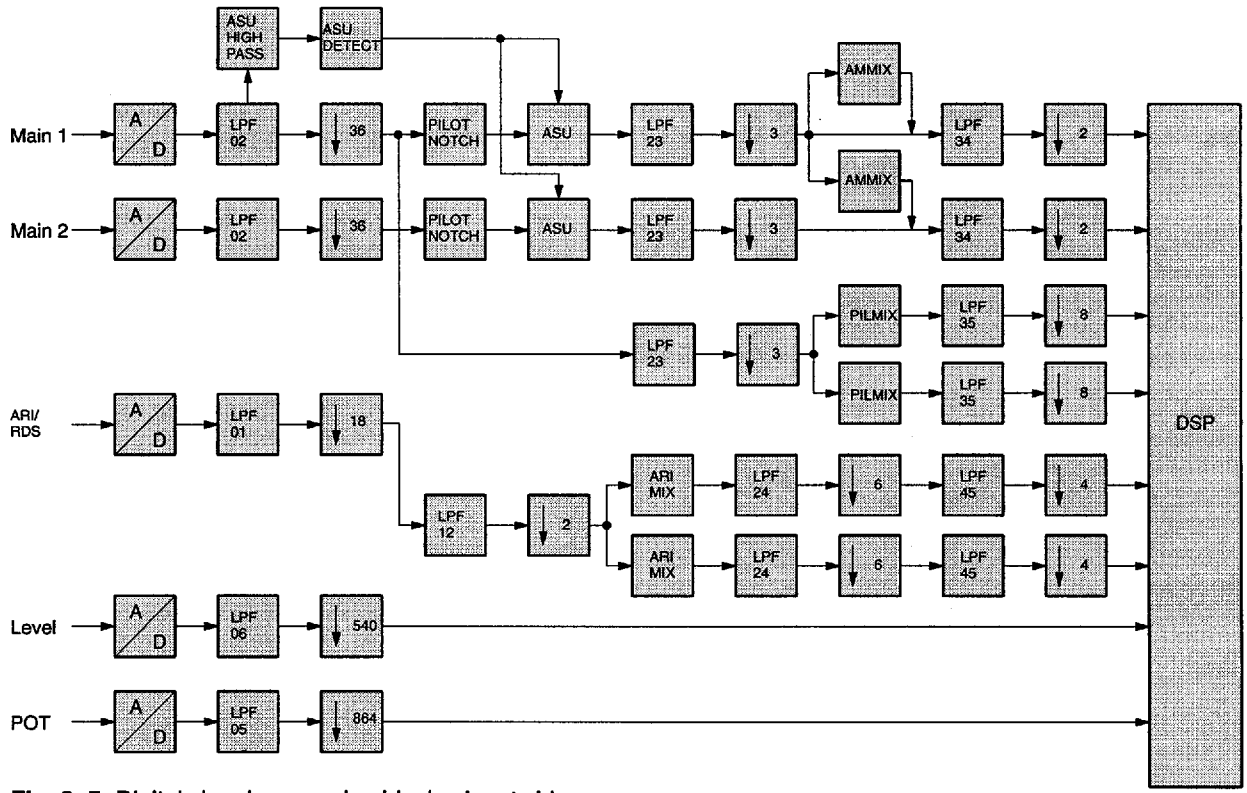


Fig. 2–5: Digital signal processing blocks, input side

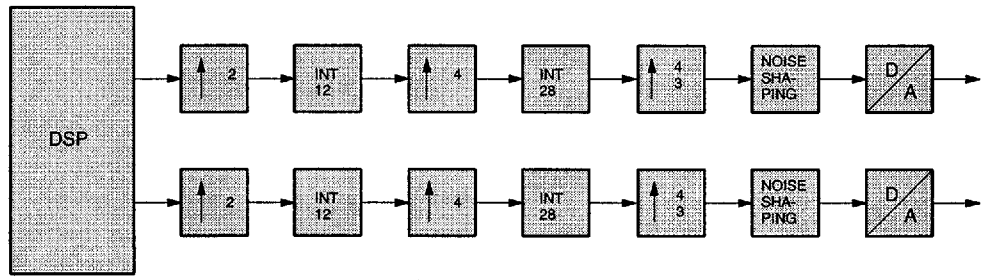


Fig. 2–6: Digital signal processing blocks, output side

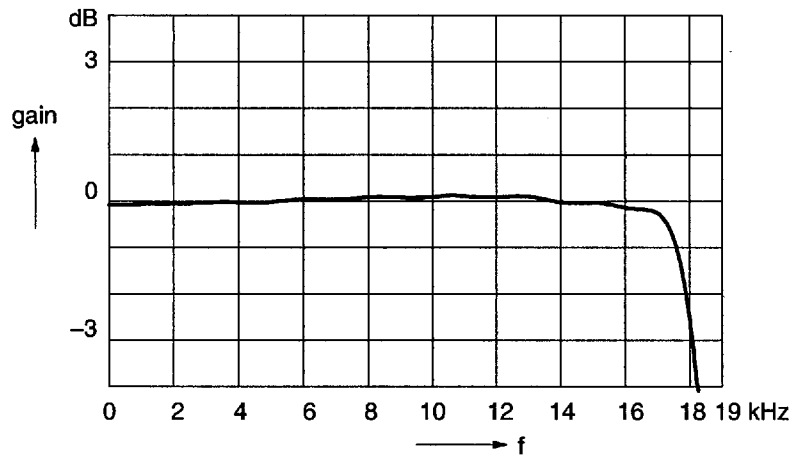


Fig. 2–7: Overall response TAPE/AUX channel

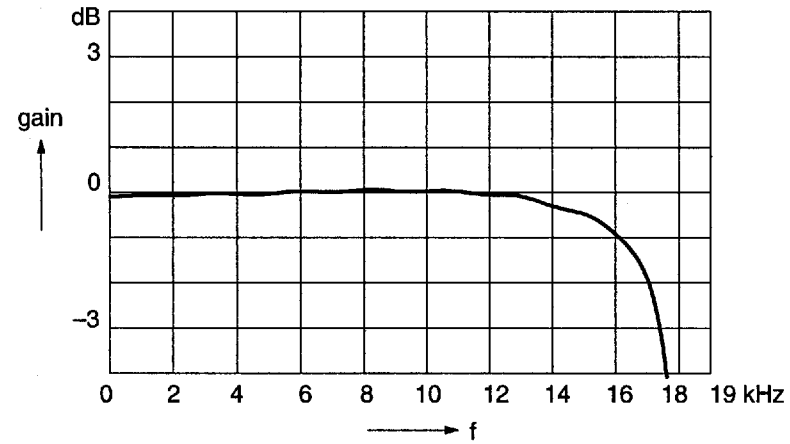


Fig. 2–8: Overall MPX response sum channel

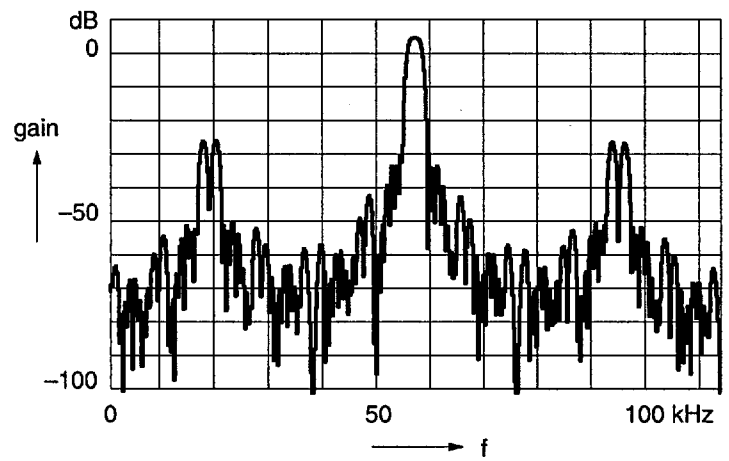


Fig. 2–9: ARI/RDS bandpass characteristic

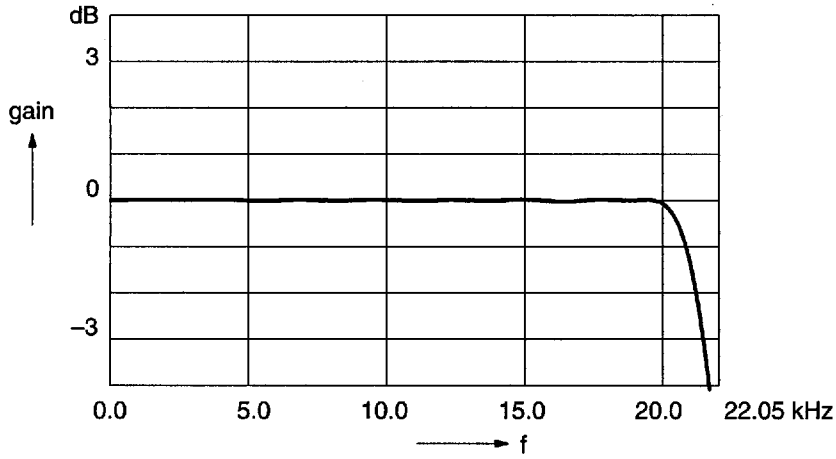


Fig. 2–10: Digital interpolation filter, passband characteristic

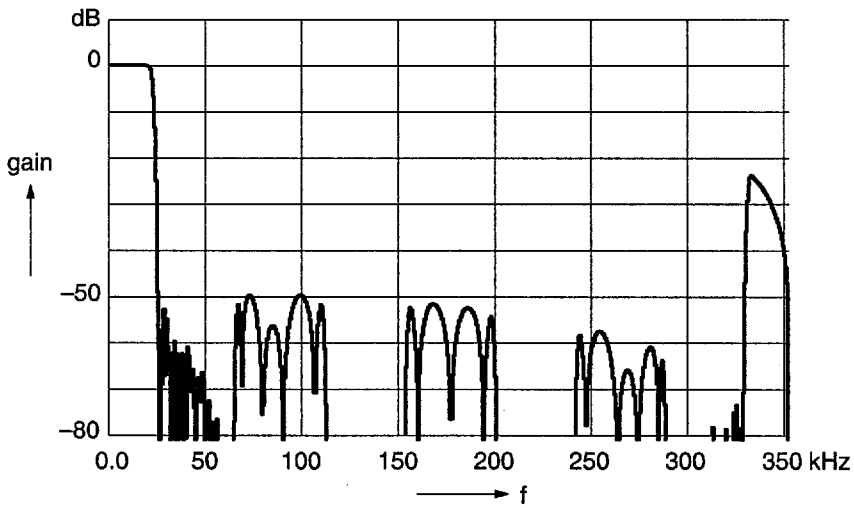


Fig. 2–11: Digital interpolation filter, attenuation

2.2.6.2. ARI Mixer ARIMX

The ARI-information in the range of 57 kHz is mixed down to a zero intermediate frequency by the two ARI mixers, whose mixer signals are again in quadrature. The reason for using two paths is that the demodulation is asynchronous in general; in the DSP there should be an operation which performs the square root of the sum of the squares of the two input signals. The quality requirements of the square rooting should not be very high. Because of the phase lock of pilot tone and ARI carrier in the FM-stereo-mode, a synchronous demodulation seems to be possible; in this case the demodulated ARI signal would be identical with the signal of the inphase path.

The chosen structure has another potential advantage, for processing the radio data system (RDS) in Europe. This signal is a part of the MPX-signal; its subcarrier frequency is the same as that of the ARI-signal but it is recommended that the two subcarriers are in quadrature. So the two paths of the ARI demodulation subsystem make the information of the ARI-signal and of the RDS-signal available to the DSP, where both can be demodulated if desired.

Please note that in this version ARI signals are not available. ARI information is replaced by the demodulation of RDS.

2.2.7. FM Noise Canceller (ASU)

The FM Noise Canceller removes peak noise from the audio signal. No external circuitry is required. All filters, delays and the control section are implemented digitally. The function is split into two sections:

- The noise detection searches for energy in the non-audio range by means of a highpass filter. The output of this filter is compared with a DSP-controlled threshold. If this threshold is exceeded the interpolation unit is triggered. The 19 kHz pilot tone is removed before the audio signal enters the detection highpass. Programmable delay adjustment makes sure of the correct timing between peak detection and peak interpolation.
- The interpolation circuit substitutes a peak-corrupted sample by the mean value of the non-corrupted adjacent samples. Once a trigger comes from the detection circuit, a programmable number (0 to 15) of successive samples is interpolated. All functions work on a 228 kHz sampling rate. At this rate the peaks are still small enough (not widened by the final decimation filters) to be removed effectively.

2.3. Analog Output Systems

2.3.1. D/A-Converters DAC

The D/A-converters used are of the oversampling type. The samples to be converted at their sampling rate f_s are first interpolated to 8 x the sampling rate and then oversampled to a higher rate f_NS where noise shaping is performed. The output of the noise shaper is then converted using a highly linear D/A-converter. Its noise power density increases with increasing frequency, the residual noise in the baseband is very low.

Only in CAP 3540B:

Within this application the DAC has to be adapted to the different modes. The digital sources (e.g. CD-player) must supply the proper clock rate in order to drive the DAC with a stable clock rate locked to the sampling rate. The clock is derived from the clock line SCLK of the PDAI bus.

2.3.2. Lowpass-Filters ALPF

The analog lowpass-filters behind the DACs eliminate the high-frequent noise in order to avoid any distortions in the AM frequency range.

2.3.3. Volume Control AVOL

The analog volume control together with the digital volume control implemented in the digital signal processor's software provide a large volume control range. The analog volume control itself covers a range of 45 dB in 1.5 dB steps and includes an additional mute position. The analog volume control can be adjusted for all 4 output channels individually.

A sensible splitting of the total gain v_tot between the digital gain v_dig and the analog gain v_anlg is

v_tot	v_anlg	v_dig
v_tot ≥ 0 dB	0 dB	v_tot
–45 dB<v_tot<0 dB	v_tot	0 dB
v_tot<–45 dB	–45 dB	v_tot+45 dB

All control bits for the hardware section are first addressed to the DSP core program. In case of hardware read-registers the bits are transmitted to the DSP core, stored in the DSP RAM and are thus available for the controller via the DSP's IM-bus interface.

2.4. Programmable Digital Audio Interface PDAI (not included in CAP 3541B)

The PDAI is the digital audio interface between the CAP 3540B and external digital sources such as CD/MD player or additional external processors. It offers a large variety of modes and should therefore cover most of the digital audio standards (I^2S-compatible formats).

Fig. 2–12 shows a standard application with an external digital source and a second CAP 3540B. The interface is split into the input section and the output section:

Input Section:

- SCLKI serial clock input
- SDIN1 serial data input 1
- WSI word select input
- ERR error line input

Output Section:

- SCLKO serial clock output
- SDOUT serial data output
- SDIN2 serial data input 2
- WSO word select output

Fig. 2–13 shows the timing of the signals and the programmable features. The programming is done by writing the correct bit patterns into the DSP output buffer. This must be handled by the DSP software.

The modes are

- 16-bit wordframe
  in this case the programmable delay is set to zero;
- 24-bit wordframe
  in this case the programmable delay is set either to 0 or to 8 × Tbck; this allows left or right adjusted handling of the 16 data bits
- 32-bit wordframe
  in this case the programmable delay is set either to 0 or to 16 × Tbck; this allows left or right adjusted handling of the 16 data bits.

In all modes:

- MSB or LSB-first can be selected,
- one-bit delay between active slope of WSI/O and first wordframe bit is programmable,
- the polarity of WSI/O can be programmed,
- in the 24 and 32-bit wordframes the open data bit locations are MSB or LSB extended (depends on left or right adjustment).

Input format and output format can be programmed separately. The restrictions are

- A 24-bit wordframe can only be sent if a 24-bit wordframe is also received. In the analog input mode, the 24-bit wordframe output is not allowed.

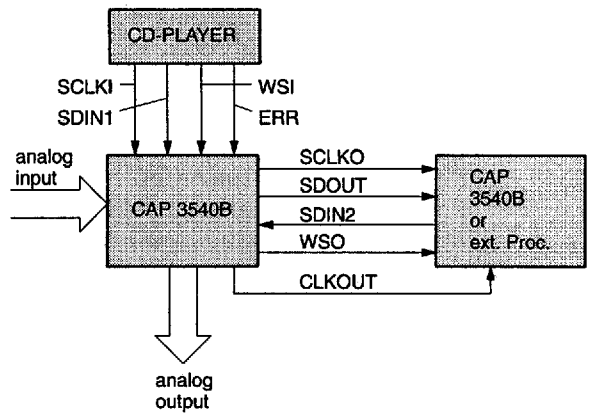


Fig. 2–12: System configuration

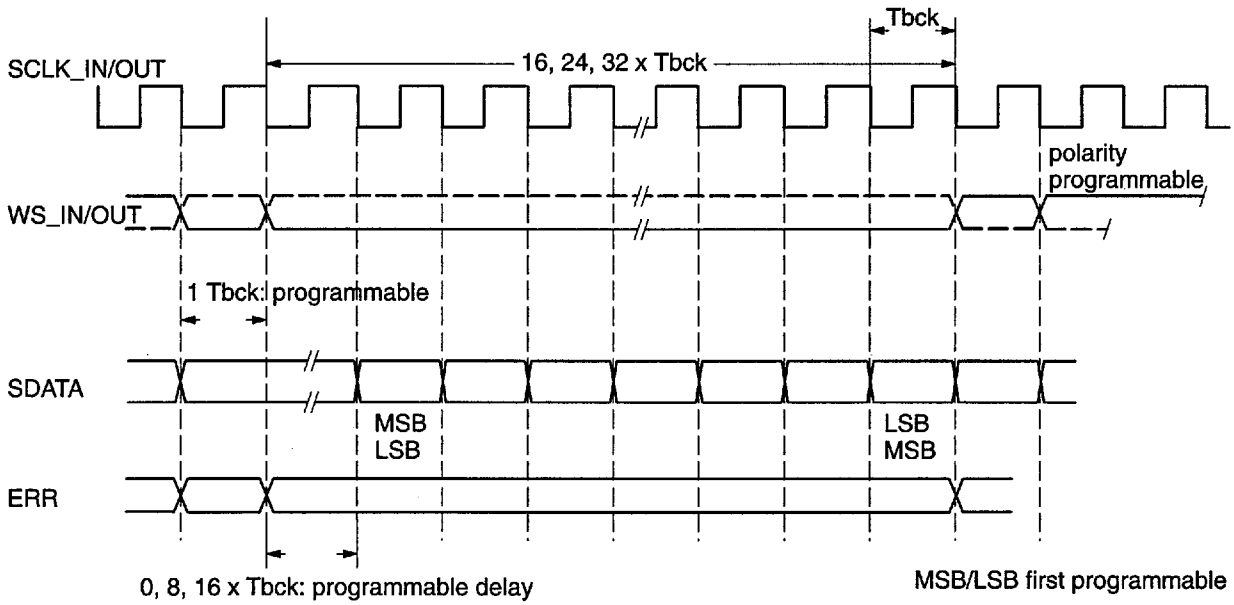


Fig. 2–13: Timing of the signals
Tbck = 1/Fbck
Fbck = 32 · Fsaudio or
Fbck = 48 · Fsaudio or
Fbck = 64 · Fsaudio

2.5. The IM-Bus Interface of the CAP 3540B

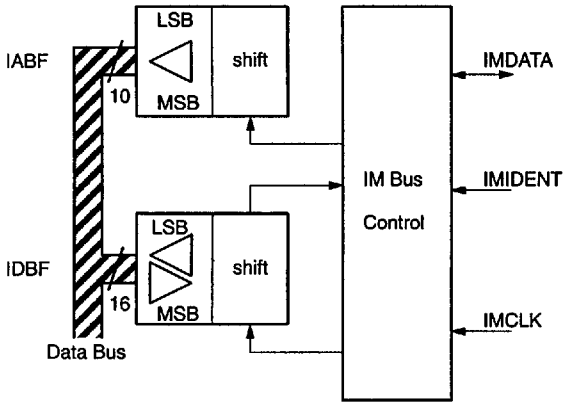


Fig. 2–14: IM-bus interface

The buffer part consists of a unidirectional address buffer IABF with a word length of 10 bit and the bidirectional data buffer IDBF with a word length of 16 bit. It is only possible to write to the address buffer from the peripheral equipment.

By means of the IM-bus interface it is possible, for example, to alter the filter coefficients of the CAP 3540B. For this purpose, the microcomputer writes an address and a data word to the appropriate buffers IABF and IDBF. ***The 10-bit address contains an address part of 8 bits (bit 9 to bit 2), a read/write bit (bit 0) and an additional bit (bit 1) which is used for selecting one of the two address counter banks***
(Fig. 2–15). Bits 0 and 1 have the following effect:

ABNK = 0 selects address counter bank 1
ABNK = 1 selects address counter bank 2

R/W = 0 selects Write, microcomputer wants to write
R/W = 1 selects Read, microcomputer wants to read

MSB	Address	LSB	ABNK	R/W

Fig. 2–15: Address format

The following convention is applicable to the data transfer: The last bit written always becomes the MSB of IABF or IDBF. If fewer bits are transferred than the respective buffer size, the unused bits are set to zero in IDBF but remain undefined in IABF. For the output: the first bit output is always the LSB of the IDBF.

2.5.1. Description of the IM-Bus

The IM-bus consists of three lines for the signals Ident (IMIDENT), Clock (IMCLK) and Data (IMDATA). The clock frequency range is 50 Hz to 1 MHz. Ident and clock are unidirectional from the controller to the slave ICs, Data is bidirectional. Bidirectionality is achieved by using open-drain outputs with on-resistances of 150 Ohm maximum. The 2.5 kΩ pull-up resistor common to all outputs is incorporated in the controller.

The timing of a complete IM-bus transaction is shown in Fig. 2–16. In the non-operative state the signals of all three bus lines are High. To start a transaction, the controller sets the ID signal to Low level, indicating an address transmission, sets the CL signal to Low level and switches the first bit on the Data line. Then 10 address bits are transmitted, beginning with the LSB. Data takeover in the slave ICs occurs at the positive edge of the clock signal. At the end of the address byte the ID signal goes High, initiating the address comparison in the slave circuits. In the addressed slave the IM-bus interface switches over to Data read or write, because these functions are correlated to the address.

In the case of a read operation, a fixed wait period has to be observed. This period is defined by the IM-bus handler in the DSP software. For practical reasons this part of the program does not run at the full sampling rate. It is recommended to place the IM-bus handler in a "low speed" time slice in order to save processing power.

For a write operation this wait period does not have to be observed, but please note that the maximum rate of IM-bus transmissions is normally limited by the DSP software.

Also controlled by the address the controller now transmits sixteen clock pulses, and accordingly two Bytes of data are written into the addressed IC or read out from it, beginning with the LSB. The completion of the bus transaction is signalled by a short Low state pulse of the ID signal. This initiates the storing of the transferred data. A bus transaction may be interrupted for up to 10 ms.

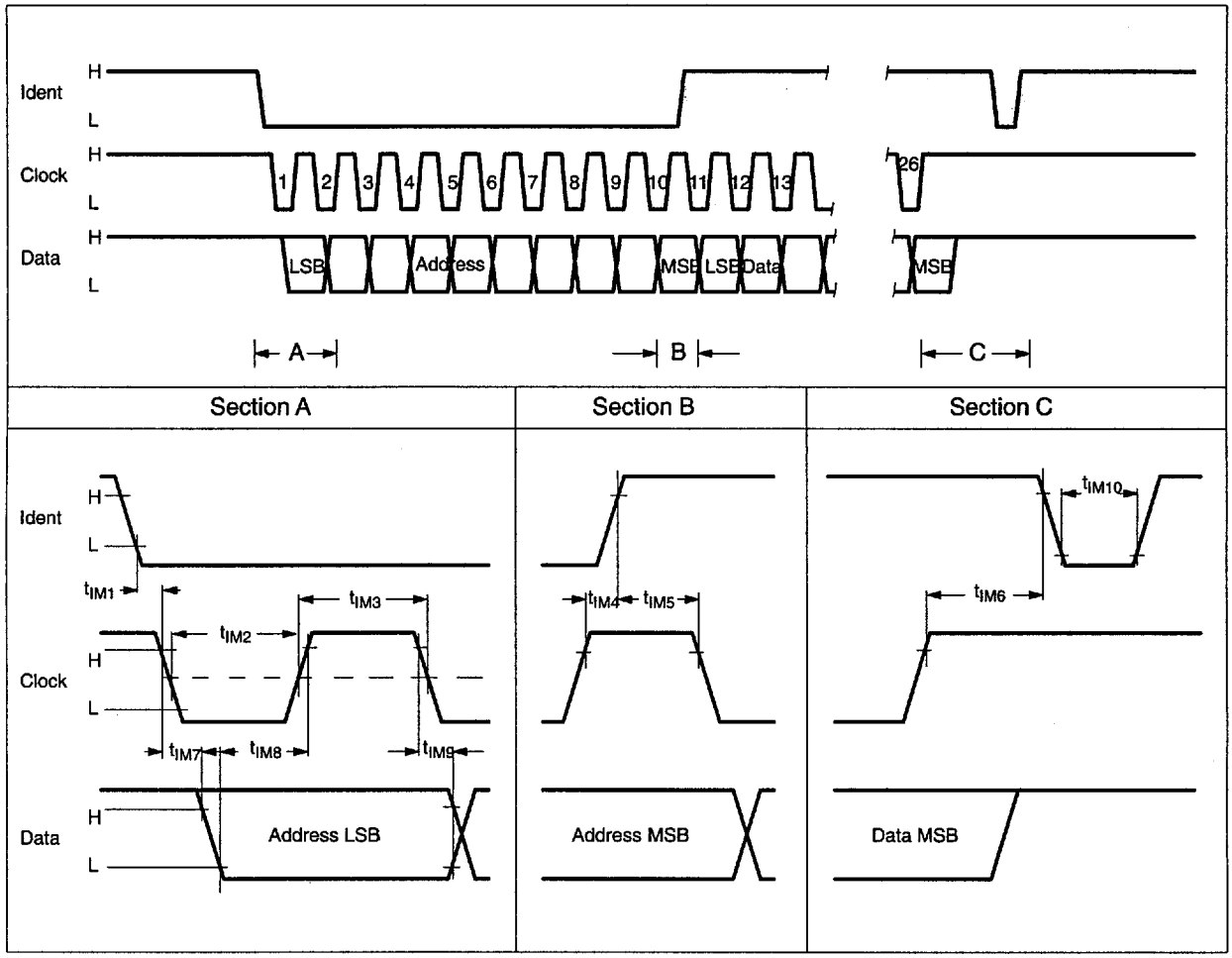


Fig. 2–16: IM-Bus waveforms

2.6. Clock Generation

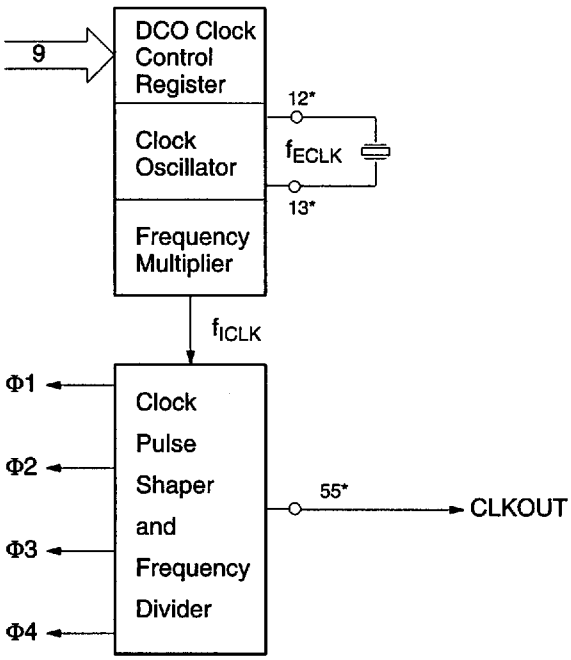
The CAP 3540B processor has an integrated clock oscillator which is crystal-controlled and oscillates with the frequency f_{ECLK} = 16.416 MHz. All components of the oscillator are integrated except for the quartz crystal. This is connected to the QX1 and QX2 oscillator pins. The crystal input QX2/ECLK can be used to supply the CAP 3540B externally with the required clock. In this case no crystal is needed.

Following the clock oscillator is a frequency multiplier with a factor of 3. The output of the frequency multiplier delivers the f_{ICLK} internal clock frequency, by which the DSP Core is clocked.

There is the possibility of pulling the f_{ECLK} oscillator frequency in a range of 350 ppm, depending on the application and the used crystal. This makes it possible to synchronize the CAP 3540B to the incoming pilot tone signal in the case of MPX reception.

Table 2–1: Oscillator characteristics

DCO Content	Frequency
011111111B	$f_{ECLKmin}$
000000000B	f_{ECLK}
100000000B	$f_{ECLKmax}$



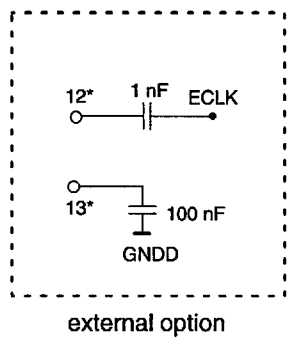


Fig. 2–17: Clock generator connections

*PSDIP64 package

3. Specifications

3.1. Outline Dimensions

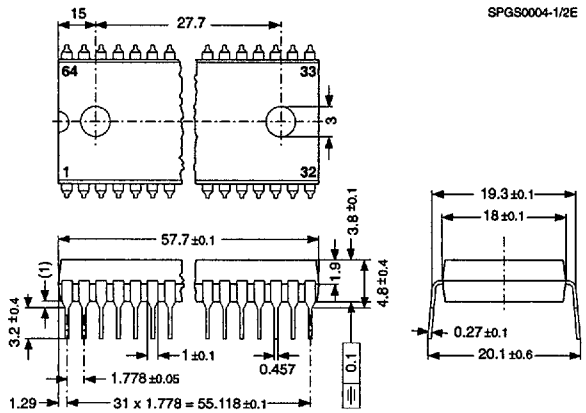


Fig. 3–1:
64-Pin PSDIP Plastic Shrink Dual Inline Package
(PSDIP64)
Weight approximately 9.0 g
Dimensions in mm

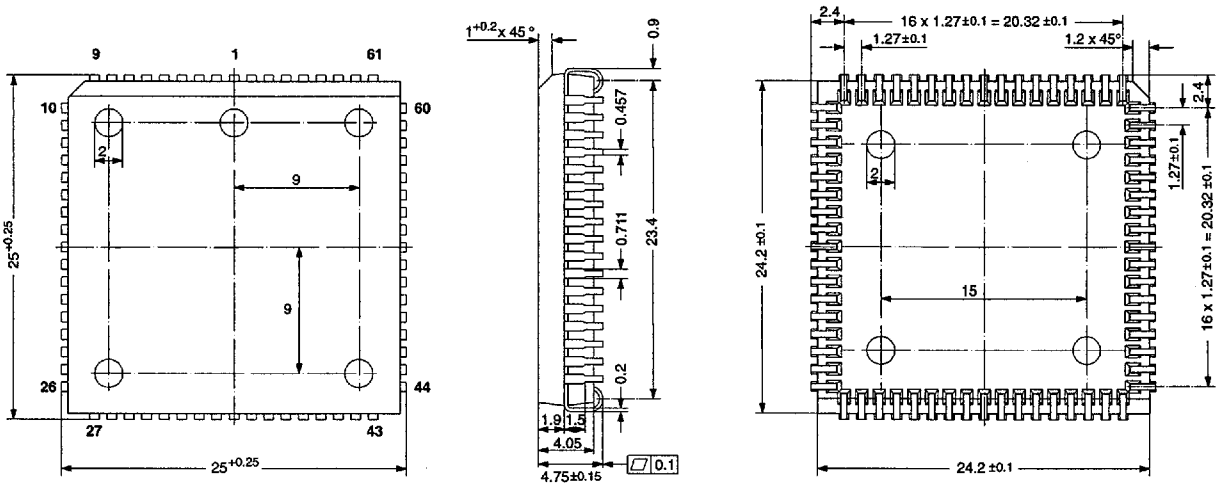


Fig. 3–2:
68-Pin Plastic Leaded Chip Carrier Package
(PLCC68)
Weight approximately 4.8 g
Dimensions in mm

3.2. Pin Connections and Short Descriptions

LV = if not used, leave vacant
X = obligatory; connect as described in circuit diagram

Pin No. PSDIP 64-pin	Pin No. PLCC 68-pin	Pin Name	Type	Connection (if not used)	Short Description
1	51	SDOUT	OUT	LV	Serial data output
2	50	WSO	OUT	LV	Serial word select output
3	49	SCLKO	OUT	LV	Serial clock output
4	48	TI3	IN	LV[1)]	Static digital input 3
5	46	TI1	IN	LV[1)]	Static digital input 1
6	45	REFCLK	IN	LV	Synthesizer Ref. Frequency input
7	44	TEOSC	IN	GNDD	Test purpose
8	43	IMIDENT	IN	X	IM-bus ident input
9	42	IMCLK	IN	X	IM-bus clock input
10	41	IMDATA	IN/OUT	X	IM-bus data input/output
11	40	RESET	IN	X	Reset input
12	39	QX2/ECLK	IN	X	Crystal/External clock input
13	38	QX1	IN	X	Crystal
14	37	TESTEN	IN	GNDD	Test Mode Enable
15	36	GNDS1	SUPPLY	X	Analog ground synthesizer
16	35	FMOSCIN	IN	LV	FM oscillator signal input
17	34	FMOSCREF	IN	LV	FMOSC capacitor connection
18	33	AMOSCIN	IN	LV	AM oscillator signal input
19	32	AMOSCREF	IN	LV	AMOSC capacitor connection
20	31	VSUP1	SUPPLY	VREF2	Analog supply voltage synthesizer
21	30	VSUP2	SUPPLY	VREF2	Analog supply voltage synthesizer
22	29	AMTUNOUT	OUT	LV	AM tuning voltage output
23	28	TUNFB	IN	LV	Tuning voltage feedback input
24	27	FMTUNOUT	OUT	LV	FM tuning voltage output
25	26	VREF2	IN	GNDA	Analog ground reference synthesizer
26	25	RF	OUT	LV	Analog output right front
27	24	RR	OUT	LV	Analog output right rear
28	23	LR	OUT	LV	Analog output left rear

Pin Connections and Short Descriptions, continued

Pin No. PSDIP 64-pin	Pin No. PLCC 68-pin	Pin Name	Type	Connection (if not used)	Short Description
29	22	LF	OUT	LV	Analog output left front
30	21	VSUPA	SUPPLY	X	Analog supply voltage
31	20	GNDA	SUPPLY	X	Analog ground
32	19	VREF1	IN	X	Analog ground reference
33	18	AGNDC	OUT	X	Internal analog ground
34	16	PDMC2	IN/OUT	BAGNDC	PDM capacitor connection
35	15	PDMC1	IN/OUT	BAGNDC	PDM capacitor connection
36	14	PDMC3	IN/OUT	BAGNDC	PDM capacitor connection
37	17	BAGNDC	OUT	LV	Buffered internal ground
38	13	TAPEL	IN	BAGNDC	Analog Tape input left
39	12	TAPER	IN	BAGNDC	Analog tape input right
40	11	AUXL	IN	BAGNDC	Auxiliary audio input left
41	10	AUXR	IN	BAGNDC	Auxiliary audio input right
42	9	AMR	IN	BAGNDC	AM right baseband input
43	8	AML	IN	BAGNDC	AM left baseband input
44	7	MPX0	IN	BAGNDC	FM MPX signal input
45	6	POT1/MPX1	IN/OUT	GNDA	DC voltage input
46	5	POT2	IN/OUT	GNDA	DC voltage input
47	4	POT3	IN/OUT	GNDA	DC voltage input
48	2	POT5/AVC	IN/OUT	GNDA	DC voltage input
49	1	FMLEVEL	IN	GNDA	FM field strength input
50	67	AMLEVEL	IN	GNDA	AM field strength input
51	66	TP1	IN	GNDD	Test purpose
52	65	TP4	OUT	LV	Test purpose
53	64	TP2	OUT	LV	Test purpose
54	63	TP3	IN	GNDD	Test purpose
55	62	CLKOUT	OUT	LV	Clock output
56	61	VSUPD	SUPPLY	X	Digital supply voltage
57	60	GNDD	SUPPLY	X	Digital ground

Pin Connections and Short Descriptions, continued

Pin No. PSDIP 64-pin	Pin No. PLCC 68-pin	Pin Name	Type	Connection (if not used)	Short Description
58	59	TO3	OUT	LV	Digital output 3
59	58	TO2	OUT	LV	Digital output 2
60	57	TO1	OUT	LV	Digital output 1
61	56	SDIN1	IN	LV	Serial data input 1
62	55	WSI	IN	LV	Serial word select input
63	54	SCLKI	IN	LV	Serial clock input
64	52	SDIN2	IN	LV	Serial data input 2
–	3	POT4	IN/OUT	GNDA	DC voltage input
–	47	TI2	IN	LV[1)]	Static digital input 2
–	53	ERR	IN	LV	Serial error input
–	68	MPLEVEL	IN	GNDA	Multipath signal input

[1)] Depending on software version

3.3. Pin Descriptions

The pin numbers refer to the PSDIP64 package.

Pin 1 – SDOUT
DAI-Bus: serial data output.

Pin 2 – WSO
DAI-Bus: word select output; this is a control line to separated left and right channel in the serial DAI stream.

Pin 3 – SCLKO
DAI-Bus: serial clock output.

Pins 4 to 5 – TI1, TI3
Static digital inputs; these signals can be used as a branch condition in the DSP software. If not used, they must be connected to GND.

Pin 6 – REFCLK
Input for the synthesizer reference frequency.

Pin 7 – TEOSC
Test purpose.

Pins 8 to 10 – IMDATA, IMCLK, IMIDENT
Via these pins the CAP 3540B sends and receives data to and from the controller.

Pin 11 – RESET
In the steady state, high level is required at this pin. A low level resets the CAP 3540B.

Pin 12 – QX2/ECLK
Crystal pin. This pin has to be connected with the crystal or with an external clock signal.

Pin 13 – QX1
Crystal pin. This pin has to be connected with the crystal.

Pin 14 – TESTEN
Test mode enable

Pin 15 – GNDS1
This pin serves as ground connection for the HF parts of the synthesizer section.

Pin 16 – FMOSCIN
Input for the FM oscillator signal.

Pin 17 – FMOSCREF
Capacitor connection for FMOSCIN reference voltage.

Pin 18 – AMOSCIN
Input for the AM oscillator signal.

Pin 19 – AMOSCREF
Capacitor connection for AMOSCIN reference voltage.

Pin 20 – VSUP1
Synthesizer supply voltage 1; power is supplied via this pin for the synthesizer circuitry of the CAP 3540B.

Pin 21 – VSUP2
Synthesizer supply voltage 2; power is supplied via this pin for the synthesizer output circuitry of the CAP 3540B.

Pin 22 – AMTUNOUT
Tuning voltage for the AM oscillator.

Pin 23 – TUNFB
Feedback input for tuning voltage amplifier.

Pin 24 – FMTUNOUT
Tuning voltage for the FM oscillator.

Pin 25 – VREF2
This pin serves as ground connection for the synthesizer bias circuits and must be connected separately to the ground point of the tuner.

Pin 26 – RF
Right front speaker output.

Pin 27 – RR
Right rear speaker output.

Pin 28 – LR
Left rear speaker output.

Pin 29 – LF
Left front speaker output.

Pin 30 – VSUPA
Analog supply voltage; power for the analog circuitry of the CAP 3540B is supplied via this pin.

Pin 31 – GNDA
This pin serves as ground connection for the analog signals and NF parts of the synthesizer section.

Pin 32 – VREF1
This pin must be connected separately to the single ground point. It serves as ground connection for the analog bias circuits.

Pin 33 – AGNDC
This pin serves as internal ground connection for the analog circuitry. It must be connected to analog ground with a 4.7 µF and a 100 nF capacitor in parallel.

Pins 34 to 36 – PDMC3, PDMC2, PDMC1
Capacitor pins for the feedback loop of the high quality pulse-density modulators.

Pin 37 – BAGNDC
Buffered internal ground. This pin is the buffered internal ground connection for the external PDM capacitors.

Pin 38 – TAPEL
Input for left tape channel.

Pin 39 – TAPER
Input for right tape channel.

Pin 40 – AUXL
Input for additional audio sources, left channel.

Pin 41 – AUXR
Input for additional audio sources, right channel.

Pin 42 – AMR
Input for right channel baseband audio.

Pin 43 – AML
Input for left channel baseband audio (AM mono).

Pin 44 – MPX0
Input for the MPX signal in case of FM reception.

Pins 45 to 48 – POT5/AVC, POT3, POT2, POT1/MPX1
Inputs for a DC-control voltage (0V to V_{SUP}). These pins can also be used as digital outputs with an external pull-up resistor; the function and selection is controlled via IM-bus.

POT1/MPX1 also serves as a second MPX input for ARI/RDS signals.

POT5/AVC also serves as a highly sensitive microphone input.

Pin 49 – FMLEVEL
Input for the FM field strength information.

Pin 50 – AMLEVEL
Input for the AM field strength information.

Pin 51 – TP1
Test purpose.

Pin 52 – TP4
Test purpose.

Pin 53 – TP2
Test purpose.

Pin 54 – TP3
Test purpose.

Pin 55 – CLKOUT
This output is used for clocking external hardware.

Pin 56 – VSUPD
Digital supply voltage. Power is supplied via this pin for the digital circuitry of the CAP 3540B.

Pin 57 – GNDD
This pin serves as ground connection for the digital signals.

Pins 58 to 60 – TO1, TO2, TO3
Digital outputs; the logical state can be defined by the DSP software.

Pin 61 – SDIN1
DAI-Bus: serial data input 1.

Pin 62 – WSI
DAI-Bus: word select input; this is a control line to separate left and right channel in the serial DAI stream.

Pin 63 – SCLKI
DAI-Bus: serial clock input.

Pin 64 – SDIN2
DAI-Bus: serial data input 2.

The following pins are available only in the 68-pin PLCC package:

– POT4
Input for a DC-control voltage (0 V to V_{SUP}). This pin can also be used as digital output with an external pull-up resistor; the function and selection is controlled via IM-bus.

– TI2
Static digital input; this signal can be used as a branch condition in the DSP software. If not used, it must be connected to GND.

– ERR
DAI-Bus: error input

– MPLEVEL
Input for the multipath information.

3.4. Pin Configuration

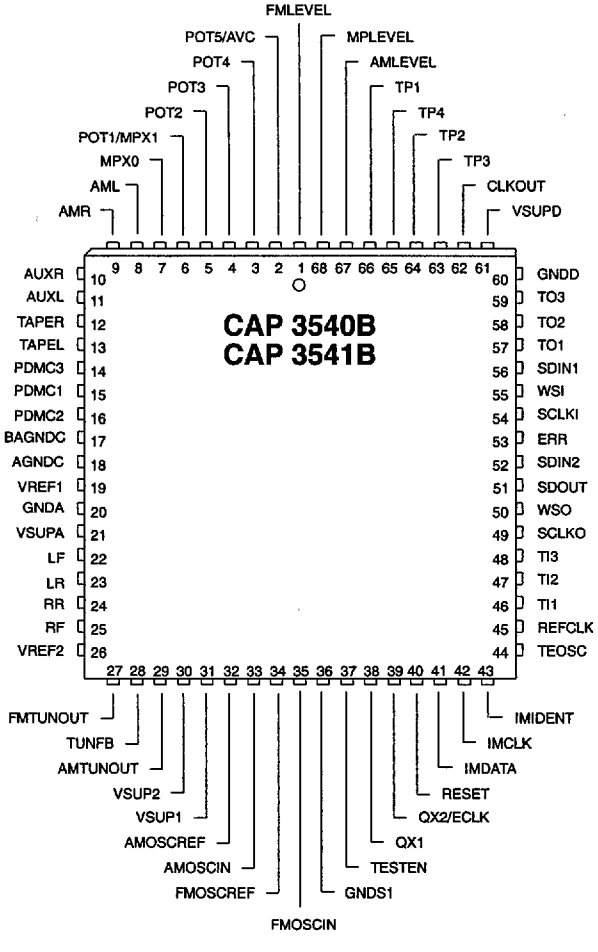


Fig. 3–3: Pinning of the CAP 3540B in PLCC68 package, top view

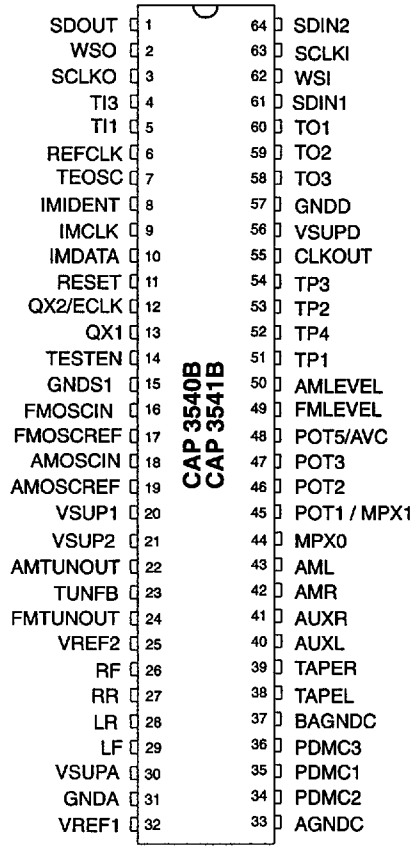


Fig. 3–4: Pinning of the CAP 3540B in PSDIP64 package, top view

MPLEVEL not available
ERR not available
POT4 not available
TI2 not available
(internally pushed to GND)

3.5. Electrical Characteristics

All voltages refer to ground. All pin numbers refer to the PSDIP64 package.

3.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	–20	+85	°C
T_S	Storage Temperature	–	–55	+125	°C
V_{SUP}	Supply Voltage	30, 56	–0.3[1)]	+6	V
V_{SUP1}	Supply Voltage	20	–0.3[1)]	+6	V
V_{SUP2}	Supply Voltage	21	–0.3[1)]	+12	V
P_{max}	Maximum Power Dissipation 68-pin PLCC without heat spreader	20, 21, 30, 56	–	1300	mW
dV_{SUP}	Voltage between VSUPA, VSUPD, and VSUP1	30, 56, 20	–0.5	+0.5	V
dV_{SUP2}	Voltage between VSUP2 and VSUPA, VSUPD, and VSUP1	21	–	+8.5	V
V_I	Input Voltage, all Inputs	4 to 10, 12, 13, 16 to 19, 23, 37 to 50, 61 to 64	–0.3	V_{SUP} +0.3	V
I_O	Output Current, all Outputs	1 to 3, 10, 22, 24, 26 to 29, 55, 58 to 60	–	2) 3)	–

1) Reversed supply 200 ms maximum.
2) The outputs are short-circuit proof (max. 5 seconds) with respect to supply and ground.
3) Total chip power dissipation must not exceed absolute maximum ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions/Characteristics of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

3.5.2. Recommended Operating Conditions at $T_A = -20$ to $+85$ °C, $f_{ECLK} = 16.416$ MHz, typical values at $T_j = 27$ °C, duty cycle = 50%

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{SUP}	Supply Voltage	30, 56	4.75	5.0	5.25	V
V_{SUP1}	Supply Voltage	20	4.75	5.0	5.25	V
V_{SUP2}	Supply Voltage	21	7.5	9.0	10.5	V
V_{ECLKL}	ECLK Clock Input Low Voltage	12	–	–	1.5	V
V_{ECLKH}	ECLK Clock Input High Voltage		V_{SUP} –1.5	–	–	V
$\frac{t_{ECLKH}}{t_{ECLKL}}$	ECLK Clock Input High/Low Ratio		0.9	1.0	1.1	–
f_{ECLK}	ECLK Clock Input Frequency (see also section 3.5.3.)		–	16.416	–	MHz
$V_{REFCLKH}$	Reference Clock Input High Voltage	6	V_{SUPD} –1.5	–	–	V
$V_{REFCLKL}$	Reference Clock Input Low Voltage		–	–	1.5	V
f_{REFCLK}	Refence Clock Input Frequency		1		16	MHz
V_{FS}	DC Input Voltage FM, AM, [MP] level	49, 50	0		V_{SUP}	–
$V_{POT/MPXI}$	DC Input Voltage POT5, [POT4], POT3, POT2, POT1	45 to 48	0		V_{SUP}	–
V_{IH}	High Level, Digital Inputs	2 to 5, 61 to 64	2.0			V
V_{IL}	Low Level, Digital Inputs				0.8	V
V_{REIL}	$\overline{\text{Reset}}$ Input Low Voltage	11	–	–	0.8	V
V_{REIH}	$\overline{\text{Reset}}$ Input High Voltage		V_{SUP} –0.8 V	–	–	–
V_{IMIL}	IM Bus Input Low Voltage	8 to 10	–	–	1.5	V
V_{IMIH}	IM Bus Input High Voltage		3.0	–	–	V
$f_{\Phi I}$	ΦI IM Bus Clock Frequency		0.05	–	1000	kHz
t_{IM1}	ΦI Clock Input Delay Time after IM Bus Ident Input		0	–	–	–
t_{IM2}	ΦI Clock Input Low Pulse Time		0.5	–	–	µs
t_{IM3}	ΦI Clock Input High Pulse Time		0.5	–	–	µs
t_{IM4}	ΦI Clock Input Setup Time before Ident Input High		0	–	–	–
t_{IM5} write data	ΦI Clock Input Hold Time after Ident Input High		0.25	–	–	µs
t_{IM5} read data	ΦI Clock Input Hold Time after Ident Input High		defined by DSP software			µs

Recommended Operating Conditions, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
t_{IM6}	ΦI Clock Input Setup Time before Ident End-Pulse Input	8 to 10	1.0	–	–	µs
t_{IM7}	IM Bus Data Input Delay after ΦI Time Clock Input		0	–	–	–
t_{IM8}	IM Bus Data Input Setup Time before ΦI Clock Input		0	–	–	–
t_{IM9}	IM Bus Data Input Hold Time after ΦI Clock Input		0	–	–	–
t_{IM10}	IM Bus Ident End-Pulse Low Time		1.0	–	–	µs
C_{PDM}	PDM Capacitor (Low Loss Type)	34 to 36	–5%	680	+5%	pF
C_{AGNDC}	AGNDC-Filter-Capacitor	33		3.3		µF
	Ceramic Capacitor in parallel			100		nF
f_{SCLKI}	Input SCLKI Frequency	63	–	–	3.1	MHz
t_{SIJ}	Input SCLKI Phase Jitter		–	–	250	ps
t_{SIW}	Input SCLKI Pulse Width		40	50	60	%
t_{IDS}	Input Data Setup Time	61, 64	40	–	–	ns
t_{IDH}	Input Data Hold Time		0	–	–	–
t_{WSS}	Input WSI Setup Time Output WSO Setup Time	2, 62	40	–	–	ns
t_{WSH}	Input WSI Hold Time Output WSO Hold Time		0	–	–	–

3.5.3. Recommended Crystal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Ambient Operating Temperature	–20	–	+85	°C
f_P	Parallel Resonance Frequency	–	16.416[1)]	–	MHz
$\frac{\Delta f_S}{f_S}$	Accuracy of Adjustment	–	–	±20	ppm
$\frac{\Delta f_S}{f_S}$	Frequency Deviation versus Temperature	–	–	±40	ppm
R_r	Series Resistance	–	–	15	Ω
C_0	Shunt Capacitance	5.5	–	7	pF
C_1	Motional Capacitance	25	30	–	fF
df	Frequency pulling range	350[2)]	–	–	ppm

[1)] at $C_L = 10.7$ pF [2)] at $\Delta C_L = 12$ pF

Remark on defining the external load capacitance: External capacitors at each crystal pin to ground are required. The higher the capacity, the lower the clock frequency results. Due to different layouts of customer PCBs, the matching capacitor size should be defined in the application.

3.5.4. Characteristics at $T_A = -20$ to $+85$ °C, V_{SUP} and $V_{SUP1} = 4.75$ to 5.25 V, $V_{SUP2} = 7.5$ to 10.5 V, $f_{ECLK} = 16.416$ MHz, typical values at V_{SUP} and $V_{SUP1} = 5.0$ V, $V_{SUP2} = 9.0$ V, $T_j = 27$ °C and duty cycle = 50%.

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
Z_{AII1}	Analog Input Impedance (MPX1, MPX0, AM, AUX, TAPE) at $T_j = 27$ °C at $T_A = -20$ to $+85$ °C	38 to 45, 48	 27 26	35	 43 47	 kΩ kΩ	$f_{signal} = 1$ kHz, $i = 0.5$ µA
Z_{AII2}	Analog Input Impedance FM, AM, [MP] level	49, 50		2		MΩ	
Z_{AVC}	Analog Input Impedance (AVC) at $T_j = 27$ °C at $T_A = -20$ to $+85$ °C	48	 3.2 3.1	4.2	 5.2 5.7	 kΩ kΩ	$f_{signal} = 1$ kHz, $i = 0.5$ µA
Z_{POT}	Analog Input Impedance (POT1 to 5)	45 to 48		2		MΩ	
V_{OSCI0}	Open Circuit Voltage (FMOSCIN, AMOSCIN, REFCLK)	16, 18, 6		$\frac{V_{SUP1}}{2}$		–	
R_{OPOT}	Output Resistance (POT1 to 5 as outputs)	45 to 48		80		Ω	$i \leq 5$ mA
R_{OSCI}	Analog Input Resistance (FMOSCIN, AMOSCIN, FMOSCREF, AMOSCREF) at $T_j = 27$ °C at $T_A = -20$ to $+85$ °C	16 to 19		 3.2 2.1	 3.6 3.6	 4.2 6.5	 kΩ kΩ
C_{OSCI}	Analog Input Capacitance (FMOSCIN, AMOSCIN, FMOSCREF, AMOSCREF)			4		pF	
R_{AO}	Analog Output Resistance (LF, LR, RR, RF) at $T_j = 27$ °C, at $T_A = -20$ to+85 °C	26 to 29	 470 440	600	 730 790	 Ω Ω	$f_{signal} = 1$ kHz, $i = 1$ mA
$V_{MPX0/1I}$	Input Voltage (MPX0, MPX1)	44, 45			2.0	V_{PP}	
$V_{AML/RI}$	Input Voltage (AML, AMR)	42, 43			1.1	V_{RMS}	
$V_{TAPER/TAPELI}$	Input Voltage (TAPER, TAPEL)	38, 39			1.6	V_{RMS}	
$V_{AUXR/LI}$	Input Voltage (AUXR, AUXL)	40, 41			1.1	V_{RMS}	
V_{AVCI}	Input Voltage (AVC)	48			14	mV_{RMS}	
V_{AICL}	Analog Audio Input Clipping Level (defines 0 dBr)	38 to 45	Max. Input Voltage	Max. Input Voltage +1 dB	Max. Input Voltage +2 dB		
Z_{AOL}	Analog Output Load	26 to 29	6		 1	kΩ nF	
V_{AOV}	Maximum Analog Output Voltage (LF, LR, RR, RF) Analog Input Digital Input		 0.8 0.9	 0.9 1.0	 1.0 1.1	 V_{RMS} V_{RMS}	output attenuation = 0 dB, analog output load > 100 kΩ

1) CD-Mode, $f_s = 44.1$ kHz
2) unused analog inputs connected to ground

Characteristics, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{AMOSC}	AM OSC Input Voltage	18	40		300	mV_{RMS}	
f_{AMOSCI}	AM OSC Input Frequency Range		0.5		20	MHz	
V_{FMOSCI}	FM OSC Input Voltage	16	40		300	mV_{RMS}	
f_{FMOSCI}	FM OSC Input Frequency Range		60		150	MHz	
SNR_{AD}	SNR A/D	38 to 44	82	85		dB	Noise measurement RMS unweighted, BW = 20 to 18000 Hz, input level = –20 dBr, f_{signal} = 1 kHz
SNR_{DA}	SNR D/A Analog Attenuation = 0 dB Analog Attenuation = 45 dB	26 to 29	 90 60	 95 65		 dB dB	RMS, unweighted, BW = 20 to 20000 Hz[1], input level = –20 dBFS, f_{signal} = 1 kHz
G_{DAM}	D/A Output Attenuation in MUTE position			110		dB	RMS, unweighted, BW = 20 to 20000 Hz[1], input level = –20 dBFS, f_{signal} = 1 kHz
THD_{AD}	THD A/D	38 to 44			0.03	%	RMS, unweighted, BW = 20 to 18000, input level = –3 dBr, f_{signal} = 1 kHz
THD_{DA}	THD D/A	26 to 29			0.01	%	BW = 20 to 20000 Hz[1], input level = –3 dBFS, f_{signal} = 1 kHz, analog attenuation = 0 dB
IMD_{AD}	Intermodulation Distortion A/D	38 to 44		0.01		%	f_{signal} = 14 kHz + 15 kHz, input level sum –3 dBr, measuring 1 kHz intermodulation[2]
XTALK1	Crosstalk attenuation within active audio channel pair	38 to 43	70			dB	input level = –3 dBr, f_{signal} = 1 kHz, measuring with bandpass at 1 kHz[2]
XTALK2	Crosstalk attenuation from a non-selected audio input pair	38 to 44	80			dB	input level = –3 dBr, f_{signal} = 1 kHz, measuring with bandpass at 1 kHz[2]
XTALK3	Crosstalk attenuation between audio input/output pairs	26 to 29, 38 to 44	100			dB	input level = –3 dBr, f_{signal} = 1 kHz, measuring with bandpass at 1 kHz[2]
$CHSEP_{MPX}$	Stereo separation MPX 250 Hz to 6.3 kHz 6.3 kHz to 12.5 kHz	14	 40 30			 dB dB	coupling capacitor on MPX input at least 1 µF
SNR_{MPX} 19 kHz	Suppression of unwanted signals in MPX stereo reception: at 19 kHz at 38 kHz at 57 kHz at 114 kHz		 45 45 60 60			 dB dB dB dB	measuring with bandpass at f_{signal}

[1] CD-Mode, f_s = 44.1 kHz
[2] unused analog inputs connected to ground

Characteristics, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
SNR_{RDS1}	SNR A/D selected MPX ARI/RDS channel	44, 45		38		dB	Noise measurement RMS, unweighted, BW = 55 to 59 kHz, input level = 55 mV_{PP} f_{signal} = 57 kHz
SNR_{RDS2}	Alias Band Suppression in RDS Channel at 171 kHz at 285 kHz		 60 70			 dB dB	f_{signal} = 57 kHz, input level = 55 mV_{PP}
SNR_{AVC}	SNR A/D3 selected AVC channel	48		56		dB	Noise measurement RMS unweighted, BW = 0 to 4 kHz, input level = –20 dBr, f_{signal} = 1 kHz
SNR_{AD4}	SNR A/D4	49, 50		54		dB	Noise measurement RMS unweighted, BW = 0 to 7 kHz, input level = –20 dBr, f_{signal} = 1 kHz
THD_{AVC}	THD A/D3 selected AVC channel	48		0.05		%	RMS unweighted, BW = 0 to 4 kHz, input level = –3 dBr, f_{signal} = 1 kHz
THD_{AD4}	THD A/D4	49, 50		0.05		%	RMS unweighted, BW = 0 to 7 kHz, input level = –3 dBr, f_{signal} = 1 kHz
BW_{ADDA}	3 dB Bandwidth A/D to D/A (TAPE, AUX)	26 to 29, 38 to 41	18			kHz	not provided in production test
BW_{DA}	3 dB Bandwidth D/A at f_s = 32 kHz at f_s = 44.1 kHz	26 to 29	 15 20			 kHz kHz	not provided in production test
dG_{AD}	Channel deviation within active input pair: AUX, TAPE AM	38 to 43			0.5 0.7	dB dB	
dG_{DA}	Channel deviation within each output of: RR, RF, LR, LF Analog attenuation = 0 to –30 dB –31.5 to –45 dB	26 to 29			 0.5 0.9	 dB dB	
dG_{AVOL}	Analog Volume Step Size (–45 dB to 0 dB)		1.4	1.5	1.6	dB	
I_{REIL}	$\overline{\text{Reset}}$ Input Leakage Current	11	–10	–	+10	µA	
I_{SUP}	Supply Current VSUPD VSUPA VSUP1 VSUP2	 56 30 20 21	 60 12 8 1.4	 85 20 11 2.2	 110 28 14 3	 mA mA mA mA	

[1] CD-Mode, f_s = 44.1 kHz
[2] unused analog inputs connected to ground

Characteristics, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{IMOL}	IM-Bus Data Output Low Voltage	10	–	–	0.4	V	
V_{IMOH}	IM-Bus Data Output High Voltage		2.8	–	–	V	
I_{IMOHL}	IM-Bus Data Output High-Impedance Leakage Current		–10	–	+10	µA	
I_{IMIL}	IM-Bus Input Leakage Current		–10	–	+10	µA	
V_{TOH} V_{TOL}	Digital Output High Voltage Digital Output Low Voltage	58 to 60	4.0	–	 0.4	V V	
V_{TIH} V_{TIL}	Digital Input High Voltage Digital Input Low Voltage	4, 5	2.4	–	 0.8	V V	
V_{TUNOUT}	Synthesizer Output Voltage (AMTUNOUT, FMTUNOUT)	22, 24	1.1	–	V_{SUP2} –1.1	V	
V_{AGNDC0}	AGNDC Open Circuit Voltage	33	2.15	2.25	2.35	V	
$R_{OUTAGND}$	AGNDC Output Resistance at 27 °C at –20 to +85 °C		 110 70	 125	 140 230	 kΩ kΩ	
dV_{BAGNDC}	Deviation of BAGNDC from AGNDC Voltage	33, 37	–20		+20	mV	
$R_{OUTBAGND}$	BAGNDC Output Resistance	37		6		Ω	f_{signal} = 1 kHz, i = 0.1 mA
dV_{DAC}	Deviation of DC Level at Audio Outputs from AGNDC Voltage	26 to 29, 33	–20		+20	mV	
$I_{OUTSYNTH}$	Synthesizer Current Source Accuracy I = 5 µA I = 50 µA I = 500 µA	22, 24	 3.3 33 330	 5 50 500	 6.5 70 740	 µA µA µA	
PSRR	Power Supply Rejection Ratio 1 kHz 20 Hz to 20 kHz	20, 21, 30, 56, 26 to 29	 50	 40		 dB dB	
dV_{TUNOUT}	Residual Noise of Synthesizer Output Voltage	24		2.2		µV	BW 22Hz to 22 kHz, i = 5 µA

1) CD-Mode, f_s = 44.1 kHz
2) unused analog inputs connected to ground

4. Starting the Processor

After power-up, the crystal oscillator has to have been started before the Reset reaches high level. An additional wait time of 0.4 ms has to be taken into account because of a DSP-internal self-test algorithm. Then the CAP 3540B can be initialized. Fig. 4–1 shows the complete start-up sequence of the typical application.

The DCO register is loaded with a zero value.

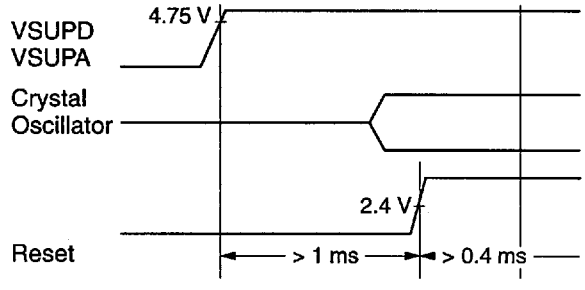


Fig. 4–1: Start-up sequence

5. Synthesizer

With the synthesizer block in the CAP 3540B, a PLL tuning system can be implemented for FM and AM receivers. The signal picked up from the mixing oscillators of the FM and AM tuners can be fed to the synthesizer block by means of highly sensitive input pins. Freely programmable dividers, operating with frequencies up to and over 100 MHz, scale the incoming signals to a reference frequency of 25 kHz. This holds true even in the case of AM, which gives AM tuning a considerable speed improvement over common designs. In order to get a tuning step size of down to 300 Hz, the reference divider is also programmable. Incoming frequencies in the range of 0.5 MHz up to more than 100 MHz can be handled, so that the designer is free to choose either a 10.7 MHz or a 450 to 460 kHz IF frequency for the AM case. The common reference frequency for AM and FM allows the implementation of a common PLL filter for the tuning output.

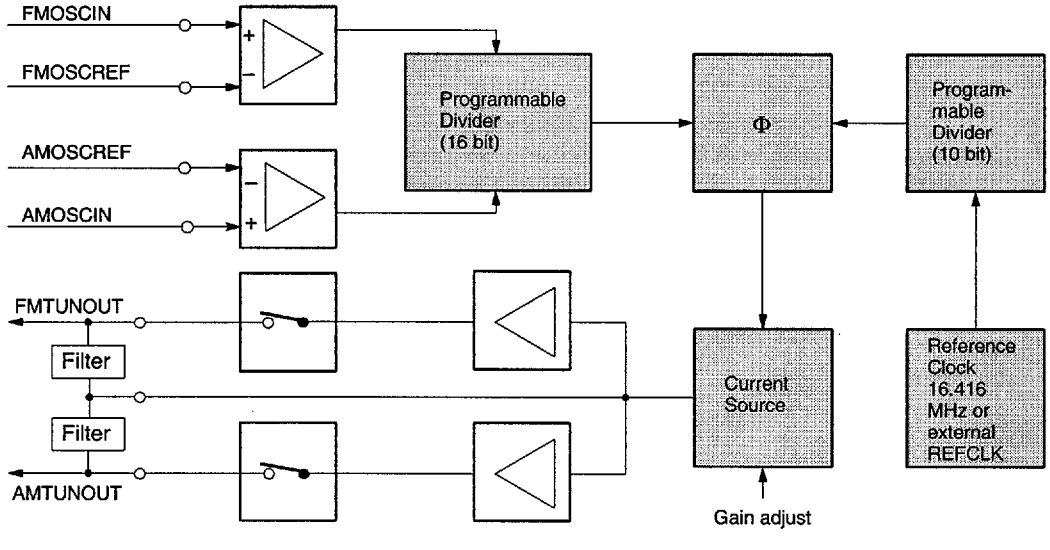


Fig. 5–1: Synthesizer block diagram

6. Application Notes

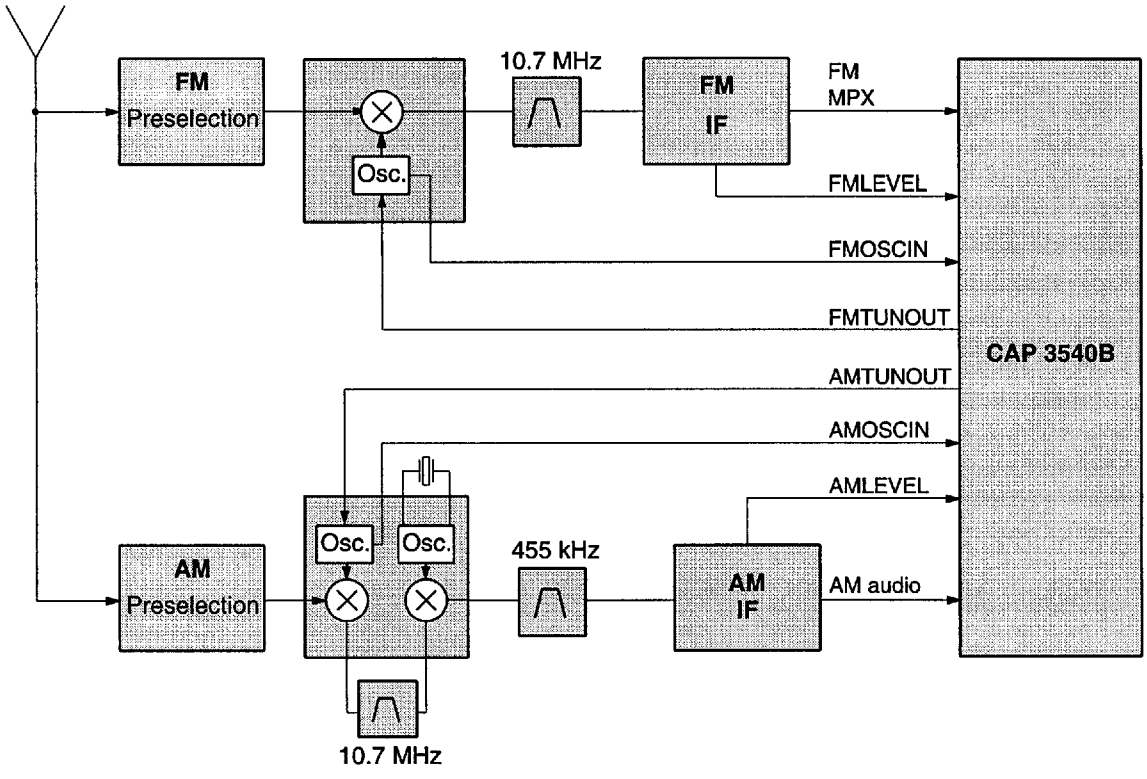


Fig. 6–1: CAP 3540B application for 10.7 MHz AM-IF in detail

7. Typical Application Circuit

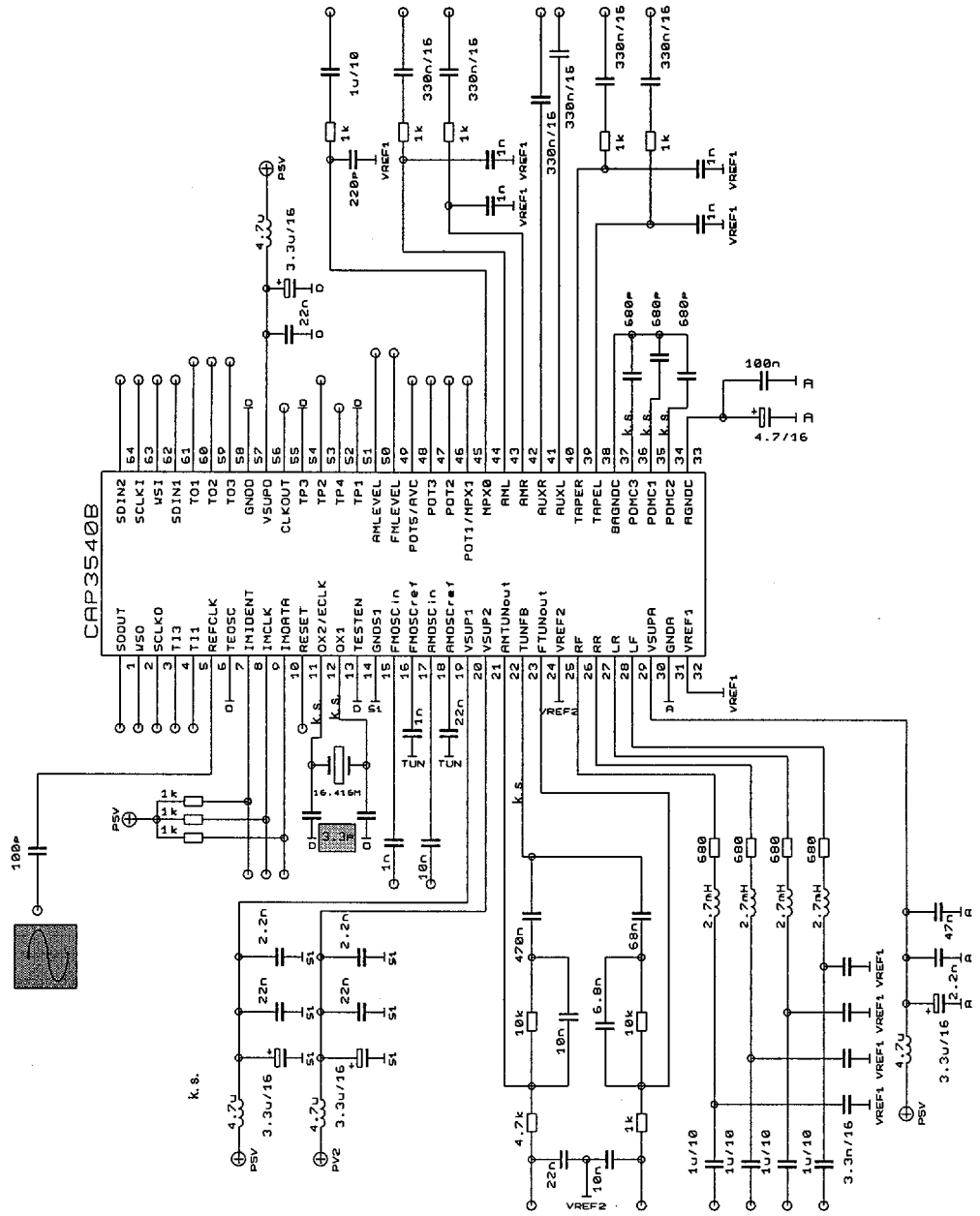


Fig. 7-1: Typical Application Circuit

3.3p These values have to be adjusted to achieve the neccessary pulling range and to define its absolute position (compensation of he parasitic board capacitors).

These ground nets are connected together to the main ground under the IC, close to the pin VREF1.

Pin VREF2 is the reference for the tuning synthesizer. It is connected to the tuner ground and has no direct connection to the main ground under the IC.

This is the ground at the tuner. It has a separate connection to the main ground under the IC.

k. s. Keep these leads as short as possible!

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