

MOS FIELD EFFECT POWER TRANSISTOR μ PA1700

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of note book computers.

FEATURES

· Low On-Resistance

 $R_{DS(on)1} = 27~m\Omega~Typ.~(V_{GS} = 10~V,~I_{D} = 3.5~A)$ $R_{DS(on)2} = 50~m\Omega~Typ.~(V_{GS} = 4~V,~I_{D} = 3.5~A)$

- Low Ciss Ciss = 850 pF Typ.
- · Built-in G-S Protection Diode
- Small and Surface Mount Package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1700G	Power SOP8

ABSOLUTE MAXIMUM RATINGS (TA = $25 \, ^{\circ}$ C)

Drain to Source Voltage	VDSS	30	V
Gate to Source Voltage	Vgds	±20	V
Drain Current (DC)	$I_{D(DC)}$	±7.0	Α
Drain Current (pulse)*	ain Current (pulse)* ID(pulse) ±28		Α
Total Power Dissipation	Рт	2.0	W
(T _A = 25 °C)**			
Channel Temperature	Тсн	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C

- * PW \leq 10 μ s, Duty Cycle \leq 1 %
- ** Mounted on ceramic substate of 1200 mm $^2 \times 0.7$ mm

PACKAGE DIMENSIONS (in millimeter) 日日日日 1,2,3 ; Source ; Gate 5,6,7,8 ; Drain 甘甘甘甘 6.0 ± 0.3 44 -0.8 0.78 Max 0.10 1.27 0.05 $0.40^{+0.10}_{-0.05}$ \oplus 0.12 M**EQUIVALENT CIRCUIT** Body Gate Diode **Gate Protection** Diode Source To keep good radiate condition, It is recommended that all pins are soldering to print board.

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

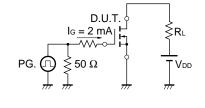


ELECTRICAL CHARACTERISTICS (TA = 25 °C)

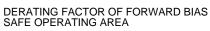
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state	RDS(on)1	Vgs = 10 V, ID = 3.5 A		20	27	mΩ
Resistance	RDS(on)2	Vgs = 4 V, ID = 3.5 A		33	50	mΩ
Gate to Source Cutoff Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0	1.6	2.0	V
Forward Transfer Admittance	yfs	V _{DS} = 10 V, I _D = 3.5 A	5.0			S
Drain Leakage Current	IDSS	V _{DS} = 30 V, V _{GS} = 0			10	μΑ
Gate to Source Leakage Current	Igss	V _{GS} = ±20 V, V _{DS} = 0			±10	μΑ
Input Capacitance	Ciss	V _{DS} = 10 V		850		pF
Output Capacitance	Coss	V _{GS} = 0		550		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		270		pF
Turn-On Delay Time	td(on)	ID = 3.5 A		20		ns
Rise Time	tr	V _{GS(on)} = 10 V		105		ns
Turn-Off Delay Time	td(off)	V _{DD} = 15 V		90		ns
Fall Time	tr	R _G = 10 Ω		60		ns
Total Gate Charge	Q _G	I _D = 7.0 A		33		nC
Gate to Source Charge	Qgs	V _{DD} = 24 V		2.4		nC
Gate to Drain Charge	Q _{GD}	V _G S = 10 V		13		nC
Body Diode Forward Voltage	V _{F(S-D)}	IF = 7.0 A, VGS = 0		0.84		V
Reverse Recovery Time	trr	IF = 7.0 A, VGS = 0		60		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		90		nC

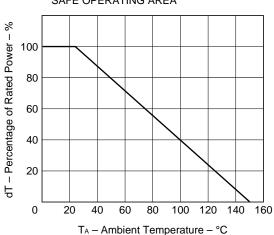
Test Circuit 1 Switching Time

Test Circuit 2 Gate Charge



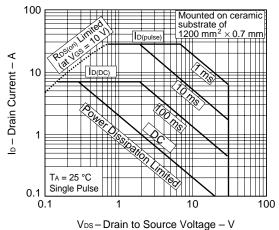
TYPICAL CHARACTERISTICS (TA = 25 °C)



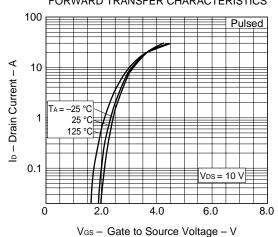


TA Ambient Temperature

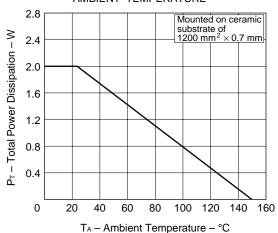
FORWARD BIAS SAFE OPERATING AREA



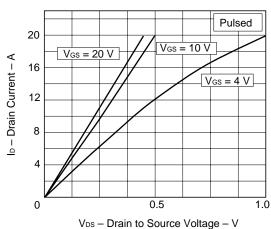
FORWARD TRANSFER CHARACTERISTICS



TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE

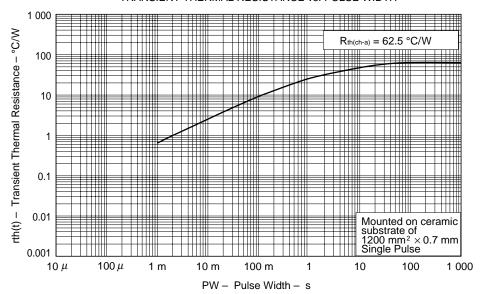


DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

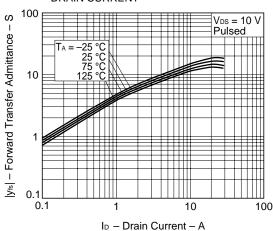




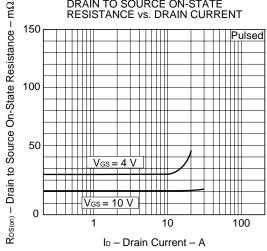
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



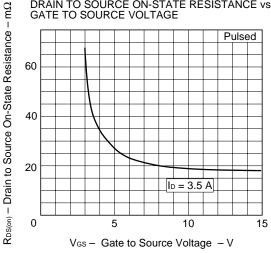




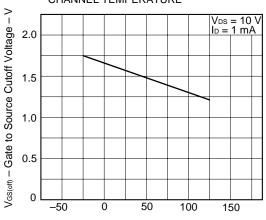
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

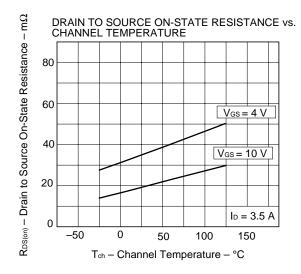


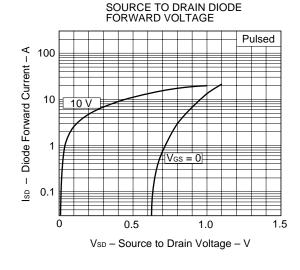
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

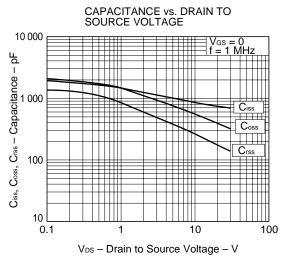


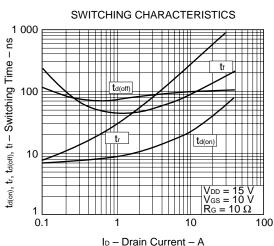
Tch - Channel Temperature - °C

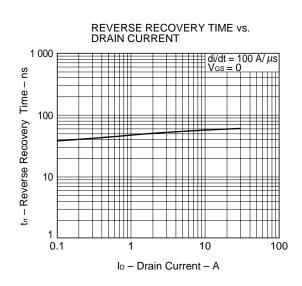


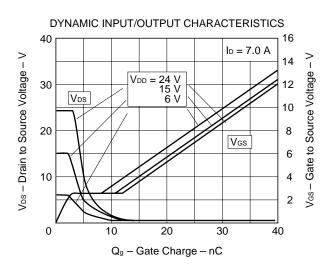














REFERENCE

Document Name	Document No.		
NEC semiconductor device reliability/quality control system	TEI-1202		
Quality grade on NEC semiconductor devices	IEI-1209		
Semiconductor device mounting technology manual	IEI-1207		
Semiconductor device package manual	IEI-1213		
Guide to quality assurance for semiconductor devices	MEI-1202		
Semiconductor selection guide	MF-1134		
Power MOS FET features and application switching power supply	TEA-1034		
Application circuits using Power MOS FET	TEA-1035		
Safe operating area of Power MOS FET	TEA-1037		

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Anti-radioactive design is not implemented in this product.

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