

Description

The μPB100470 is a very high-speed 100K interface ECL RAM with full voltage and temperature compensation. The device is organized as 4K words by 1 bit, and is designed with an open emitter output (noninverted) for low power consumption. Two fast access time versions are available: 10 ns maximum and 15 ns maximum. The μPB100470 is available in a hermetic, 300-mil, 18-pin cerdip.

Features

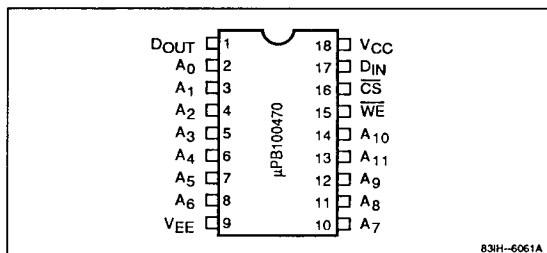
- 4,096-word x 1-bit organization
- 100K ECL interface with full voltage and temperature compensation
- Open emitter output (noninverted)
- Fast access times
- Low power consumption
- 300-mil, 18-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Package
μPB100470D-10	10 ns	18-pin cerdip
D-15	15 ns	

Pin Configuration

18-Pin Cerdip



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Pin Identification

Symbol	Function
A ₀ - A ₁₁	Address inputs
D _{IN}	Data input
D _{OUT}	Data output
CS	Chip select
WE	Write enable
V _{CC}	Ground
V _{EE}	-4.5-volt power supply

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	-7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	-30 to +0.1 mA
Storage temperature, T_{STG}	-65 to +150°C
Storage temperature under bias, T_{STG} (bias)	-55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Truth Table

CS	WE	D_{IN}	Function	Output
H	X	X	Not selected	L
L	L	L	Write 0	L
L	L	H	Write 1	L
L	H	X	Read	D_{OUT}

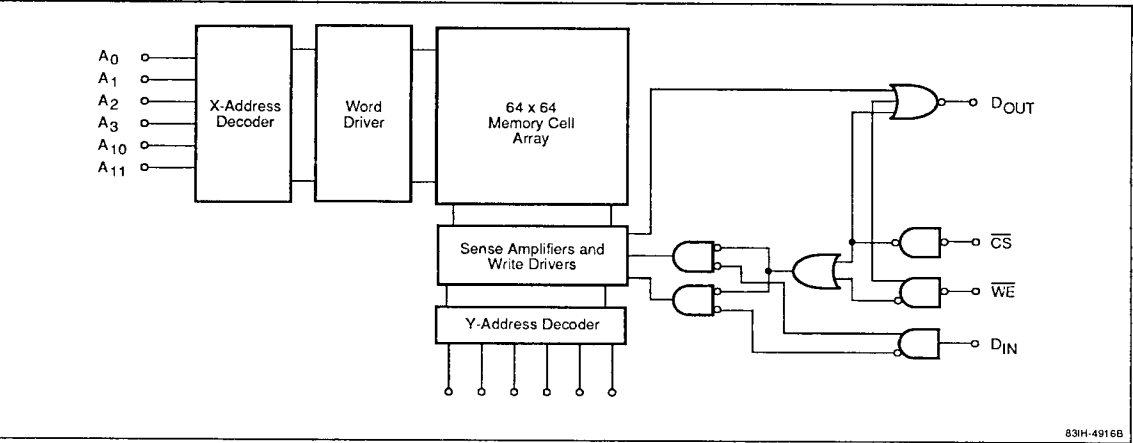
Notes:

(1) X = don't care.

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

Block Diagram



831H-4916B

DC Characteristics

$T_A = 0$ to $+85^{\circ}\text{C}$; $V_{EE} = -4.5\text{ V}$; output load = $50\ \Omega$ to -2.0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	-1025	-880	mV	$V_{IN} = V_{IH}(\text{max})$ or $V_{IL}(\text{min})$
Output voltage, low	V_{OL}	-1810	-1620	mV	
Output threshold voltage, high	V_{OHC}	-1035		mV	$V_{IN} = V_{IH}(\text{min})$ or $V_{IL}(\text{max})$
Output threshold voltage, low	V_{OLC}		-1610	mV	
Input voltage, high	V_{IH}	-1165	-880	mV	Guaranteed input voltage high for all inputs
Input voltage, low	V_{IL}	-1810	-1475	mV	Guaranteed input voltage low for all inputs
Input current, high	I_{IH}		220	μA	$V_{IN} = V_{IH}(\text{max})$
Input current, low	I_{IL}	0.5	170	μA	For CS: $V_{IN} = V_{IL}(\text{min})$
		-50		μA	For all others: $V_{IN} = V_{IL}(\text{min})$
Supply current	I_{EE}	-220		mA	All inputs and outputs open

Notes:

- (1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

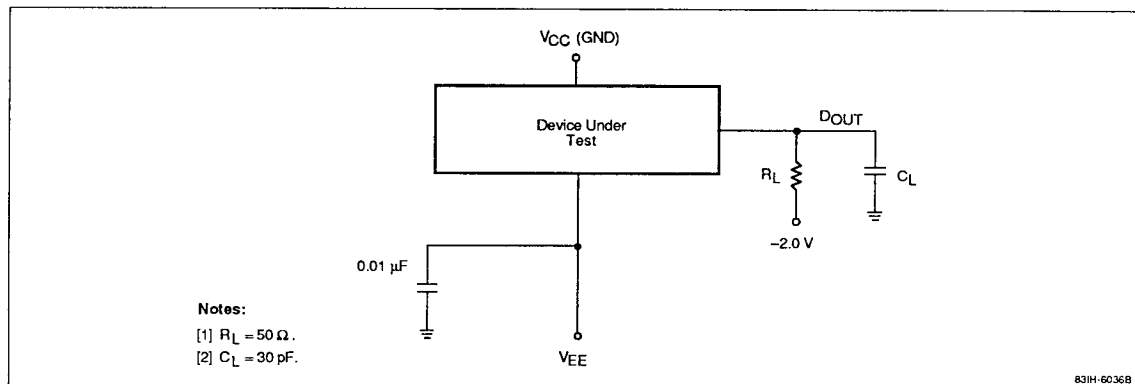
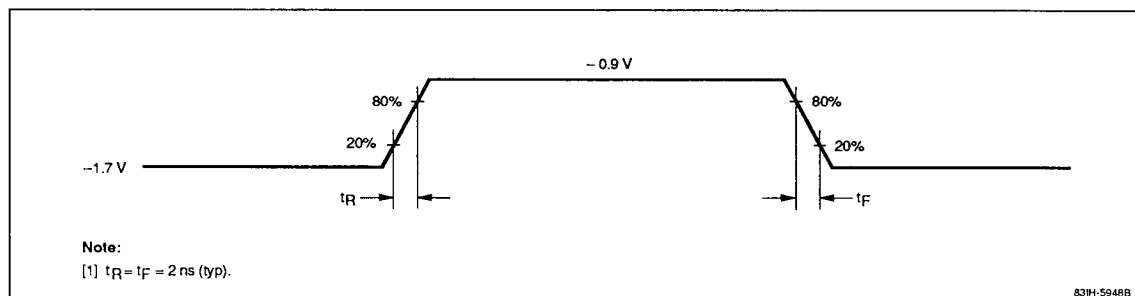
$T_A = 0$ to $+85^{\circ}\text{C}$; $V_{EE} = -4.5\text{ V} \pm 5\%$

Parameter	Symbol	μPB100470-10			μPB100470-15			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Read Operation									
Address access time	t _{AA}			10			15	ns	
Chip select access time	t _{ACS}			6			8	ns	
Chip select recovery time	t _{RCS}			6			8	ns	
Write Operation									
Write pulse width	t _W	10			15			ns	
Data setup time	t _{WSD}	2			2			ns	
Data hold time	t _{WHD}	2			2			ns	
Address setup time	t _{WSA}	3			3			ns	
Address hold time	t _{WHA}	2			2			ns	
Chip select setup time	t _{WSCS}	2			2			ns	
Chip select hold time	t _{WHCS}	2			2			ns	
Write disable time	t _{WS}			6			8	ns	
Write recovery time	t _{WR}			10			10	ns	
Output Rise and Fall Times									
Rise time	t _R		2			2		ns	
Fall time	t _F		2			2		ns	

Notes:

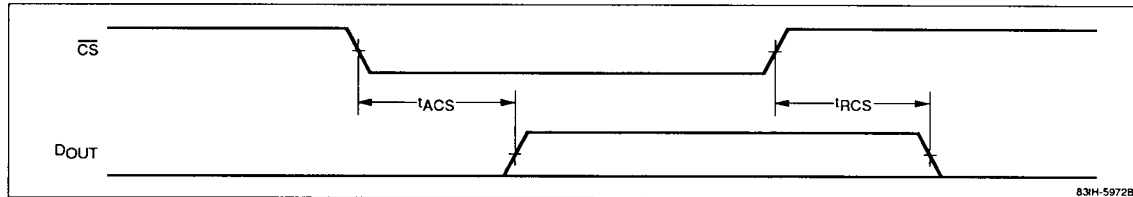
- (1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

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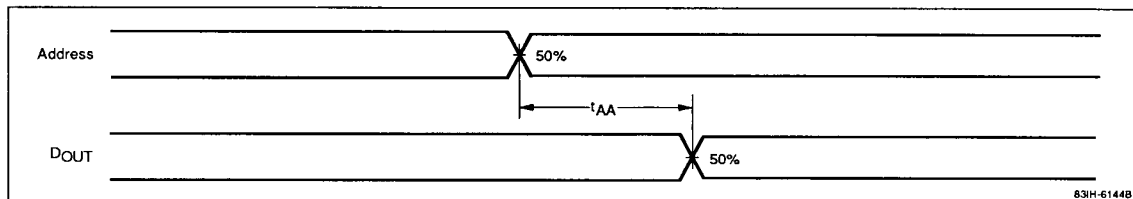
Figure 1. Loading Conditions Test Circuit**Figure 2. Input Pulse**

Timing Waveforms

Chip Select Access Cycle

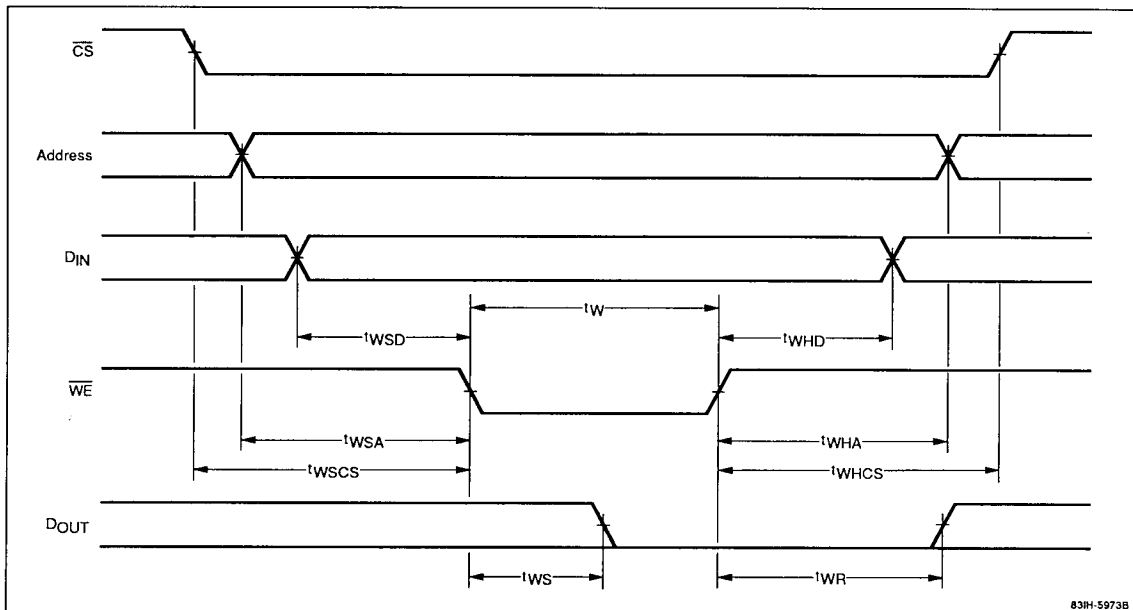


Address Access Cycle



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Write Cycle



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