NEC
NEC Electronics U.S.A. Inc.
Microcomputer Division

μPB409
μPB429
μPB409-1
μPB429-1
μPB409-2
μPB429-2

2048 WORD BY 8 BIT BIPOLAR TTL PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The μPB409 and μPB429 are high-speed, electrically programmable, fully-decoded 16384 bit TTL read only memories. On-chip address decoding, three chip enable inputs and open-collector/three-state outputs allow easy expansion of memory capacity. The μPB409 and μPB429 are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

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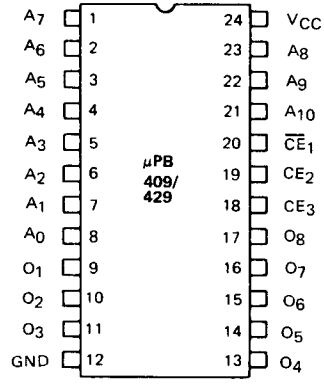
FEATURES

- 2048 WORDS x 8 BITS Organization (Fully Decoded)
- TTL Interface
- Fast Read Access Time :50 ns MAX
- Medium Power Consumption :500 mW TYP
- Three Chip Enable Inputs for Memory Expansion
- Open-Collector Outputs (μPB409)
- Three-State Outputs (μPB429)
- Ceramic 24-Lead Dual In-Line Package (μPB409D, μPB429D)
- Plastic 24-Lead Dual In-Line Package (μPB409C, μPB429C)
- Fast Programming Time :200 μs/bit TYP
- Replaceable with :82S190/191
  HM76160/76161, 3636
  and Equivalent Type Devices

PIN CONFIGURATION



PIN NAMES

A_0-A_{10}	Address Inputs
CE_1-CE_3	Chip Enable Inputs
O_1-O_8	Data Outputs

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . -0.5 to +7.0V
Input Voltage . . . . . -0.5 to +5.5V
Output Voltage . . . . . -0.5 to +5.5V
Output Current . . . . . 50 mA
Operating Temperature . . . . . -25°C to +75°C
Storage Temperature
Ceramic Package . . . . . -65°C to +150°C
Plastic Package . . . . . -55°C to +125°C

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to 75°C, V_{CC} = 4.5 to 5.5V

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.85	V	
Input High Current	I_{IH}			40	μA	V_I=5.5V, V_{CC}=5.5V
Input Low Current	$-I_{IL}$			0.25	mA	V_I=0.4V, V_{CC}=5.5V
Output Low Voltage	V_{OL}			0.45	V	I_O=16 mA, V_{CC}=4.5V
Output Leakage Current	I_{OFF1}			40	μA	V_O=5.5V, V_{CC}=5.5V
Output Leakage Current	$-I_{OFF2}$			40	μA	V_O=0.4V, V_{CC}=5.5V
Input Clamp Voltage	$-V_{IC}$			1.3	V	I_I=-18 mA, V_{CC}=4.5V
Power Supply Current	I_{CC}		100	160	mA	All inputs Grounded, V_{CC}=5.5V
Output High Voltage*	V_{OH}	2.4			V	I_O=-2.4 mA, V_{CC}=4.5V
Output Short Circuit Current*	$-I_{SC}$	20		70	mA	V_O=0V

*Note: Applicable to μPB429

CAPACITANCE

T_a = 25°C, f = 1 MHz, V_{CC} = 5V, V_{IN} = 2.5V

CHARACTERISTICS	SYMBOL	MIN	MAX	UNIT
Input Capacitance	C_{IN}		8	pF
Output Capacitance	C_{OUT}		10	pF

AC CHARACTERISTICS

T_a = 0°C to 75°C, V_{CC} = 4.5 to 5.5V ①②③④

CHARACTERISTIC	SYMBOL	μPB409-2, μPB429-2		μPB409-1, μPB429-1		μPB409, μPB429		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Address Access Time	t_{AA}		50		60		70	ns
Chip Enable Access Time	t_{ACE}		30		40		50	ns
Chip Enable Disable Time	t_{DCE}		30		40		50	ns

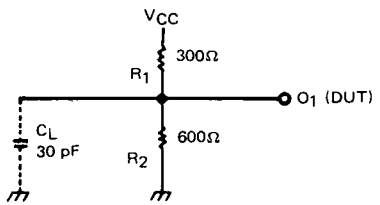


FIGURE 1

NOTES: ① Output Load: See Fig. 1.
② Input Waveform: 0.0V for low level and 3.0V for high level, less than 10ns for both rise and fall times.
③ Measurement References: 1.5V for both inputs and outputs.
④ C_L in Fig. 1 includes jig and probe stray capacitances.

OPERATION

You can program only when the outputs are disabled by any one of the chip enable inputs. This insures that the output will not be damaged when you apply programming voltages.

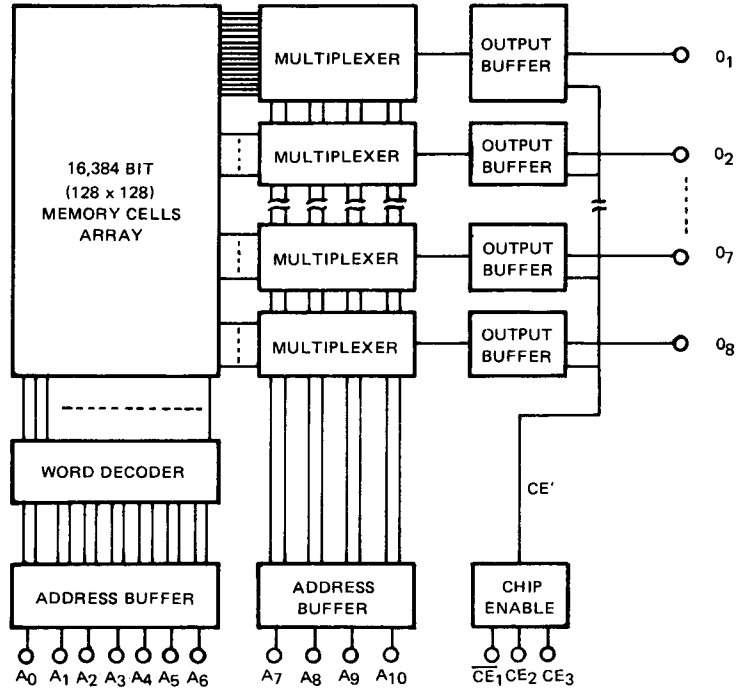
Programming

You can permanently program a logic one into a selected bit location by using special equipment (programmer). First, disable the chip as described above. Second, apply a train of high-current programming pulses to the desired output. Apply an additional pulse train after the sensed voltage indicates that the selected bit is in the logic one state. Then, stop the pulse train.

Reading

To read the memory, enable the chip (i.e., $CE_1 = 0, CE_2 = CE_3 = 1$). The outputs then correspond to the data programmed into the selected words. When the chip is disabled, all the outputs will be in a high impedance (floating) state.

LOGIC DIAGRAM



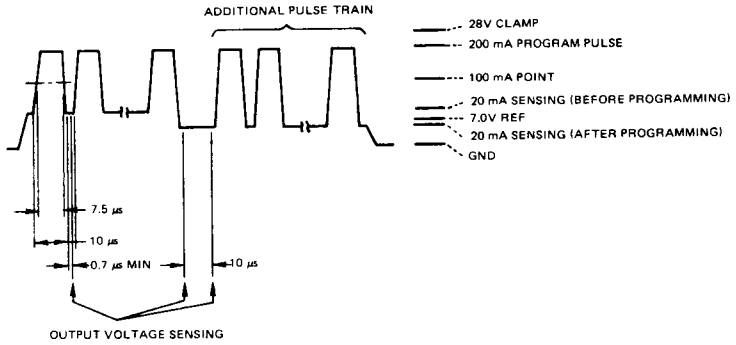
PROGRAMMING SPECIFICATION

It is imperative that this specification be rigorously observed in order to correctly program the μPB409 and μPB429. NEC will not accept responsibility for any device found to be defective if it was not programmed according to this specification.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ± 5	°C	
Programming Pulse			
Amplitude	200 ± 5%	mA	
Clamp Voltage	28 + 0% – 2%	V	
Ramp Rate (Both in Rise and in Fall)	70 MAX	V/μs	
Pulse Width	7.5 ± 5%	μs	15V point/150Ω load
Duty Cycle	70% MIN		
Sense Current			
Amplitude	20 ± 0.5	mA	
Clamp Voltage	28 + 0% – 2%	V	
Ramp Rate	70 MAX	V/μs	15V point/150Ω load
Sense Current Interruption before and after address change	10 MIN	μs	
Programming V_{CC}	5.0 + 5% – 0%	V	
Maximum Sensed Voltage* for programmed "1"	7.0 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN	μs	

*A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse pass the limit. When this condition has been met, four additional pulses are applied, then the sense current is terminated.

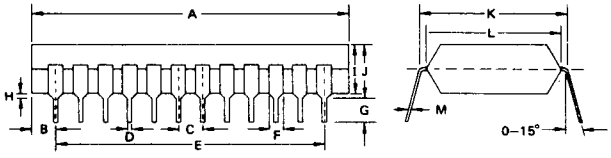
TYPICAL OUTPUT VOLTAGE WAVEFORM



PROGRAMMING EQUIPMENT

APPROVED MANUFACTURER	MODEL NO.	PERSONALITY MODULE	SOCKET ADAPTORS
Data I/O Issaquah, WA	5, 7, 9, 17, 19	919-1555	715-1628-2
Minato Electronics Tokyo, Japan	1802	μPB4XX	SA-24-/B429
Takeda Riken Tokyo, Japan	TR-429 B	PZ 3834	WZ3256-123
Toyo Data Tokyo, Japan	PECKER-O	UN-711F	AD-7118

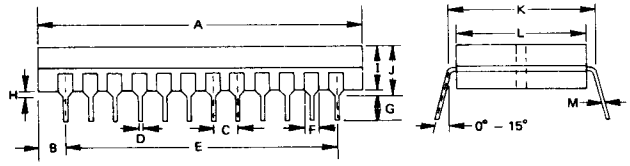
PACKAGE OUTLINE
μPB409C/429C



(Plastic)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

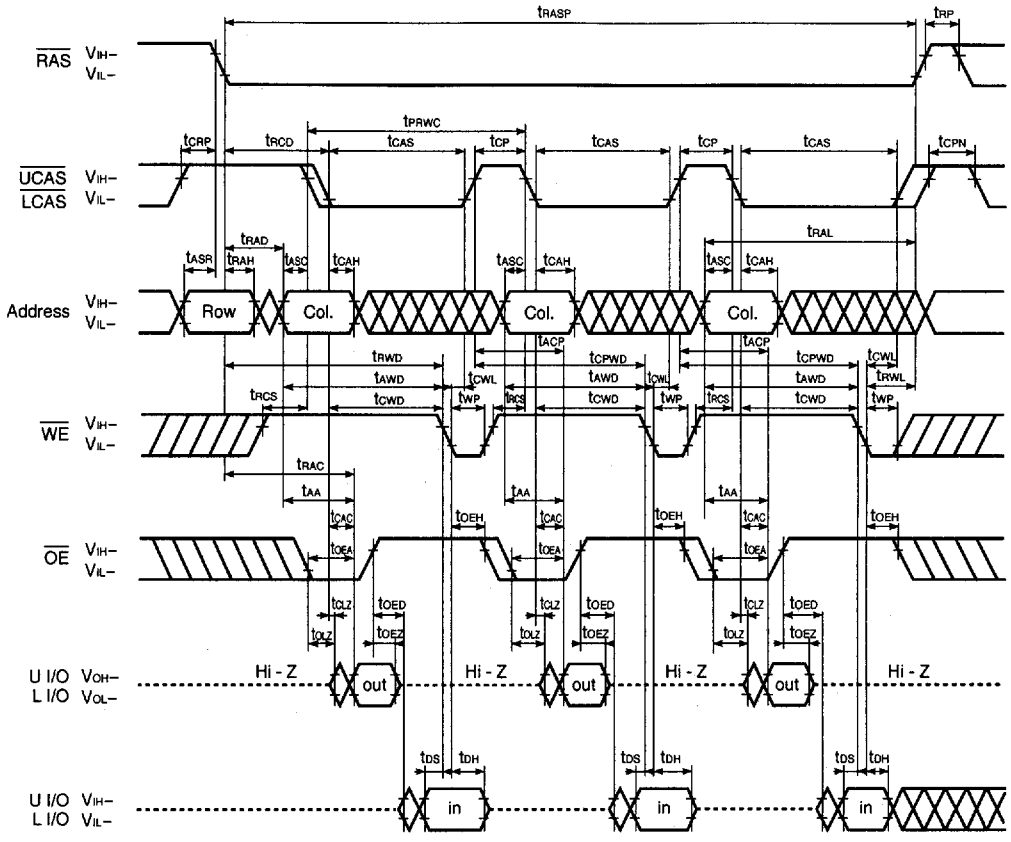
μPB409D/429D



(Cerdip)

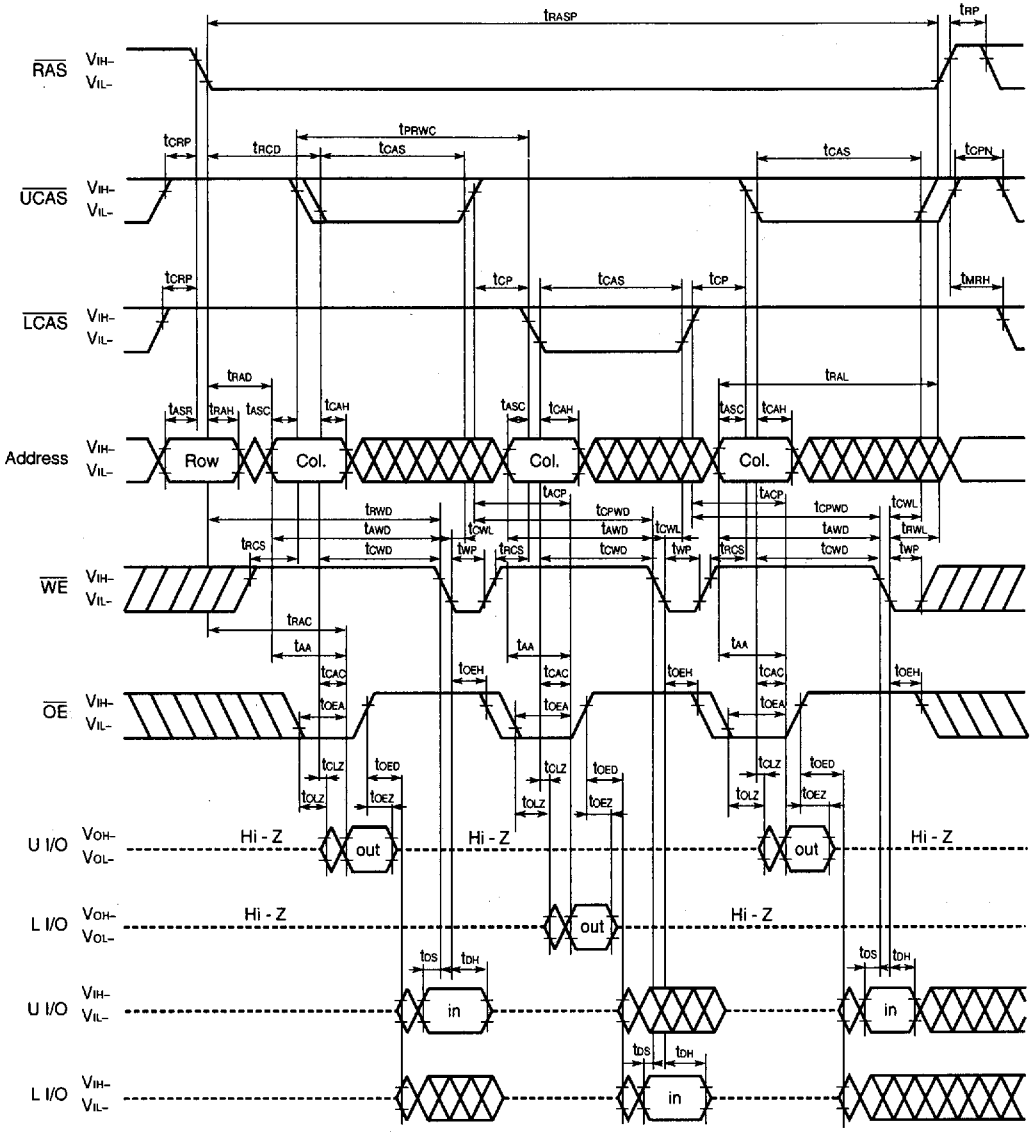
ITEM	MILLIMETERS	INCHES
A	33.5 MAX	1.32 MAX
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.2 MAX
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

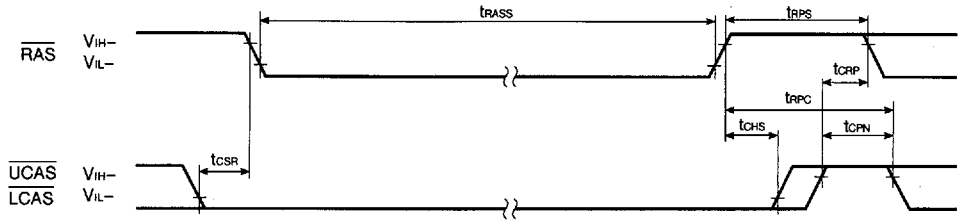
Fast Page Mode Byte Read Modify Write Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S18160)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

μPD42S18160: 1,024 times within a 16 ms interval

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

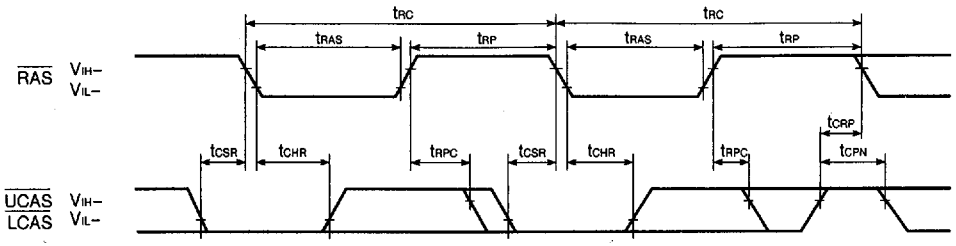
μPD42S18160: 1,024 times within a 16 ms interval

(3) If $t_{RASS\ (MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles as follows should be met.

μPD42S18160: 1,024 times within a 128 ms interval

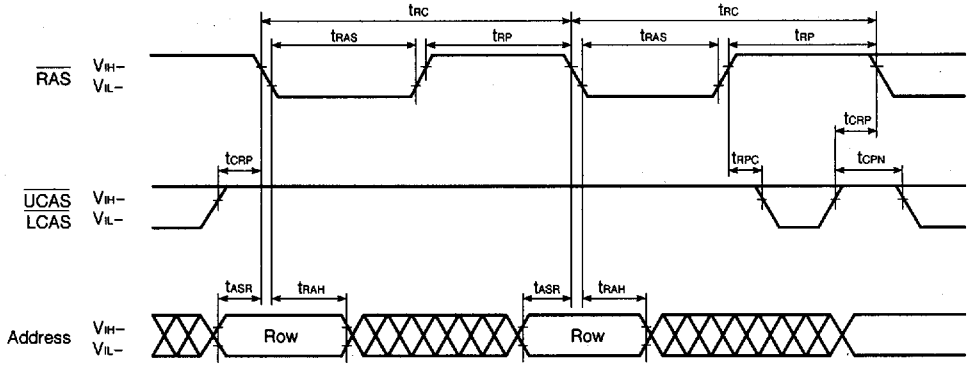
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle



Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)