

## Description

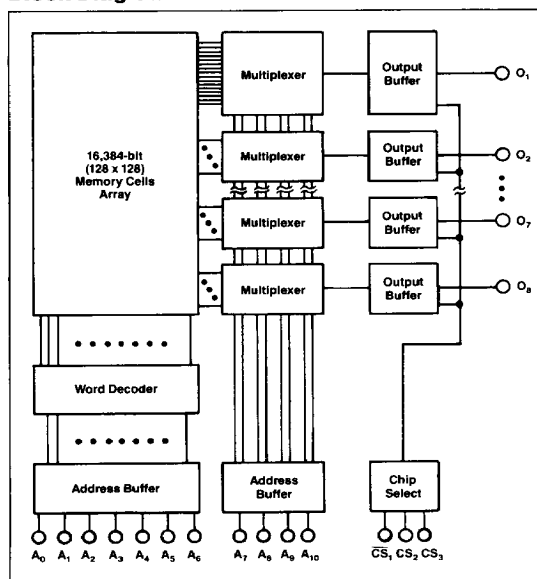
The μPB429 is a high-speed, electrically programmable, fully decoded 16384-bit TTL read-only memory. On-chip address decoding, three chip-select inputs and three-state outputs allow easy expansion of memory capacity. The μPB429 is fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

## Features

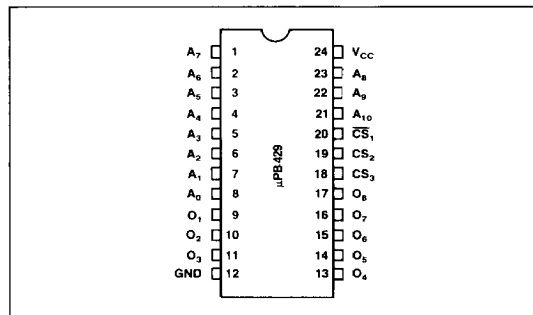
- ☐ A.I.M. (Avalanche Induced Migration), Shorted-junction technology
- ☐  $\pm 10\%$   $V_{CC}$  Operation
- ☐ Three Chip Select inputs for memory expansion
- ☐ Three-state outputs (μPB429)
- ☐ Cerdip and plastic 24-lead dual in-line packages
- ☐ Fast programming time: 10 sec. max for all 16K bits
- ☐ Replaces: 82S191, HM76161, 3636 and equivalent devices
- ☐ 4 performance ranges:

Device	Address Access Time	Power Supply
μPB429	70ns	160mA
μPB429-1	60ns	160mA
μPB429-2	50ns	160mA
μPB429-3	45ns	160mA

## Block Diagram



## Pin Configuration



## Pin Identification

$A_0$ - $A_{10}$	Address Inputs
$O_1$ - $O_8$	Data Outputs
$\overline{CS}_1$ , $CS_2$ , $CS_3$	Chip Selects
$V_{CC}$	Power (+ 5V)
GND	Ground

## Operation

### Programming

A logic one can be permanently programmed into a selected bit location by using a programmer. First, the desired word is selected by the eleven address inputs in TTL levels. Disenable the memory by proper application of logic levels on the chip selects. Secondly, a train of high-current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then stopped.

### Reading

To read the memory, enable the device (i.e.,  $\overline{CS}_1 = 0$ ,  $CS_2 = CS_3 = 1$ ). The outputs then correspond to the data programmed in the selected words. When the chip is deselected, all the outputs will be floating.

### Absolute Maximum Ratings\*

Operating Temperature	-25°C to +75°C
Storage Temperature	-65°C to +150°C
All Output Voltages	-0.5 to +5.5 Volts
All Input Voltages	-0.5 to +5.5 Volts
Supply Voltage $V_{CC}$	-0.5 to +7.0 Volts
Output Currents	50 mA

\*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Capacitance

$T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ ,  $V_{CC} = 5.0\text{V}$ ,  $V_{IN} = 2.5\text{V}$

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance	$C_{IN}$			8	pF
Output Capacitance	$C_{OUT}$			10	pF

### DC Characteristics

$T_A = 0^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{CC} = 4.5\text{V}$  to  $5.5\text{V}$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
Input High Voltage	$V_{IH}$	2.0			V	
Input Low Voltage	$V_{IL}$		0.8		V	
Input High Current	$I_{IH}$		40		$\mu\text{A}$	$V_I = 5.5\text{V}, V_{CC} = 5.5\text{V}$
Input Low Current	$-I_{IL}$		0.25		$\text{mA}$	$V_I = 0.4\text{V}, V_{CC} = 5.5\text{V}$
Output Low Voltage	$V_{OL}$		0.45		V	$I_{OL} = 16\text{ mA}, V_{CC} = 4.5\text{V}$
Output Leakage Current	$I_{OFF1}$		40		$\mu\text{A}$	$V_O = 5.5\text{V}, V_{CC} = 5.5\text{V}$
Output Leakage Current	$-I_{OFF2}$		40		$\mu\text{A}$	$V_O = 0.4\text{V}, V_{CC} = 5.5\text{V}$
Input Clamp Voltage	$-V_{IC}$		1.2		V	$I_I = -18\text{mA}, V_{CC} = 4.5\text{V}$
Power Supply Current	$I_{CC}$		100	160	$\text{mA}$	All inputs Grounded, $V_{CC} = 5.5\text{V}$
Output High Voltage	$V_{OH}$	2.4			V	$I_{OH} = -2.4\text{ mA}$
Output Short Circuit Current	$-I_{SC}$	20		70	$\text{mA}$	$V_O = 0\text{V}$

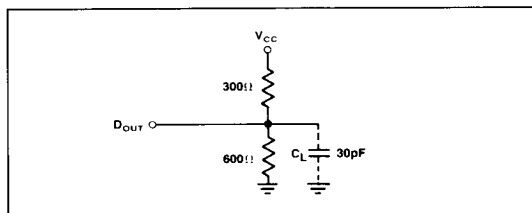
### AC Characteristics

$T_A = 0^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{CC} = 4.5\text{V}$  to  $5.5\text{V}$

Parameter	Symbol	μPB429-3		μPB429-2		μPB429-1		μPB429		Unit	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Address Access Time	t <sub>AA</sub>	45	50	60	70	ns					
Chip Select Access Time	t <sub>ACS</sub>	30	30	40	40	50	ns	①②③④			
Chip Select Disable Time	t <sub>DCS</sub>	30	30	40	40	50	ns				

- Notes: ① Output Load: See Figure 1.  
 ② Input Waveform: 0.0V for low level and 3.0V for high level, less than 10ns for both rise and fall times.  
 ③ Measurement References: 1.5V for both inputs and outputs.  
 ④  $C_L$  in Figure 1 includes jig and probe stray capacitances.

Figure 1. Loading Conditions Test Circuit



### Programming Specification

You must rigorously observe this specification in order to program the NEC Bipolar PROMS correctly. NEC will not accept responsibility for any device found to be defective if it was not programmed according to this specification.

A typical programming operation is performed by sensing, programming, and sensing again to find out if the word to be programmed has reached the desired state. Disenable the memory by proper application of logic levels in the three chip selects.

Sensing is accomplished by forcing a 20 mA current into the selected location via the output. The sense measurement ensures that the voltage required to force this 20 mA current is less than the reference voltage. If this condition is satisfied, then that bit location is in the logic one (high) state.

Programming is accomplished by forcing a 200 mA current into the selected bit via the output. The current pulse is applied for 7.5  $\mu\text{s}$  and then the location is sensed before a second programming current pulse is applied. This process continues until the selected bit is altered to the one state. You can tell that a bit is programmed when two successive sense readings, 10  $\mu\text{s}$  apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied, and the sense current is terminated.

Characteristic	Limit	Unit	Notes
Ambient Temperature	25 $\pm$ 5	$^\circ\text{C}$	
Programming pulse			
Amplitude	200 $\pm$ 5%	$\text{mA}$	
Clamp voltage	28 + 0% - 2%	V	
Ramp rate (both in rise and in fall)	70 max.	V/ $\mu\text{s}$	
Pulse width	7.5 $\pm$ 5%	$\mu\text{s}$	15V point/150 $\Omega$ load.
Duty cycle	70% min.		
Sense current			
Amplitude	20 $\pm$ 0.5	$\text{mA}$	
Clamp voltage	28 + 0% - 2%	V	
Ramp rate	70 max.	V/ $\mu\text{s}$	15V point/150 $\Omega$ load.
Sense current interruption before and after address change	10 min.	$\mu\text{s}$	
Programming $V_{CC}$	5.0 + 5% - 0%	V	
Maximum sensed voltage for programmed one	7.0 $\pm$ 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 min.	$\mu\text{s}$	

Timing diagram for the output voltage sensing circuit. The diagram shows a series of pulses. Key timing parameters are labeled: 0.7  $\mu$ s, 7.5  $\mu$ s, 10  $\mu$ s, and 10  $\mu$ s. A bracket labeled "Additional Pulse Train" covers a group of pulses. A legend on the right identifies the signals: 28V Clamp, 200 mA Program Pulse, 100 mA Point, 20 mA Sensing (Before P), 7.0V Ref., 20 mA Sensing (After P), and GND. The x-axis is labeled "Output Voltage Sensing".

Approved Manufacturer	Model No.	Personality Module	Socket Adaptors
Date I/O Isaquah, WA	5, 7, 9, 17, 19, 29A	919-1555	715-1628-2
Date I/O Isaquah, WA	Unipak II (950-0059-03C)	Family Code 72	Pinout Code 21
Minato Electronics Tokyo, Japan	1850/1870	7SP-4XXN	55A-24P74
Kontrol Redwood City, CA	MPP-805	MOD 18C	SA22