PRELIMINARY INFORMATION

Description

The μPB9201 floppy disk interface (FDI) is an LSI device that provides a wide range of functions commonly needed in a floppy disk controller design. A floppy disk controller design using the μPD765A and the μPB9201 requires only four to five chips, depending on individual requirements.

The digital phase lock loop implemented in the FDI simulates the function of an analog PLL. If higher resolution is required, the device provides for the addition of an external VCO chip. This essentially converts the digital PLL to an analog one. The external VCO is seldom required, however, due to the excellent performance of the digital PLL.

The FDI generates the write clock and processor clock for the μPD765A. The clocks are automatically switched in frequency when the 8" or 5-1/4" mode is selected. These clocks are changed synchronously so that random clock edges are not generated.

The FDI includes a precompensation circuit that allows delays of 0 ns, 125 ns, 187.5 ns, and 250 ns.

The on-chip drive select logic combined with the head load (HDL) signal eliminates the normally required selection logic. The on-chip buffers allow direct connections from $\overline{DS_0}$-$\overline{DS_3}$ and $\overline{HS_0}$-$\overline{HS_3}$ to the FDD.

The FDI provides the designer with the ability to delay the DRQ signal that normally goes from the FDC to the host DMA controller. The minimum delay is either 0.75 μs or 1.5 μs, depending on the selection of 8" or 5-1/4" mode. This allows the use of fast DMA controllers such as the μPD8237A-5.

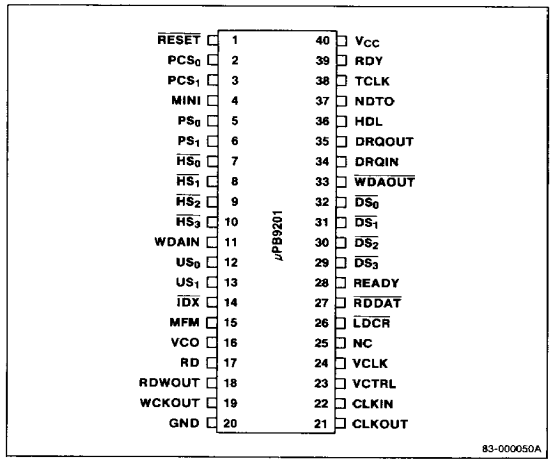
Features

- ☐ Programmable digital write precompensation
- ☐ Write clock generation for 5-1/4" and 8" drives
- ☐ Data separation
- ☐ 5-1/4" and 8" drives select
- ☐ External VCO hook-up provision (optional)
- ☐ Processor clock generation
- ☐ Internal buffers capable of sinking 24 mA
- ☐ TTL-compatible
- ☐ Drive select logic
- ☐ Head select logic
- ☐ DRQ delay
- ☐ No data time out

Ordering Information

Part Number	Package Type
μPB9201C	40-pin plastic DIP

Pin Configuration



Pin Identification

No.	Symbol	Function
1	$\overline{RESET}$	Reset input
2, 3	PCS_0, PCS_1	Precompensation select input
4	MINI	Mode select
5, 6	PS_0, PS_1	Precompensation input
7-10	$\overline{HS_0}$-$\overline{HS_3}$	Head select
11	WDAIN	Write data input
12, 13	US_0, US_1	Unit select input
14	$\overline{IDX}$	Index output
15	MFM	MFM mode input
16	VCO	VCO sync input
17	RD	Read data output
18	RDWOUT	Read data window output
19	WCKOUT	Write clock output
20	GND	Ground
21	CLKOUT	Clock output
22	CLKIN	Clock input
23	VCTRL	VCO control
24	VCLK	VCO clock input
25	NC	No connect
26	$\overline{LDCR}$	Load control register input
27	$\overline{RDDAT}$	Read data input
28	READY	Ready input
29-32	$\overline{DS_3}$-$\overline{DS_0}$	Drive select outputs

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Pin Identification (cont)

No.	Symbol	Function
33	$\overline{WDAOUT}$	Write data output
34	DRQIN	DMA request input
35	DRQOUT	DMA request output
36	HDL	Head load input
37	NDTO	No data time out input/output
38	TCLK	Test clock output
39	RDY	Ready output
40	V_{CC}	Power supply

Pin Functions

$\overline{RESET}$

When $\overline{RESET}$ is low, the FDI internal logic is reset. This feature is used mainly for text purposes. Normally this pin is pulled high.

$\overline{HS_0}$-$\overline{HS_3}$

These head select outputs are derived from the head load and the US_0 - US_1 signals from the μPD765A. Each of these open collector output sinks 24 mA.

PCS_0, PCS_1

These inputs select the precompensation delay according to the following table:

PCS_1	PCS_0	Delay
0	0	0 ns
0	1	125 ns
1	0	187.5 ns
1	1	250 ns

PS_0, PS_1

These are the precompensation input signals from the μPD765A.

WDAIN

Write data from the μPD765A is input at this pin. It passes through the circuitry which is controlled by PS_0, PS_1 and the FDI control register to provide various precompensation levels.

MINI

When this input is high, 5-1/4" mode is selected. When it is low, 8" mode is selected.

US_0, US_1

These are the unit select input pins. The μPD765A uses them to select up to four double-sided drives.

$\overline{IDX}$

The FDI uses this signal to generate index pulses to the μPD765A when there is no data coming from the disk drive.

MFM

This signal controls the read data window to conform to MFM (double density) or FM (single density) recording modes. It also controls the frequency of the WCKOUT signal. MFM is input from the μPD765A.

VCO

This is the VCO sync input from the μPD765A. It is used for internal control.

RD

The read data output signal is the same as the data coming from the FDD but it has been shaped and synchronized to the 16 MHz clock. RD is directly connected to the RD signal of the μPD765A.

RDWOUT

This signal is generated by the FDI PLL circuitry. It is controlled by the MFM signal from the μPD765A and by the selection of 5-1/4" or 8" mode.

WCKOUT

This write clock output signal is output to the WCK pin of the μPD765A.

CLKOUT

This signal provides the processor clock for the μPD765A and is programmable via the FDI control register for an 8 MHz or 4 MHz square wave output. The switching between 4 MHz and 8 MHz is synchronous.

CLKIN

This input signal should be a 16 MHz TTL-compatible square wave. All timing for the FDI is derived from this signal.

VCLK

If an external VCO chip is used, this pin should be connected to the output of the VCO. If an external VCO is not used, then this pin should be connected to the 16 MHz clock input.

VCTRL

This three-state signal controls the external VCO frequency. It is the equivalent of combined pump-up and pump-down signals.

TCLK

This signal is used to test different modes of the FDI. Depending upon the mode, this pin outputs a 4 MHz, 8 MHz or 16 MHz square wave. It is not used in controller design.

$\overline{\text{LDCR}}$

This input signal is level triggered. When $\overline{\text{LDCR}}$ is low, PSC_0, PSC_1, and MINI are transferred to the internal control register. When $\overline{\text{LDCR}}$ goes high, the data on pins 6-8 will remain latched. Pins 6-8 may be connected to a data bus and $\overline{\text{LDCR}}$ may be used as a strobe, or they may be driven from external latches by connecting $\overline{\text{LDCR}}$ to GND.

$\overline{\text{RDDAT}}$

This input is directly connected to the read data signal from the floppy disk interface.

READY

This input signal is connected through an inverter to the FDD. The RDY output signal is generated by this signal.

RDY

This output signal is directly connected to the RDY pin of the μPD765A. When the 8" mode is selected, the READY signals from the floppy disk drive is sent directly to the μPD765A. When the FDI is in the 5-1/4" mode, RDY is set to 1 at all times.

DRQIN

This is an input from the μPD765A. DRQIN is delayed 3 to 4 clock pulses before being output (DRQOUT). This achieves the DRQ to RD delay that is required by the μPD765A.

DRQOUT

This is the output of the delayed DRQIN signal.

$\overline{\text{WDAOUT}}$

This open collector output is directly connected to the floppy disk drive and writes data to it. $\overline{\text{WDAOUT}}$ sinks 24 mA.

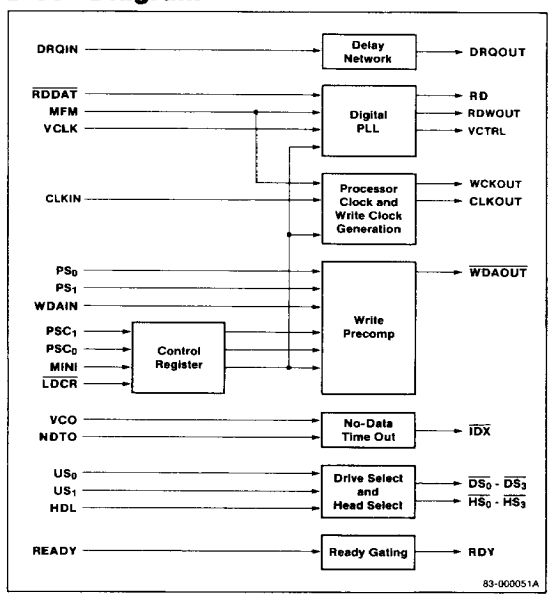
NDTO

The FDI uses this pin to generate a time out when there is no data coming from the floppy disk drive. External RC components are required for the timing.

HDL

The head load input is used in conjunction with the US_1 and US_0 signals from the μPD765A to generate the drive and head select signals.

Block Diagram



Absolute Maximum Ratings

$T_A = +25°C$

Operating temperature, T_{OPT}	0 to +70°C
Storage temperature, T_{STG}	−65 to +150°C
All output voltages, V_O	−5 to +5.5 V
All input voltages, V_I	−5 to +7 V
Power supply voltage, V_{CC}	−5 to +7 V
Power dissipation, P_D	1.5 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damange. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5 V ±10% unless otherwise specified

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Low level input voltage	V_{IL}			0.8	V	
High level input voltage	V_{IH}	2.0			V	
Input clamp voltage	V_{IC}	1.5			V	V_{CC} = 4.5 V I_{IL} = −18 mA
Low level output voltage	V_{OL}		0.3	0.5	V	V_{CC} = 4.5 V I_{OL} = 12 mA
High level output voltage	V_{OH}	2.5	3.4		V	V_{CC} = 4.5 V I_{OH} = 1 mA (1)
Short circuit output current	I_{OS}	−100		−25	mA	V_{CC} = 5.5 V V_O = 0 V
Low level input current	I_{IL}	−100			μA	V_{CC} = 5.5 V V_I = 0.4 V
High level input current	I_{IH}			20	μA	V_{CC} = 5.5 V V_I = 2.7 V
High level output current	I_{OH}			100	μA	V_{CC} = 4.5 V V_O = 4.5 V (2)
Off state output current						
Three state output	I_{OZ1}	−20			μA	V_{CC} = 5.5 V V_O = 0.4 V/2.7 V
Bidirectional	I_{OZ2}	−100		+40	μA	(VCO CNTRL pin)
V_{CC} supply current	I_{CC}		170	296	mA	T_A = +25°C

Note:

(1) Does not apply to open collector outputs.

(2) For open collector outputs only.

Capacitance

T_A = +25°C; f_C = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Clock input	C_{IN} (φ)			20	pF	All pins except those under test tied to AC GND
Input	C_{IN}			10	pF	
Output	C_{OUT}			15	pF	

AC Characteristics

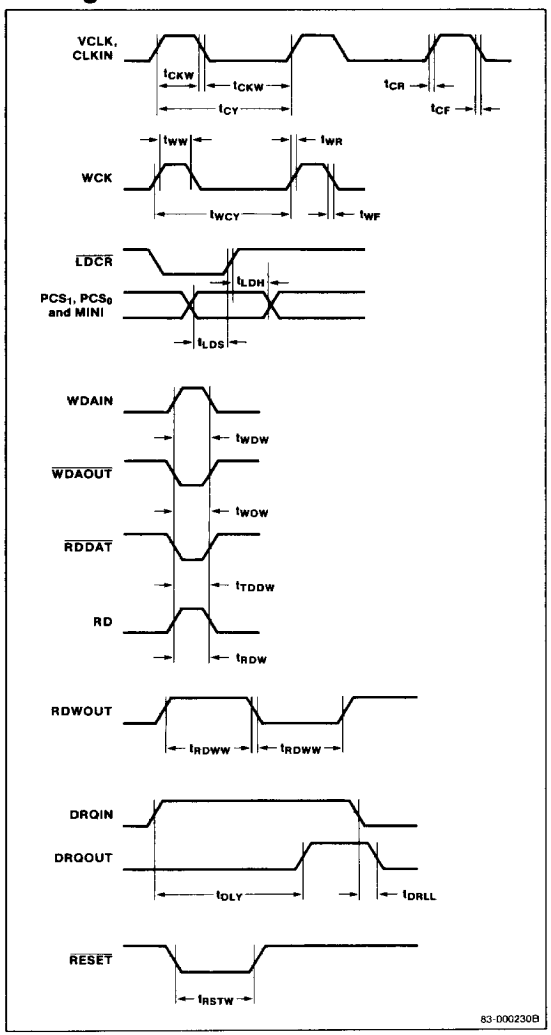
T_A = 0 to +70°C; V_{CC} = +5 V ±10% unless otherwise specified

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
CLKIN high and low width	t_{CKW}	20			ns	
CLKIN period	t_{CY}	55	62.5		ns	
CLKIN rise time	t_{CR}			10	ns	
CLKIN fall time	t_{CF}			10	ns	
WCK cycle time	t_{WCY}		1 2 2 4		μs μs μs μs	MFM, 8" FM, 8" MFM, 5-1/4" FM, 5-1/4" CLKIN = 16 MHz
WCK high width	t_{WW}		250		ns	
WCK rise time	t_{WR}			20	ns	
WCK fall time	t_{WF}			20	ns	
PCS_0, PCS_1, MINI set up time to $\overline{LDCR}$	t_{LDS}	10			ns	
PCS_0, PCS_1, MINI hold time from $\overline{LDCR}$	t_{LDH}	10			ns	
WDAIN high width	t_{WDW}	25			ns	
$\overline{WDAOUT}$ low width	t_{WOW}		$4t_{CY}$			t_{WOW} = 250 ns where CLKIN = 6 MHz
$\overline{RDDAT}$ high width	t_{RDDW}	25			ns	
RD high width	t_{RDW}		$2t_{CY}$ $4t_{CY}$			MINI = 0 MINI = 1
RDWOUT width	t_{RDWW}		1 2 2 4		μs μs μs μs	MFM, 8" FM, 8" MFM, 5-1/4" FM, 5-1/4" CLKIN = 16 MHz
DRQOUT delay time from DRQIN	t_{DLY}	0.75 1.5		1 2	μs μs	MINI = 0 MINI = 1
DRQOUT low from DRQIN low	t_{DRLL}			30	ns	
$\overline{RESET}$ low width	t_{RSTW}	250			ns	
VCLK period	t_{CY}	55	62.5		ns	
VCLK high and low width	t_{CKW}	20			ns	

Note:

The FDI is designed to run at 16 MHz, and all of the test conditions for signals generated by the FDI are at 16 MHz.

Timing Waveforms



Interfacing

Figure 1 shows all the required interconnections between the FDI and a typical FDC chip such as the μPD765A. An external 16 MHz clock input to the CLKIN pin is required. The FDI generates all the internal timing from this input clock.

An alternate method of utilizing the μPB9201 is shown in figure 2. This method minimizes the parts count and fully utilizes all of the FDI features.

The type of the drive can be selected by setting the value of the MINI pin; ie, MINI = 0: 8" and MINI = 1: 5-1/4". This can be achieved by either a jumper or a peripheral port.

The PCS_0 and PCS_1 pins are used to program the device for a desired amount of precompensation. The PS_0 and PS_1 signals from the μPD765A inform the FDI whether the bit shift is late, normal, or early.

The $\overline{LDCR}$ (load control register) pin can be used as a strobe to latch the values of MINI, PCS_1, and PCS_0 into the control register of the FDI. Whenever $\overline{LDCR}$ is low, the control register is updated. If the strobing of $\overline{LCRC}$ is not preferred, then $\overline{LDCR}$ should be connected to ground and MINI, PCS_1, and PCS_0 should be connected either to logic 1 or 0, depending upon the desired mode of operation.

The FDI uses the US_1, US_0, and HDSL signals from the μPD765A to generate the $\overline{DS_0}$-$\overline{DS_3}$ (drive select) and the $\overline{HS_0}$-$\overline{HS_3}$ (head select) signals. All these output signals are capable of sinking 24 mA and can be directly connected to the corresponding FDD signals. (This assumes that the FDD contains 220/330 termination resistors. Some drives contain 150-ohm pull-up resistors, which will require the use of a buffer external to the μPB9201.) The designer has two options available when using the head select signals. The first option is to connect all the head select signals together to the HEAD LOAD 0 signal of the FDD interface. This method generates one common "head load" signal for all drives. The second option is to add external delay circuits to each head select signal. This causes the head for the particular drive to stay loaded for the amount of specified time delay when the drive is deselected. The advantage of this method, as compared to the former one, is that it eliminates redundant head loading and unloading when copying diskettes from one to another.

Figure 1. Typical Personal Computer Application of the μPB9201

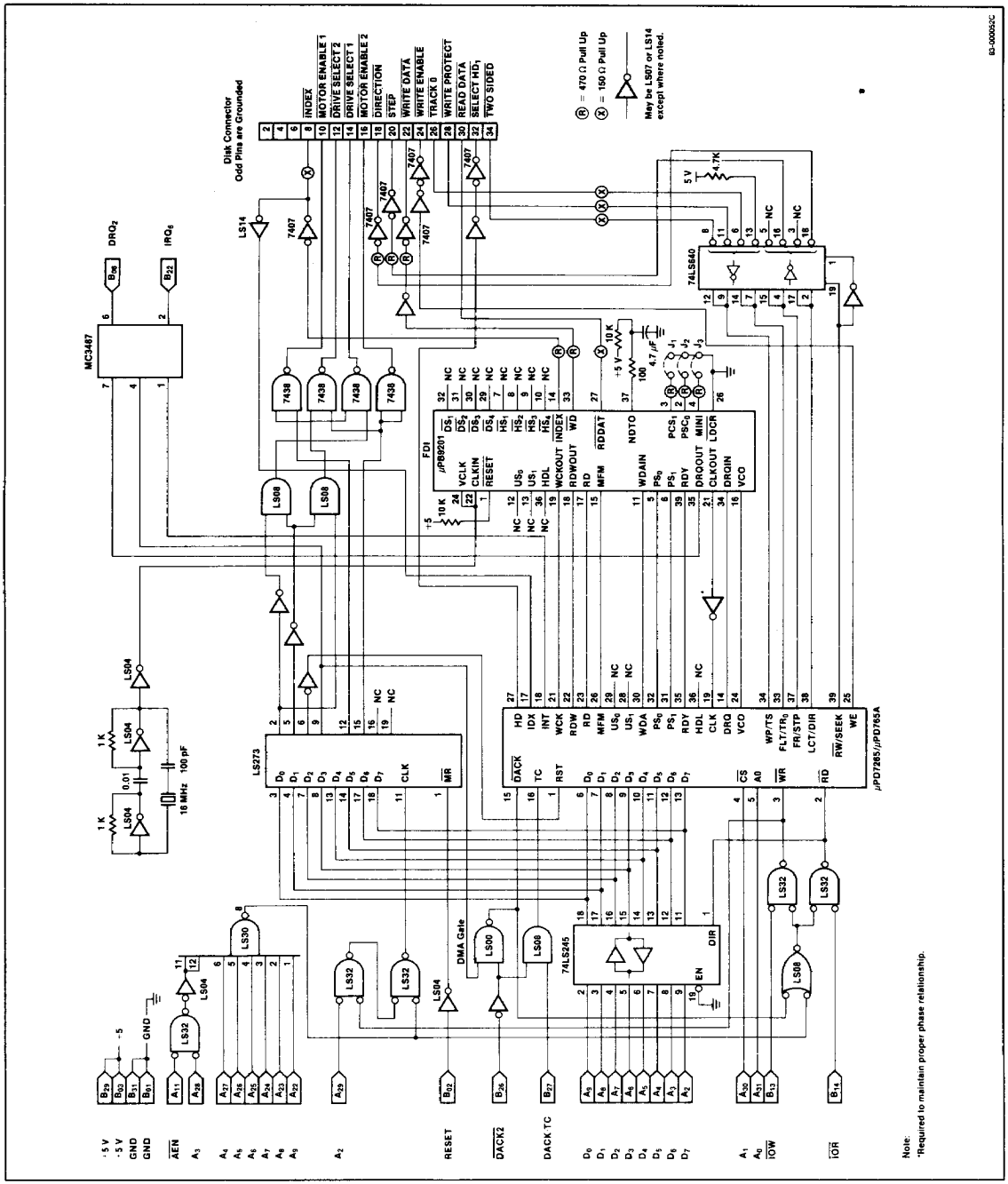
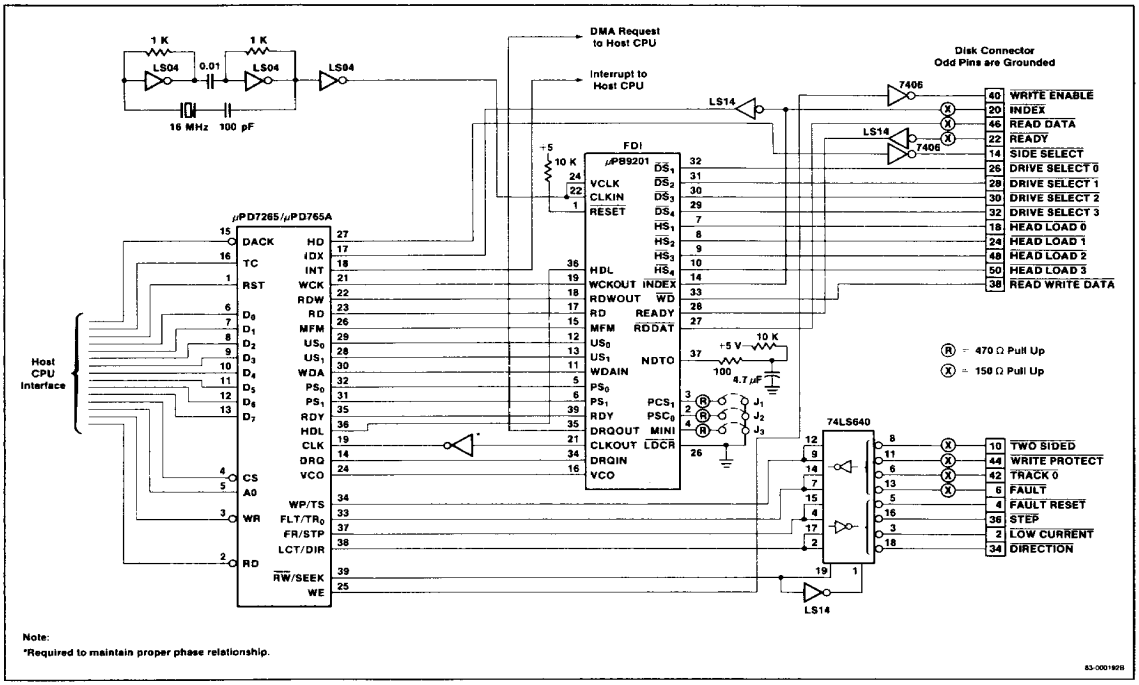


Figure 2. Typical 8" Floppy Disk Controller; Minimum Parts Count



Optionally, an external VCO chip can be added to achieve better performance. As an example, figure 3 illustrates the necessary interconnections between the 74LS624 VCO chip and the FDI. The input frequency control of the VCO is connected to the VCTRL pin of the FDI through an integrator (a simple RC circuit). The VCTRL signal is the output of the internal digital phase comparator. When there is no data bit coming in, this pin stays at approximately 2.0 volts (high impedance state). Since the frequency control pin of 74LS624 is also at 2.0 volts (adjusted by R2), the voltage across R1 will be 0 volts. As a result of this, C1 is neither charged nor discharged and the VCO will be running at its nominal frequency (16 MHz).

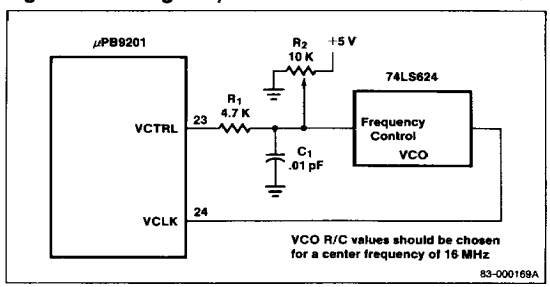
When a data bit occurs, the VCTRL pin goes first to a high state, then to a low state, and finally back to the high impedance state. The high and low states correspond to ramp-up and ramp-down respectively. The duration of ramp-up and ramp-down are determined by the position of the data bit in the read window.

If the data always arrives early, then ramp-up will have a longer period than ramp-down, causing an increase in VCO frequency. If the data arrives late, the converse is true. The integrator averages the frequency changes of the signal coming from the VCTRL pin. The values of R1 and C1 determine the time constant for the integrator. These values can be selected so that the VCO follows the slow speed variations of the disk drive. The VCLK pin should be connected to the output of the VCO when using the external VCO. If the VCO is not used, then the VCLK pin should be connected to the 16 MHz input clock.

The μPD765A requires a fairly long delay from DRQ going high to the issuance of a READ pulse to the chip. It is usually necessary to delay the DRQ signal going to the host DMA controller so that the READ pulse does not arrive early. The FDI is capable of delaying the DRQ from the μPD765A controller for approximately 1 μs (8" drive), or 2 μs for a 5-1/4" drive. In figure 1, the DRQ from the μPD765A is connected to the DRQIN pin of the FDI and the DRQOUT is connected to the host DMA controller. DRQOUT is automatically reset when DRQIN goes low.

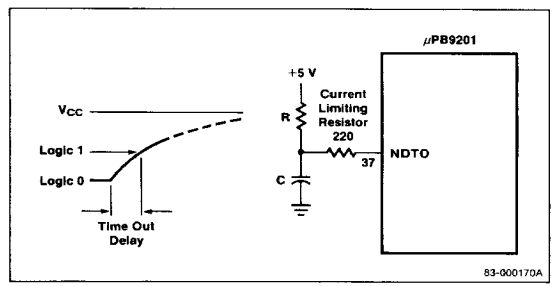
The FDI provides the necessary logic for the READY signal when the μPD765A is in mini-floppy mode. When the 8" mode is selected, the FDI passes the READY signal from the FDD interface directly to the μPD765A. When 5-1/4" mode is selected, it sets the RDY pin of the μPD765A high. If you have 5" drives that have a ready signal, it is not necessary to use this signal.

Figure 3. Using the μPB9201 with an External VCO



The FDI is capable of correcting a rare hang-up condition that occurs when there is no data coming from the disk drive to the μPD765A. When no data is coming from the FDD, the FDI waits for the time determined by the RC circuit connected to the NDTO pin. Once the time-out signal occurs, the FDI generates index pulses to the μPD765A. This causes the controller to leave the hang-up condition (see figure 4).

Figure 4. Implementing the No-Data Time Out Function



Additional Application Information

The logic diagram, shown in figure 1, illustrates a floppy disk controller as implemented on a personal computer. It is compatible with the existing controllers, but has the ability to control 8" drives and single and double density as well.