PRELIMINARY DATA SHEET

NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC2731GS

L-BNAD SILICON DOWNCONVERTER IC WITH AGC AMPLIFIER FOR DBS TUNER AND MOBILE COMMUNICATIONS

DESCRIPTION

μPC2731GS is a silicon monolithic integrated circuit designed for DBS tuner and mobile communications. This IC consists of double balanced mixer, local oscillator, IF amplifier, regulator and AGC amplifier. This means that L-band downconverter and AGC amplifier are integrated in 1 chip. This 1 chip IC is packaged in 20 pin SOP suitable for high-density surface mounting. Thus, this product contributes to produce physically-small DBS tuner and mobile communication equipments.

The μPC27×× series is manufactured using NEC's 20 GHz f_T NESAT™ III silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion and migration. Thus, this IC has excellent performance, uniformity and reliability.

FEATURES

- L-Band Operation – f_{RF} = 0.9 G to 2.0 GHz
- L-Band downconverter and AGC amplifier are integrated in 1 chip.
- Internal double balanced mixer minimizes carrier leak.
- 50 Ω impedance output.
- Supply voltage 5.0 V TYP.
- Circuit current – $I_{CCTOTAL}$ = 69 mA (Downconverter: 42 mA, AGC Amplifier: 27 mA)
- Packaged in 20 pin SOP suitable for high-density surface mounting.

ORDERING INFORMATION

PART NUMBER	PACKAGE	SUPPLYING FORM
μPC2731GS-E1	20 pin plastic SOP (300 mil)	Embossed tape 24 mm wide. Pin 1 indicates pull-out direction of tape. QTY 2.5 kp/REEL.
μPC2731GS-E2	20 pin plastic SOP (300 mil)	Embossed tape 24 mm wide. Pin 1 indicates roll-in direction of tape. QTY 2.5 kp/REEL.

* For evaluation sample order, please contact your local NEC sales office (Part number: μPC2731GS).

Caution: Electro-static sensitive device

The information in this document is subject to change without notice.

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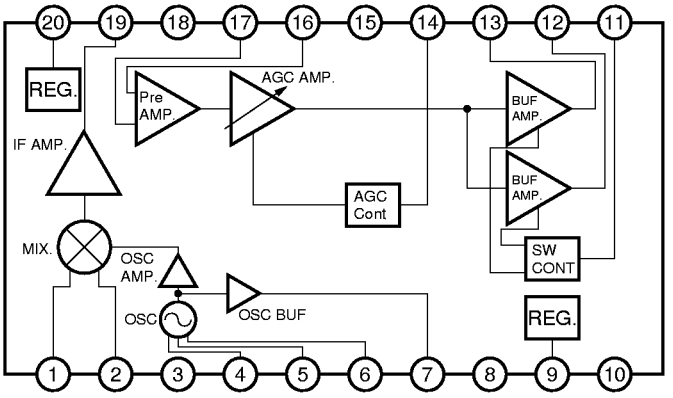
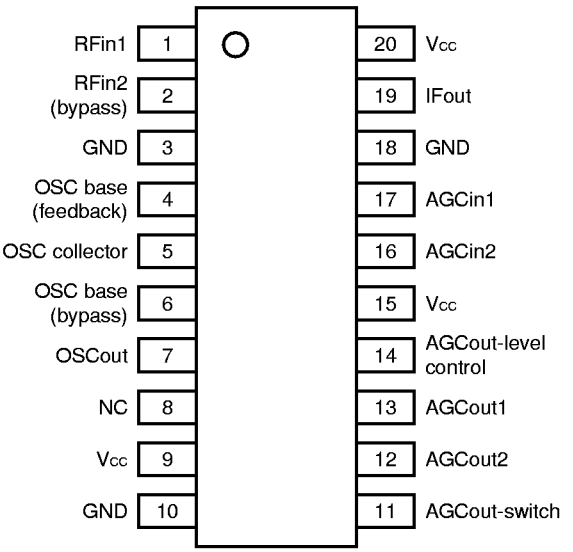
INTERNAL BLOCK DIAGRAM



PIN CONNECTIONS (Top View)

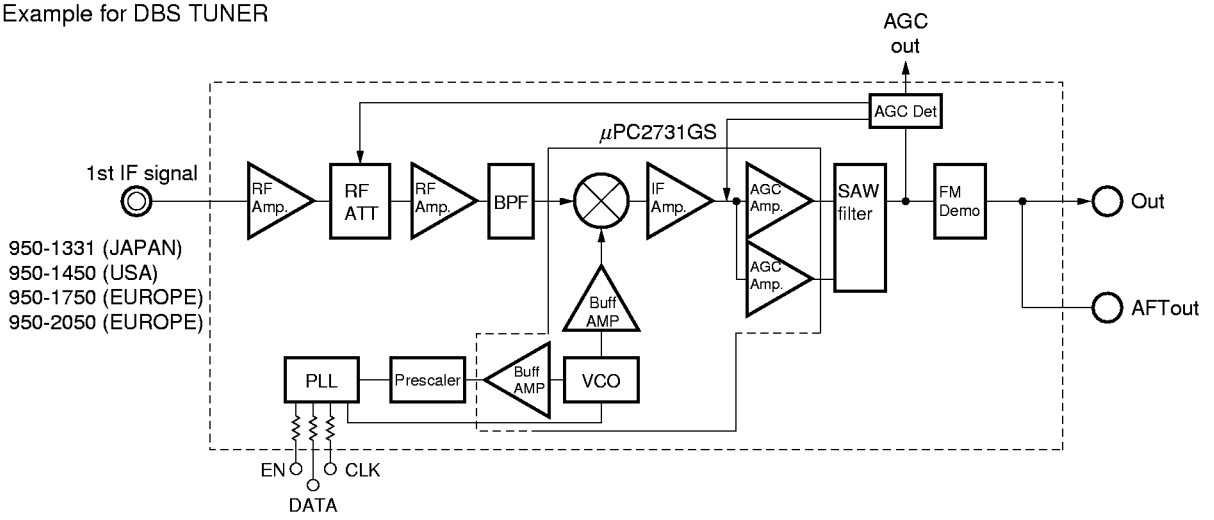


SELECTOR GUIDE (T_A = +25 °C, V_{CC} = 5.0 V)

Main Feature	Device Number	f_{RF} (GHz)	CG (dB)	NF (dB)	D_{AGC} (dB)	$G_{AGC\ MAX.}$ (dB)	Package
50 Ω impedance output	μPC2721GR	0.9 - 2.0	21	11	–	–	8 pin SOP
High impedance output	μPC2722GR	0.9 - 2.0	18	11	–	–	8 pin SOP
• Equipped with AGC amplifier • 50 Ω impedance output	μPC2731GS	0.9 - 2.0	14	14	60	25	20 pin SOP

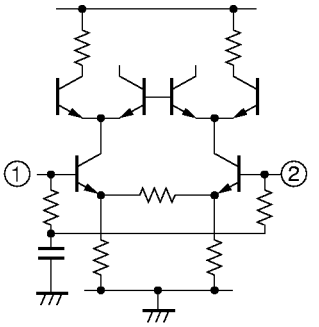
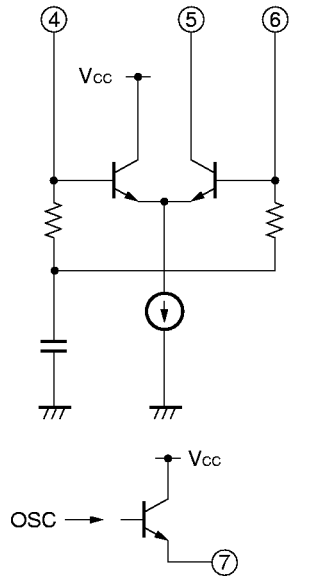
TYPICAL SYSTEM APPLICATION

Example for DBS TUNER



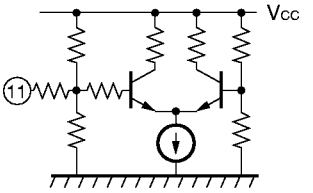
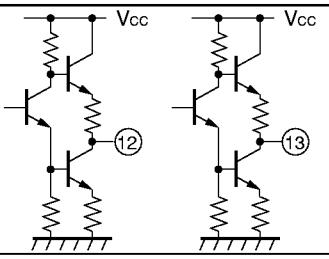
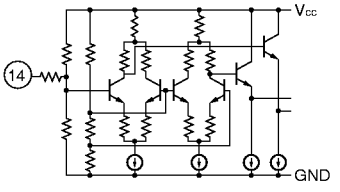
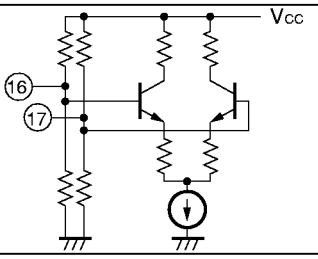
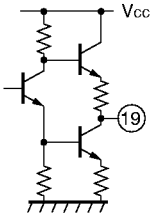
To know the detail in associated products, please refer to their latest data sheet.

PIN EXPLANATIONS

Pin No.	Symbol	Pin Voltage (V)	Explanation	Equivalent Circuit
1	RF input 1	2.4	① and ② pins are inputs for mixer designed as double balanced type. Either pin can be assigned for input and another for ground.	
2	RF input 2 (bypass)	2.4		
3	GND	0*	Must be connected to the system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. (Track length should be kept as short as possible.)	———
4	OSC base (feedback)	2.9	Internal oscillator consist in balance amplifier. ④ and ⑤ pins should be externally equipped with tank resonater circuit in or-der to oscillate with feedback loop. ⑥ pin should be grounded through coupling capacitor (e.g. 0.5 pF). ⑤ pin is defined as open collector. This pin should be coupled through resistor or chock coil in order to adjust Q and be supplied voltage to. In case of undesired oscillation, adjust its Q lower to stabilize the operation.	
5	OSC collector	5.0		
6	OSC base (bypass)	2.9		
7	OSC OUTPUT	3.7	Oscillator output pin. Must be connected PLL synthesizer IC's input pin.	
8	NC	–	Non connection pin.	———
9	V_{CC}	5.0 ± 0.5*	AGC amplifier's power supply pin. Operates on 5.0 ± 0.5 V bias supply. Must be connected bypass capacitor (e.g. 1 000 pF) to minimize ground impedance.	———
10	GND	0*	Must be connected to the system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. (Track length should be kept as short as possible).	———

* Externally supply voltage

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Pin Voltage (V)</th><th>Explanation</th><th>Equivalent Circuit</th></tr>
<tr><td>11</td><td>AGC out switch (SW control)</td><td>V_{SW}*
H: 5 V
L: 0 V</td><td>⑫ and ⑬ pins are outputs of AGC amplifier. These pins can be selected by V_{SW} voltage to ⑪ pin.

<table><tr><td colspan="2"></td><td>AGC out pin</td></tr><tr><td colspan="2"></td><td>out</td><td>Pin No.</td></tr><tr><td rowspan="2">V_{SW} ⑪</td><td>H: 5 V</td><td>out 1</td><td>⑬</td></tr><tr><td>L: Open or GND</td><td>out 2</td><td>⑫</td></tr></table>
Both ⑫ and ⑬ output with 50 Ω impedance constant.</td><td rowspan="2">  </td></tr>
<tr><td>12</td><td>AGC_{OUT2}</td><td>2.2</td></tr>
<tr><td>13</td><td>AGC_{OUT1}</td><td>2.2</td><td>  </td></tr>
<tr><td>14</td><td>AGC out level control</td><td>(open: 2.0)
0 to 5.0*</td><td>Auto gain control pin.
This pin's bias govern the AGC out level.</td><td>  </td></tr>
<tr><td>15</td><td>V_{CC}</td><td>5.0 ± 0.5*</td><td>Supply voltage pin for AGC amplifier.
Must be conneced bypass capacitor (e.g. 1 000 pF) to minimize ground impedance.</td><td></td></tr>
<tr><td>16</td><td>AGC in 2 (bypass)</td><td>2.0</td><td>Bypass pin of AGC amplifier input. Must be grounded through capacitor.</td><td rowspan="2">  </td></tr>
<tr><td>17</td><td>AGC in 1</td><td>2.0</td><td>Input of AGC amplifier.
Must be coupled with capacitor to cut DC. (e.g. 1 000 pF)</td></tr>
<tr><td>18</td><td>GND</td><td>0*</td><td>Ground pin of AGC amplifier.
Must be connected to the system ground with minimum inductance. Ground pattern should be formed as wide as possible. (Track length be kept as short as possible.)</td><td></td></tr>
<tr><td>19</td><td>IF_{OUT}</td><td>2.0</td><td>Output from IF amplifier of downconverter. This amplifier is designed as single-end push-pull amplifier. This pin is assigned for the emitter follower output whit 50 Ω impedance.</td><td>  </td></tr>
<tr><td>20</td><td>V_{CC}</td><td>5.0 ± 0.5*</td><td>Downconverter's power supply pin.
Operates on 5.0 ± 0.5 V.
Must be connected bypass capacitor (e.g. 1 000 pF) to minimize ground impedance.</td><td></td></tr>
</table>

* Externally supply voltage

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC}	T_A = + 25 °C	6.0	V
AGC control voltage	V_{AGC}	T_A = + 25 °C	5.5	V
SW control voltage	V_{SW}	T_A = + 25 °C	5.5	V
Power dissipation depend on package	P_D	Mounted on 50 × 50 × 1.6 mm double copper clad epoxy glass board at T_A = + 85 °C	640	mW
Operating temperature	T_{opt}		–20 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

RECOMMENDED OPERATING RANGE

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
AGC control voltage	V_{AGC}	0	–	5.0	V
SW control voltage	V_{SW}	0	–	5.0	V
Operating temperature	T_{opt}	–20	+25	+85	°C

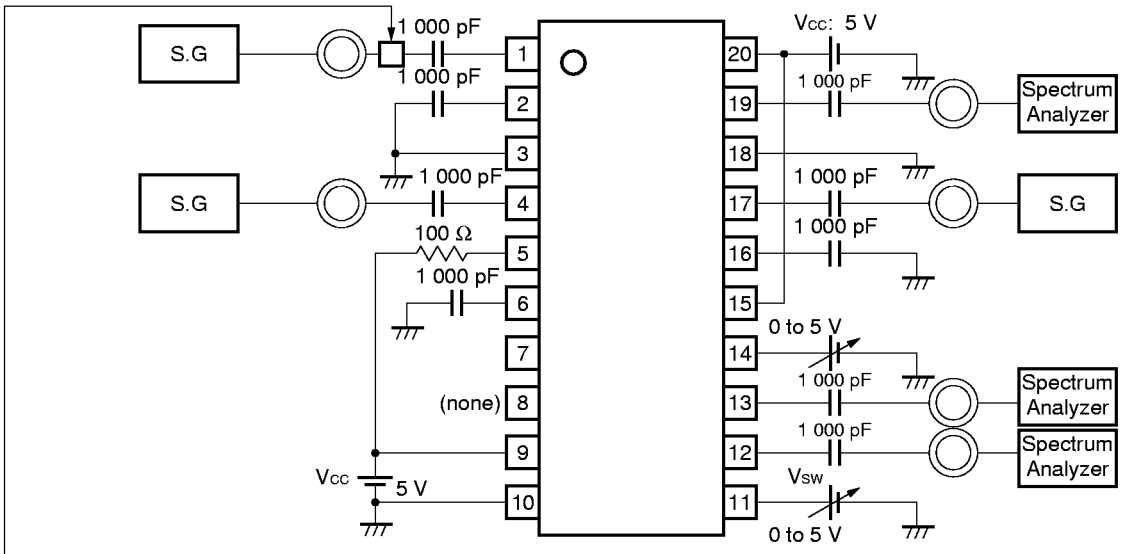
ELECTRICAL CHARACTERISTICS (T_A = + 25 °C, V_{CC} = 5.0 V, Z_L = Z_S = 50 Ω)

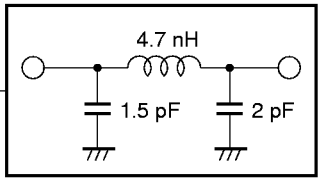
PARAMETERS		SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Circuit current	Downconverter	Icc	28.7	42.0	54.0	mA	No Input Signal
	AGC Amplifier		13.3	27	38		
	IC Total		44	69	92		
DOWNCONVERTER BLOCK: UNLESS OTHERWISE SPECIFIED, f_{IFout} = 403 MHz							
Lower RF input frequency		f_{RFl}			0.9	GHz	P_{in} = – 30 dBm
Upper RF input frequency		f_{RFu}	2.0			GHz	P_{in} = – 30 dBm
Conversion gain 1		CG1	11.5	14.5	17.5	dB	f_{RF} = 900 MHz
Conversion gain 2		CG2	10.5	13.5	16.5	dB	f_{RF} = 2 GHz
IF maximum output		P_{OSAT}	0	+7	+10	dBm	f_{RF} = 2 GHz
Noise figure 1		NF1		12	15	dB	f_{RF} = 900 MHz
Noise figure 2		NF2		17	20	dB	f_{RF} = 2 GHz
AGC AMPLIFIER BLOCK: UNLESS OTHERWISE SPECIFIED, f_{IFin} = 403 MHz							
Lower AGC input frequency		f_{IFl}			140	MHz	3 dB down CG from f_{IFin} = 403 MHz
Upper AGC input frequency		f_{IFu}	550			MHz	3 dB down CG from f_{IFin} = 403 MHz
Conversion gain 1		$G_{pMAX.}$		25		dB	P_{in} = –60 dBm
Conversion gain 2		$G_{pMIN.}$		–40		dB	P_{in} = –10 dBm
Gain Control Range		GC	45	65		dB	V_{AGC} = 0 to 5.0 V, P_{in} = –30 dBm

STANDARD CHARACTERISTIC FOR REFERENCE (T_A = +25 °C, V_{CC} = 5.0 V, Z_L = Z_S = 50 Ω)

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
DOWNCONVERTER BLOCK: UNLESS OTHERWISE SPECIFIED, f_{IFout} = 403 MHz						
3rd order intermodulation distortion	IM_3		–39		dBc	f_{RF} = 2.0 GHz, 2.04 GHz P_{in} = – 30 dBm
Local oscillator frequency	Local	1.3		2.4	GHz	Internal local oscillating
Noise figure 2'	NF2'		14		dB	Internal local oscillating f_{RF} = 2 GHz
AGC AMPLIFIER BLOCK: UNLESS OTHERWISE SPECIFIED, f_{IFin} = 403 MHz						
Input dynamic range	D_{range}		60		dBc	Range kept Po = –30 ± 1 dB
3rd order intermodulation distortion	IM_3		–50		dBc	f_{IFin} = 400 MHz, 420 MHz V_{AGC} = 0 V, Po = –20 dBm
SW control voltage	V_{SW}	4	5	6	V	AGC_{OUT1}
		0	0	1	V	AGC_{OUT2}

TEST CIRCUIT

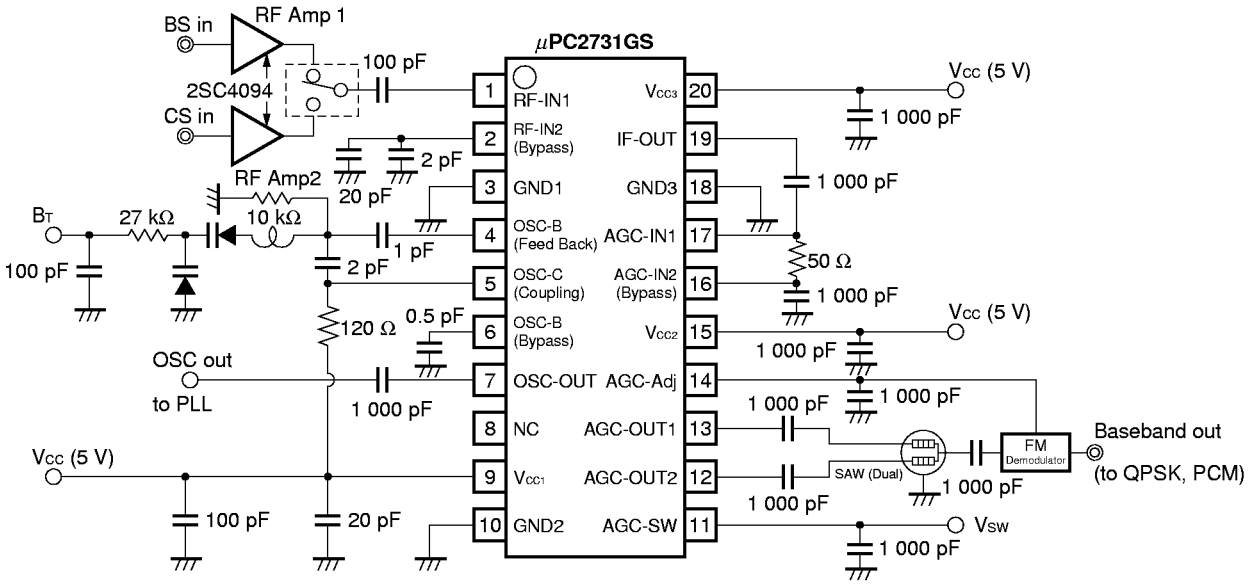




Matching circuit

		AGC out pin	
		Output	Pin No.
Vsw 11 pin	H: 5 V	output 1	13
	L: Open or 0 V	output 2	12

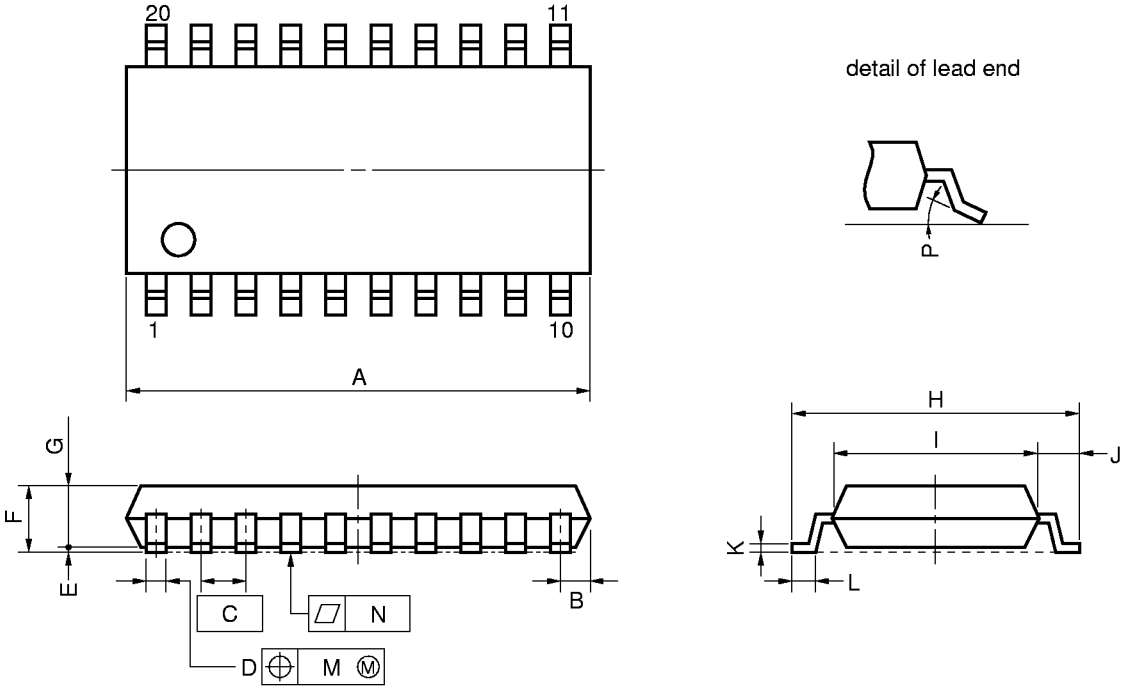
APPLICATION CIRCUIT EXAMPLE



The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

PACKAGE DIMENSIONS

20 PIN PLASTIC SOP (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.00 MAX.	0.512 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7±0.3	0.303±0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

P20GM-50-300B, C-4

NOTE ON CORRECT USE

(1) Observe precautions for handling because of electrostatic sensitive devices.
(2) Form a ground pattern as wide as possible to prevent increase in ground impedance (which can cause undesired oscillation).
(3) Keep the track length of the ground pins as short as possible.
(4) Connect a bypass capacitor (having, for example, a capacitance of 1 000 pF) to the V_{CC} pin.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering method and conditions than the recommended conditions are to be consulted with out sales representatives.

μPC2731GS

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 1, Exposure limit*: None	IR30-00-1
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 1, Exposure limit*: None	VP15-00-1
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Number of flow process: 1, Exposure limit*: None	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 3 seconds or below, Exposure limit*: None	

* Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Note Apply only a single process at once, except for "Partial heating method".
For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E)