NEC

MOS INTEGRATED CIRCUIT

μPD16633

312 OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64 GRAY SCALES)

The μPD16633 is a source driver for TFT-LCDs capable of dealing with displays with 64 gray scales. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 260,000 colors by output of 64 values γ-corrected by an internal D/A converter and 5-by-2 external power modules. Because the output dynamic range is as large as 9.8 V_{P-P}, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a maximum clock frequency of 45 MHz when driving at 3.0 V, this driver is applicable to XGA-standard TFT-LCD panels.

FEATURES

- Capable of outputting 64 values by means of 5-by-2 external power modules (10 units) and a D/A converter
- Output dynamic range 9.8 V_{P-P} min. (@V_{DD2} = 10.0 V)
- CMOS level input
- Input of 6 bits (gradation data) by 6 dots
- High-speed data transfer: $f_{max.}$ = 45 MHz (internal data transfer speed when operating at 3.0 V)
- 312 outputs
- Single bank arrangement is possible (loaded with slim TCP)

ORDERING INFORMATION

Part Number	Package
μPD16633N-xxx	TCP (TAB package)

The TCP's external shape is customized. To order your TCP's external shape, please contact a NEC salesperson.

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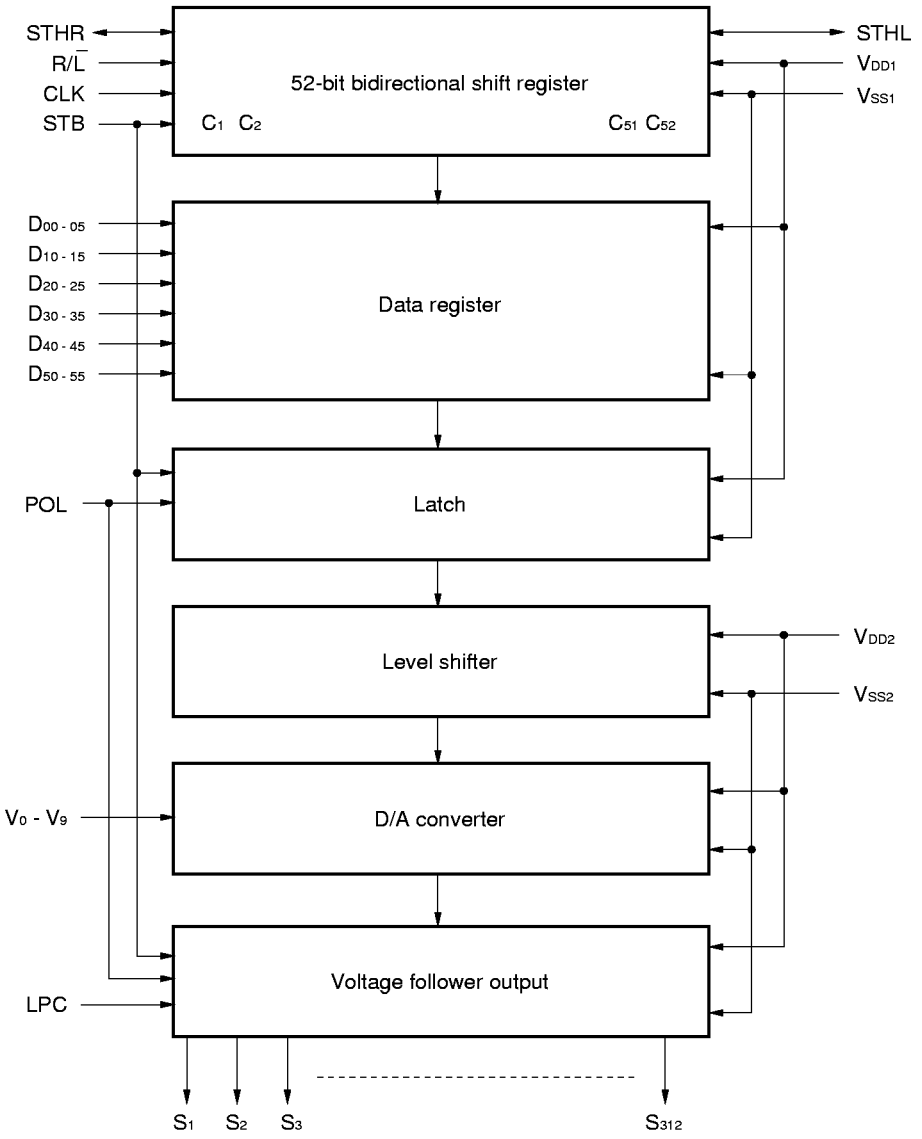
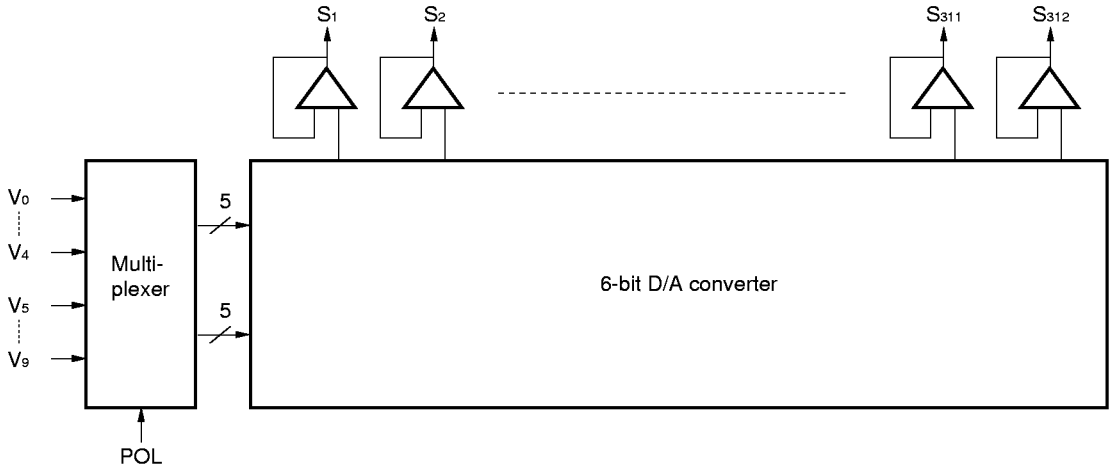
1. BLOCK DIAGRAM



2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



POL	S_{2n-1}	S_{2n}
L	V_0 to V_4	V_5 to V_9
H	V_5 to V_9	V_0 to V_4

S_{2n-1} (odd output), S_{2n} (even output) n = 1, 2, ..., 156

3. PIN FUNCTIONS

Pin Symbol	Pin Name	Description
S_1 to S_{312}	Driver output	The D/A converted 64-gray-scale analog voltage is output.
D_{01} to D_{05}	Display data input	The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6 dots (2 pixels). D_{X0}: LSB, D_{X5}: MSB
D_{10} to D_{15}		
D_{20} to D_{25}		
D_{31} to D_{35}		
D_{40} to D_{45}		
D_{50} to D_{55}		
R/$\overline{L}$	Shift direction switching input	These refer to the start pulse input/output pins when cascades are connected. The shift directions of the shift registers are as follows. R/$\overline{L}$ = H: STHR input, $S_1 \rightarrow S_{312}$, STHL output R/$\overline{L}$ = L: STHL input, $S_{312} \rightarrow S_1$, STHR output
STHR	Right shift start pulse input/output	R/$\overline{L}$ = H: Becomes the start pulse input pin. R/$\overline{L}$ = L: Becomes the start pulse output pin.
STHL	Left shift start pulse input/ output	R/$\overline{L}$ = H: Becomes the start pulse output pin. R/$\overline{L}$ = L: Becomes the start pulse input pin.
CLK	Shift clock input	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. At the rising edge of the 52th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-stage driver. The initial-stage driver's 52th clock becomes valid as the next-stage driver's start pulse is input. If 54 clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge.
STB	Latch input	The contents of the data register are transferred to the latch at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
LPC	Low power control input	The output buffer constant current source is blocked, reducing current consumption. In lower power mode (LPC = 'H': DC-level input possible), the ordinary static current consumption can be reduced by approx. 50%. The condition that low power mode can be used is that the load constant is at least 10 kΩ + 50 pF.
V_0 to V_9	γ-corrected power supplies	Input the γ-corrected power supplies from outside. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2}$
TEST	Test pin	Set it to 'OPEN'.
V_{DD1}	Logic power supply	3.3 V ± 0.3 V
V_{DD2}	Driver power supply	10 to 13.5 V
V_{SS1}	Logic ground	Grounding
V_{SS2}	Driver ground	Grounding

Cautions 1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V_0 to V_9 in that order. Reverse this sequence to shut down. (Simultaneous power application to V_{DD2} and V_0 to V_9 is possible.)

2. To stabilize the supply voltage, please be sure to insert a 0.1 μF bypass capacitor between V_{DD1}-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also advised between the γ-corrected power supply terminals (V_0, V_1, V_2, ..., V_9) and V_{SS2}.

4. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

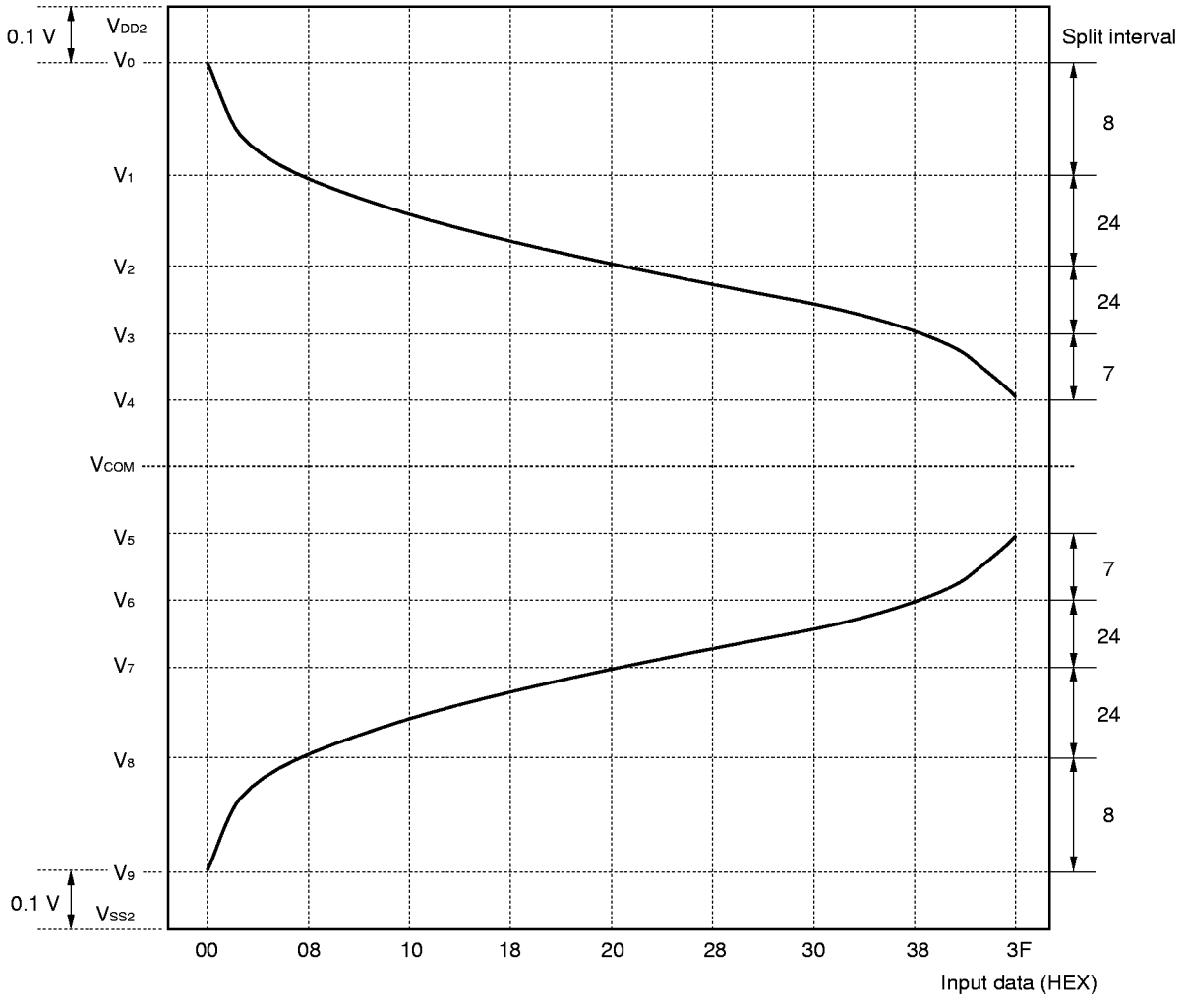
This product incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches. The ladder resistors r_0 to r_{62} are so designed that the ratios between the LCD panel's γ-corrected voltages and V_0' to V_{63}' and V_0" to V_{63}" are roughly equal; and their respective resistance values are as shown on page 9. Among the 5-by-2 γ-corrected voltages, input gray scale voltages of the same polarity with respect to the common voltage, for the respective five γ-corrected voltages of V_0 to V_4 and V_5 to V_9. If fine gray scale voltage precision is not necessary, the voltage follower circuit supplied to the γ-corrected power supplies V_1 to V_3 and V_6 to V_8 can be deleted.

Figure 1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2}, common electrode potential V_{COM}, and γ-corrected voltages V_0 to V_9 and the input data. Be sure to maintain the voltage relationships of $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2}$. Figures 2-1 and 2-2 show the relationship between the input data and the output data. Table 1 shows the resistance values of the resistor strings.

This driver IC is designed for single-sided mounting. Therefore, please do not use it for γ-corrected power supply level inversion in double-sided mounting.

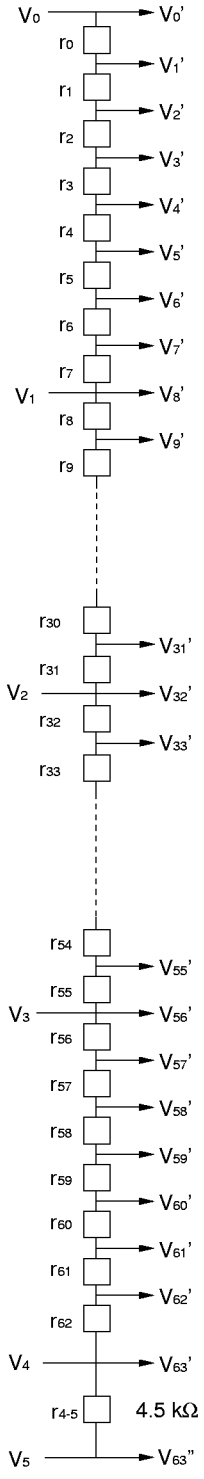
Because the current flowing through ladder resistors r_0 to r_{62} is small, its use for double-sided mounting impairs the IC's stable operation when the level of the γ-corrected power supply terminal is inverted thus causing display failures.

Figure 1. Relationship Between Input Data and Output Voltage



Resistor Strings

Figure 2-1. Relationship Between Input Data and Output Voltage: $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_{SS2}$

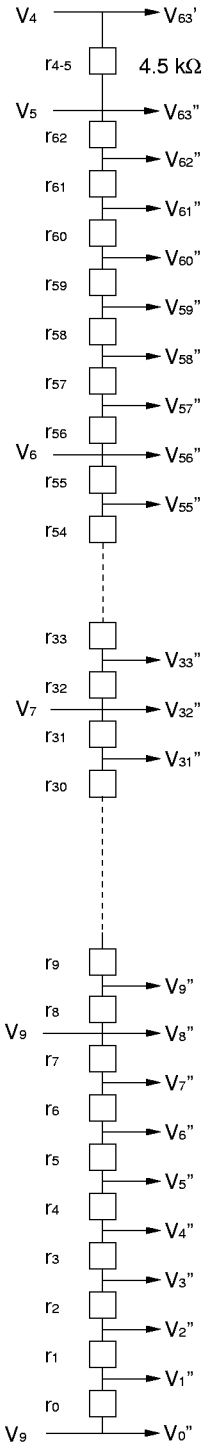


Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage		
00_H	0	0	0	0	0	0	V_0'	V_0	
01_H	0	0	0	0	0	1	V_1'	$V_1 + (V_0 - V_1)$	2250/2650
02_H	0	0	0	0	1	0	V_2'	$V_1 + (V_0 - V_1)$	1850/2650
03_H	0	0	0	0	1	1	V_3'	$V_1 + (V_0 - V_1)$	1450/2650
04_H	0	0	0	1	0	0	V_4'	$V_1 + (V_0 - V_1)$	1100/2650
05_H	0	0	0	1	0	1	V_5'	$V_1 + (V_0 - V_1)$	750/2650
06_H	0	0	0	1	1	0	V_6'	$V_1 + (V_0 - V_1)$	450/2650
07_H	0	0	0	1	1	1	V_7'	$V_1 + (V_0 - V_1)$	200/2650
08_H	0	0	1	0	0	0	V_8'	V_1	
09_H	0	0	1	0	0	1	V_9'	$V_2 + (V_1 - V_2)$	1800/2000
$0A_H$	0	0	1	0	1	0	V_{10}'	$V_2 + (V_1 - V_2)$	1650/2000
$0B_H$	0	0	1	0	1	1	V_{11}'	$V_2 + (V_1 - V_2)$	1500/2000
$0C_H$	0	0	1	1	0	0	V_{12}'	$V_2 + (V_1 - V_2)$	1350/2000
$0D_H$	0	0	1	1	0	1	V_{13}'	$V_2 + (V_1 - V_2)$	1200/2000
$0E_H$	0	0	1	1	1	0	V_{14}'	$V_2 + (V_1 - V_2)$	1100/2000
$0F_H$	0	0	1	1	1	1	V_{15}'	$V_2 + (V_1 - V_2)$	1000/2000
10_H	0	1	0	0	0	0	V_{16}'	$V_2 + (V_1 - V_2)$	900/2000
11_H	0	1	0	0	0	1	V_{17}'	$V_2 + (V_1 - V_2)$	800/2000
12_H	0	1	0	0	1	0	V_{18}'	$V_2 + (V_1 - V_2)$	700/2000
13_H	0	1	0	0	1	1	V_{19}'	$V_2 + (V_1 - V_2)$	650/2000
14_H	0	1	0	1	0	0	V_{20}'	$V_2 + (V_1 - V_2)$	600/2000
15_H	0	1	0	1	0	1	V_{21}'	$V_2 + (V_1 - V_2)$	550/2000
16_H	0	1	0	1	1	0	V_{22}'	$V_2 + (V_1 - V_2)$	500/2000
17_H	0	1	0	1	1	1	V_{23}'	$V_2 + (V_1 - V_2)$	450/2000
18_H	0	1	1	0	0	0	V_{24}'	$V_2 + (V_1 - V_2)$	400/2000
19_H	0	1	1	0	0	1	V_{25}'	$V_2 + (V_1 - V_2)$	350/2000
$1A_H$	0	1	1	0	1	0	V_{26}'	$V_2 + (V_1 - V_2)$	300/2000
$1B_H$	0	1	1	0	1	1	V_{27}'	$V_2 + (V_1 - V_2)$	250/2000
$1C_H$	0	1	1	1	0	0	V_{28}'	$V_2 + (V_1 - V_2)$	200/2000
$1D_H$	0	1	1	1	0	1	V_{29}'	$V_2 + (V_1 - V_2)$	150/2000
$1E_H$	0	1	1	1	1	0	V_{30}'	$V_2 + (V_1 - V_2)$	100/2000
$1F_H$	0	1	1	1	1	1	V_{31}'	$V_2 + (V_1 - V_2)$	50/2000
20_H	1	0	0	0	0	0	V_{32}'	V_2	
21_H	1	0	0	0	0	1	V_{33}'	$V_3 + (V_2 - V_3)$	1300/1350
22_H	1	0	0	0	1	0	V_{34}'	$V_3 + (V_2 - V_3)$	1250/1350
23_H	1	0	0	0	1	1	V_{35}'	$V_3 + (V_2 - V_3)$	1200/1350
24_H	1	0	0	1	0	0	V_{36}'	$V_3 + (V_2 - V_3)$	1150/1350
25_H	1	0	0	1	0	1	V_{37}'	$V_3 + (V_2 - V_3)$	1100/1350
26_H	1	0	0	1	1	0	V_{38}'	$V_3 + (V_2 - V_3)$	1050/1350
27_H	1	0	0	1	1	1	V_{39}'	$V_3 + (V_2 - V_3)$	1000/1350
28_H	1	0	1	0	0	0	V_{40}'	$V_3 + (V_2 - V_3)$	950/1350
29_H	1	0	1	0	0	1	V_{41}'	$V_3 + (V_2 - V_3)$	900/1350
$2A_H$	1	0	1	0	1	0	V_{42}'	$V_3 + (V_2 - V_3)$	850/1350
$2B_H$	1	0	1	0	1	1	V_{43}'	$V_3 + (V_2 - V_3)$	800/1350
$2C_H$	1	0	1	1	0	0	V_{44}'	$V_3 + (V_2 - V_3)$	750/1350
$2D_H$	1	0	1	1	0	1	V_{45}'	$V_3 + (V_2 - V_3)$	700/1350
$2E_H$	1	0	1	1	1	0	V_{46}'	$V_3 + (V_2 - V_3)$	650/1350
$2F_H$	1	0	1	1	1	1	V_{47}'	$V_3 + (V_2 - V_3)$	600/1350
30_H	1	1	0	0	0	0	V_{48}'	$V_3 + (V_2 - V_3)$	550/1350
31_H	1	1	0	0	0	1	V_{49}'	$V_3 + (V_2 - V_3)$	500/1350
32_H	1	1	0	0	1	0	V_{50}'	$V_3 + (V_2 - V_3)$	450/1350
33_H	1	1	0	0	1	1	V_{51}'	$V_3 + (V_2 - V_3)$	400/1350
34_H	1	1	0	1	0	0	V_{52}'	$V_3 + (V_2 - V_3)$	350/1350
35_H	1	1	0	1	0	1	V_{53}'	$V_3 + (V_2 - V_3)$	300/1350
36_H	1	1	0	1	1	0	V_{54}'	$V_3 + (V_2 - V_3)$	200/1350
37_H	1	1	0	1	1	1	V_{55}'	$V_3 + (V_2 - V_3)$	100/1350
38_H	1	1	1	0	0	0	V_{56}'	V_3	
39_H	1	1	1	0	0	1	V_{57}'	$V_4 + (V_3 - V_4)$	1150/1250
$3A_H$	1	1	1	0	1	0	V_{58}'	$V_4 + (V_3 - V_4)$	1050/1250
$3B_H$	1	1	1	0	1	1	V_{59}'	$V_4 + (V_3 - V_4)$	900/1250
$3C_H$	1	1	1	1	0	0	V_{60}'	$V_4 + (V_3 - V_4)$	750/1250
$3D_H$	1	1	1	1	0	1	V_{61}'	$V_4 + (V_3 - V_4)$	600/1250
$3E_H$	1	1	1	1	1	0	V_{62}'	$V_4 + (V_3 - V_4)$	400/1250
$3F_H$	1	1	1	1	1	1	V_{63}'	V_4	

Caution V_4 and V_5 are interconnected inside the IC by resistors r_{4-5} (4.5 kΩ).

Resistor Strings

Figure 2-1. Relationship Between Input Data and Output Voltage: $V_{DD2} > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2}$



Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage		
00_H	0	0	0	0	0	0	V_0"	V_9	
01_H	0	0	0	0	0	1	V_1"	$V_9 + (V_8 - V_9)$	400/2650
02_H	0	0	0	0	1	0	V_2"	$V_9 + (V_8 - V_9)$	800/2650
03_H	0	0	0	0	1	1	V_3"	$V_9 + (V_8 - V_9)$	1200/2650
04_H	0	0	0	1	0	0	V_4"	$V_9 + (V_8 - V_9)$	1550/2650
05_H	0	0	0	1	0	1	V_5"	$V_9 + (V_8 - V_9)$	1900/2650
06_H	0	0	0	1	1	0	V_6"	$V_9 + (V_8 - V_9)$	2200/2650
07_H	0	0	0	1	1	1	V_7"	$V_9 + (V_8 - V_9)$	2450/2650
08_H	0	0	1	0	0	0	V_8"	V_8	
09_H	0	0	1	0	0	1	V_9"	$V_8 + (V_7 - V_8)$	200/2000
$0A_H$	0	0	1	0	1	0	V_{10}"	$V_8 + (V_7 - V_8)$	350/2000
$0B_H$	0	0	1	0	1	1	V_{11}"	$V_8 + (V_7 - V_8)$	500/2000
$0C_H$	0	0	1	1	0	0	V_{12}"	$V_8 + (V_7 - V_8)$	650/2000
$0D_H$	0	0	1	1	0	1	V_{13}"	$V_8 + (V_7 - V_8)$	800/2000
$0E_H$	0	0	1	1	1	0	V_{14}"	$V_8 + (V_7 - V_8)$	900/2000
$0F_H$	0	0	1	1	1	1	V_{15}"	$V_8 + (V_7 - V_8)$	1000/2000
10_H	0	1	0	0	0	0	V_{16}"	$V_8 + (V_7 - V_8)$	1100/2000
11_H	0	1	0	0	0	1	V_{17}"	$V_8 + (V_7 - V_8)$	1200/2000
12_H	0	1	0	0	1	0	V_{18}"	$V_8 + (V_7 - V_8)$	1300/2000
13_H	0	1	0	0	1	1	V_{19}"	$V_8 + (V_7 - V_8)$	1350/2000
14_H	0	1	0	1	0	0	V_{20}"	$V_8 + (V_7 - V_8)$	1400/2000
15_H	0	1	0	1	0	1	V_{21}"	$V_8 + (V_7 - V_8)$	1450/2000
16_H	0	1	0	1	1	0	V_{22}"	$V_8 + (V_7 - V_8)$	1500/2000
17_H	0	1	0	1	1	1	V_{23}"	$V_8 + (V_7 - V_8)$	1550/2000
18_H	0	1	1	0	0	0	V_{24}"	$V_8 + (V_7 - V_8)$	1600/2000
19_H	0	1	1	0	0	1	V_{25}"	$V_8 + (V_7 - V_8)$	1650/2000
$1A_H$	0	1	1	0	1	0	V_{26}"	$V_8 + (V_7 - V_8)$	1700/2000
$1B_H$	0	1	1	0	1	1	V_{27}"	$V_8 + (V_7 - V_8)$	1750/2000
$1C_H$	0	1	1	1	0	0	V_{28}"	$V_8 + (V_7 - V_8)$	1800/2000
$1D_H$	0	1	1	1	0	1	V_{29}"	$V_8 + (V_7 - V_8)$	1850/2000
$1E_H$	0	1	1	1	1	0	V_{30}"	$V_8 + (V_7 - V_8)$	1900/2000
$1F_H$	0	1	1	1	1	1	V_{31}"	$V_8 + (V_7 - V_8)$	1950/2000
20_H	1	0	0	0	0	0	V_{32}"	V_7	
21_H	1	0	0	0	0	1	V_{33}"	$V_7 + (V_6 - V_7)$	50/1350
22_H	1	0	0	0	1	0	V_{34}"	$V_7 + (V_6 - V_7)$	100/1350
23_H	1	0	0	0	1	1	V_{35}"	$V_7 + (V_6 - V_7)$	150/1350
24_H	1	0	0	1	0	0	V_{36}"	$V_7 + (V_6 - V_7)$	200/1350
25_H	1	0	0	1	0	1	V_{37}"	$V_7 + (V_6 - V_7)$	250/1350
26_H	1	0	0	1	1	0	V_{38}"	$V_7 + (V_6 - V_7)$	300/1350
27_H	1	0	0	1	1	1	V_{39}"	$V_7 + (V_6 - V_7)$	350/1350
28_H	1	0	1	0	0	0	V_{40}"	$V_7 + (V_6 - V_7)$	400/1350
29_H	1	0	1	0	0	1	V_{41}"	$V_7 + (V_6 - V_7)$	450/1350
$2A_H$	1	0	1	0	1	0	V_{42}"	$V_7 + (V_6 - V_7)$	500/1350
$2B_H$	1	0	1	0	1	1	V_{43}"	$V_7 + (V_6 - V_7)$	550/1350
$2C_H$	1	0	1	1	0	0	V_{44}"	$V_7 + (V_6 - V_7)$	600/1350
$2D_H$	1	0	1	1	0	1	V_{45}"	$V_7 + (V_6 - V_7)$	650/1350
$2E_H$	1	0	1	1	1	0	V_{46}"	$V_7 + (V_6 - V_7)$	700/1350
$2F_H$	1	0	1	1	1	1	V_{47}"	$V_7 + (V_6 - V_7)$	750/1350
30_H	1	1	0	0	0	0	V_{48}"	$V_7 + (V_6 - V_7)$	800/1350
31_H	1	1	0	0	0	1	V_{49}"	$V_7 + (V_6 - V_7)$	850/1350
32_H	1	1	0	0	1	0	V_{50}"	$V_7 + (V_6 - V_7)$	900/1350
33_H	1	1	0	0	1	1	V_{51}"	$V_7 + (V_6 - V_7)$	950/1350
34_H	1	1	0	1	0	0	V_{52}"	$V_7 + (V_6 - V_7)$	1000/1350
35_H	1	1	0	1	0	1	V_{53}"	$V_7 + (V_6 - V_7)$	1050/1350
36_H	1	1	0	1	1	0	V_{54}"	$V_7 + (V_6 - V_7)$	1150/1350
37_H	1	1	0	1	1	1	V_{55}"	$V_7 + (V_6 - V_7)$	1250/1350
38_H	1	1	1	0	0	0	V_{56}"	V_6	
39_H	1	1	1	0	0	1	V_{57}"	$V_6 + (V_5 - V_6)$	100/1250
$3A_H$	1	1	1	0	1	0	V_{58}"	$V_6 + (V_5 - V_6)$	200/1250
$3B_H$	1	1	1	0	1	1	V_{59}"	$V_6 + (V_5 - V_6)$	350/1250
$3C_H$	1	1	1	1	0	0	V_{60}"	$V_6 + (V_5 - V_6)$	500/1250
$3D_H$	1	1	1	1	0	1	V_{61}"	$V_6 + (V_5 - V_6)$	650/1250
$3E_H$	1	1	1	1	1	0	V_{62}"	$V_6 + (V_5 - V_6)$	850/1250
$3F_H$	1	1	1	1	1	1	V_{63}"	V_5	

Caution V_4 and V_5 are interconnected inside the IC by resistors r_{4-5} (4.5 kΩ).

Ladder Resistance Values (r_0 to r_{62}): Reference Value

Resistor Name	Resistance Value ( )	Resistor Name	Resistance Value ( )
r_0	400	r_{32}	50
r_1	400	r_{33}	50
r_2	400	r_{34}	50
r_3	350	r_{35}	50
r_4	350	r_{36}	50
r_5	300	r_{37}	50
r_6	250	r_{38}	50
r_7	200	r_{39}	50
r_8	200	r_{40}	50
r_9	150	r_{41}	50
r_{10}	150	r_{42}	50
r_{11}	150	r_{43}	50
r_{12}	150	r_{44}	50
r_{13}	100	r_{45}	50
r_{14}	100	r_{46}	50
r_{15}	100	r_{47}	50
r_{16}	100	r_{48}	50
r_{17}	100	r_{49}	50
r_{18}	50	r_{50}	50
r_{19}	50	r_{51}	50
r_{20}	50	r_{52}	50
r_{21}	50	r_{53}	100
r_{22}	50	r_{54}	100
r_{23}	50	r_{55}	100
r_{24}	50	r_{56}	100
r_{25}	50	r_{57}	100
r_{26}	50	r_{58}	150
r_{27}	50	r_{59}	150
r_{28}	50	r_{60}	150
r_{29}	50	r_{61}	200
r_{30}	50	r_{62}	400
r_{31}	50	Total	7250

V_0, V_9 → (top of r_0)
V_1, V_8 → (r_7)
V_2, V_7 → (r_{31})
← V_2, V_7 (top of r_{32})
← V_3, V_6 (r_{55})
← V_4, V_5 (r_{62})

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format : 6 bits × 2 RGBs (6 dots)
Input width : 36 bits (2-pixel data)

$R/\overline{L}$ = H (Right shift)

Output	S_1	S_2	S_3	S_4	S_5	...	S_{311}	S_{312}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	D_{40} to D_{45}	...	D_{40} to D_{45}	D_{50} to D_{55}

$R/\overline{L}$ = L (Left shift)

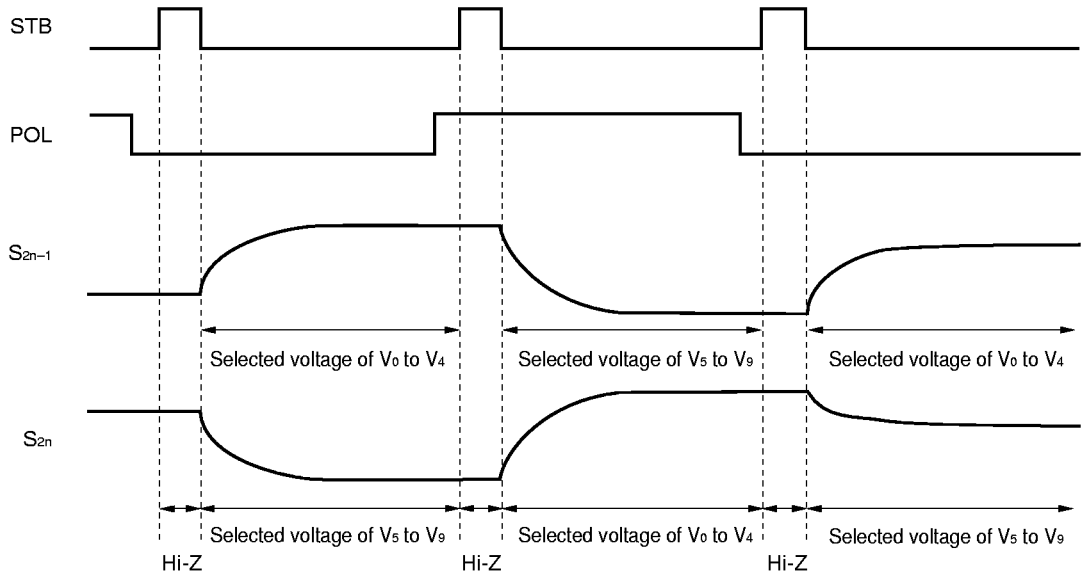
Output	S_1	S_2	S_3	S_4	S_5	...	S_{311}	S_{312}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	D_{40} to D_{45}	...	D_{40} to D_{45}	D_{50} to D_{55}

POL	S_{2n-1}	S_{2n}
L	V_0 to V_4	V_5 to V_9
H	V_5 to V_9	V_0 to V_4

S_{2n-1} (Odd output), S_{2n} (Even output) n = 1, 2, ..., 156

6. RELATIONSHIP BETWEEN STB, POL, AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB rising edge.



Absolute Maximum Ratings (T_A = 25 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	–0.5 to +6.5	V
Driver Part Supply Voltage	V_{DD2}	–0.5 to +12.0	V
Logic Part Input Voltage	V_{I1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Input Voltage	V_{I2}	–0.5 to V_{DD2} + 0.5	V
Logic Part Output Voltage	V_{O1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Output Voltage	V_{O2}	–0.5 to V_{DD2} + 0.5	V
Total Power Dissipation	P_D	500	mW
Operating Temperature Range	T_A	–10 to +75	°C
Storage Temperature Range	$T_{stg.}$	–55 to +125	°C

Recommended Operating Range (T_A = –10 to +75 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}	3.0	3.3	3.6	V
Driver Part Supply Voltage	V_{DD2}	10.0	10.5	13.5	V
High-Level Input Voltage	V_{IH}	0.7 V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}	0		0.3 V_{DD1}	V
γ-Corrected Voltage	V_0 to V_9	V_{SS2} + 0.05		V_{DD2} – 0.05	V
Driver Part Output Voltage	V_O	V_{SS2} + 0.1		V_{DD2} – 0.1	V
Maximum Clock Frequency	$f_{max.}$	45			MHz

Electrical specifications (T_A = –10 to +75 °C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 10.5 V ±0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input Leak Current	I_L					±1.0	μA
High-Level Output Voltage	V_{OH}	STHR (STHL), I_O = 0 mA		V_{DD1} – 0.1			V
Low-level Output Voltage	V_{OL}	STHR (STHL), I_O = 0 mA				0.1	V
γ-Corrected Supply Current		V_0 – V_9 = 10 V	V_0, V_9		0.6	1.0	mA
Driver Output Current	I_{VOH}	V_X = 9 V, V_{OUT} = 3 V[Note]				–0.3	mA
	I_{VOL}	V_X = 3 V, V_{OUT} = 9 V[Note]		0.3			mA

Note V_X refers to the output voltage of analog output pins S_1 to S_{312}.
V_{OUT} refers to the voltage applied to analog output pins S_1 to S_{312}.

Electrical Specifications (T_A = –10 to +75 °C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 10.5 V ±0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output Voltage Deviation[Note 1]	ΔV_O	Input data: 00_H to $3F_H$		±5	±20	mV
Average Output Voltage Variation[Note 2]	ΔV_{AV}	Input data: 00_H to $3F_H$		±10		mV
Output Voltage Range	V_O	Input data: 00_H to $3F_H$	0.1		V_{DD2} - 0.2	V
Logic Part Dynamic Current Consumption	I_{DD1}	V_{DD}; when with no load[Notes 3, 4]		0.39	10	mA
Driver Part Dynamic Current Consumption	I_{DD21}	V_{DD2} = 10.5 ± 0.5 V when with no load[Notes 3, 4]		2.7	8.0	mA
	I_{DD22}	V_{DD2} = 13.5 ± 0.5 V when with no load[Notes 3, 4]		3.5	10.0	mA

Notes 1. The output voltage deviation refers to the voltage difference between adjoining output pins when the display data is the same (within the chip).

2. The average output voltage variation refers to the average output voltage difference between chips. The average output voltage refers to the average voltage between chips when the display data is the same.

3. The STB cycle is defined to be 20 μs at f_{CLK} = 45 MHz.
The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.

4. Refers to the current consumption per driver when cascades are connected under the assumption of XGA single-sided mounting (10 units).

Switching Characteristics (T_A = –10 to +75 °C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 10.5 V ±0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	C_L = 25 pF		8.8	15	ns
Driver Output Delay Time 1	t_{PHL2}	C_L = 50 pF, R = 50 kΩ		5.3	11	μs
Driver Output Delay Time 2	t_{PHL3}	C_L = 50 pF, R = 50 kΩ		11	17	μs
Driver Output Delay Time 3	t_{PLH2}	C_L = 50 pF, R = 50 kΩ		5.7	11	μs
Driver Output Delay Time 4	t_{PLH3}	C_L = 50 pF, R = 50 kΩ		11	17	μs
Input Capacitance 1	C_1	STHR, STHL excluded T_A = 25 °C		5	15	pF
Input Capacitance 2	C_2	STHR, STHL T_A = 25 °C		5	15	pF

Timing Requirement

(T_A = –10 to +75 °C, V_{DD1} = 3.3 V ±0.3 V, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 8.0 ns)

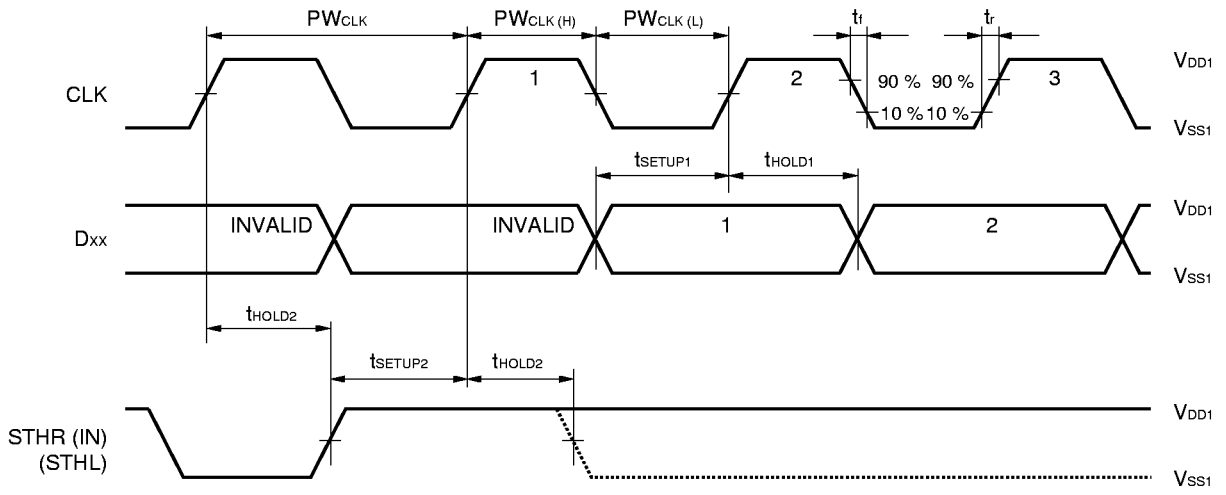
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		22			ns
Clock Pulse Low Period	$PW_{CLK(L)}$		6			ns
Clock Pulse High Period	$PW_{CLK(H)}$		6			ns
Data Setup Time	t_{SETUP1}		6			ns
Data Hold Time	t_{HOLD1}		6			ns
Start Pulse Setup Time	t_{SETUP2}		6			ns
Start Pulse Hold Time	t_{HOLD2}		6			ns
Start Pulse Low Period	t_{SPL}		6			ns
STB Pulse Width	PW_{STB}		0.5			μs
Data Invalid Period	t_{INV}		1			CLK
Final Data Timing	t_{LDT}		2			CLK
CLK-STB Time	$t_{CLK-STB}$	CLK ↑ → STB ↓	6			ns
STB-CLK Time	$t_{STB-CLK}$	STB ↓ → CLK ↑	6			ns
Time Between STB and Start Pulse	$t_{STB-STH}$	STB ↓ → STHR ↑	60			ns
POL-STB Time	$t_{POL-STB}$	POL ↑ or ↓ → STB ↑	–5			ns
STB-POL Time	$t_{STB-POL}$	STB ↓ → POL ↑ or ↓	6			ns

Switching Characteristics Waveform (R/$\overline{L}$ = H)

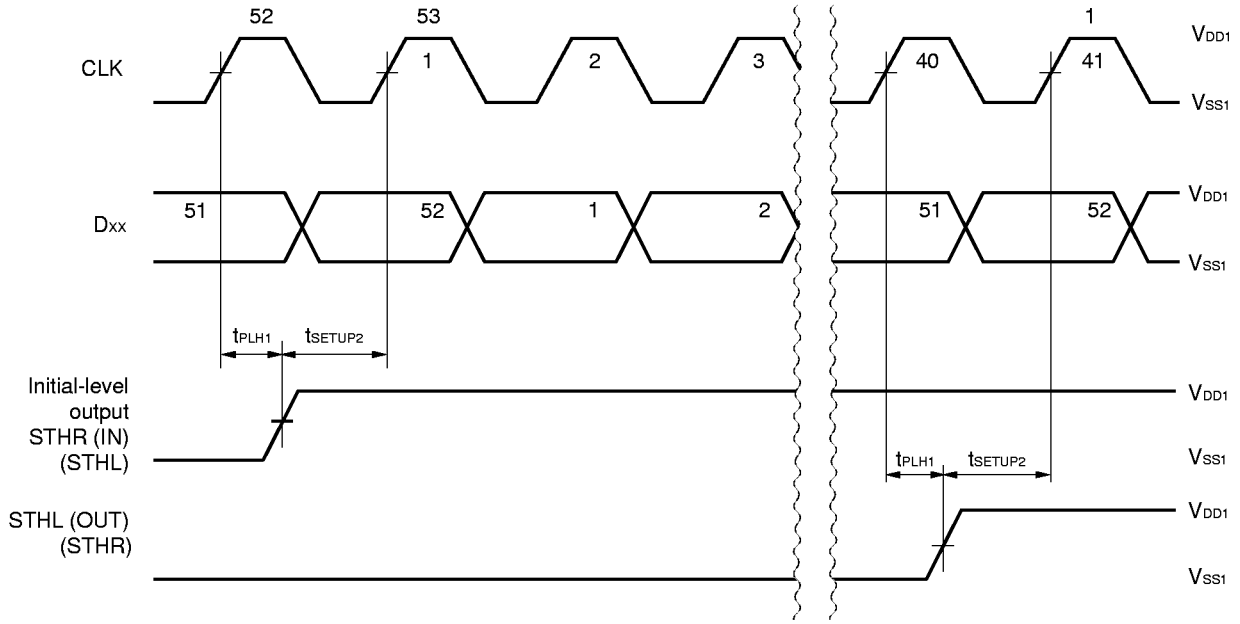
In ( ) : R/$\overline{L}$ = L

Unless otherwise specified, the input level is defined to be 0.5 V_{DD1}.

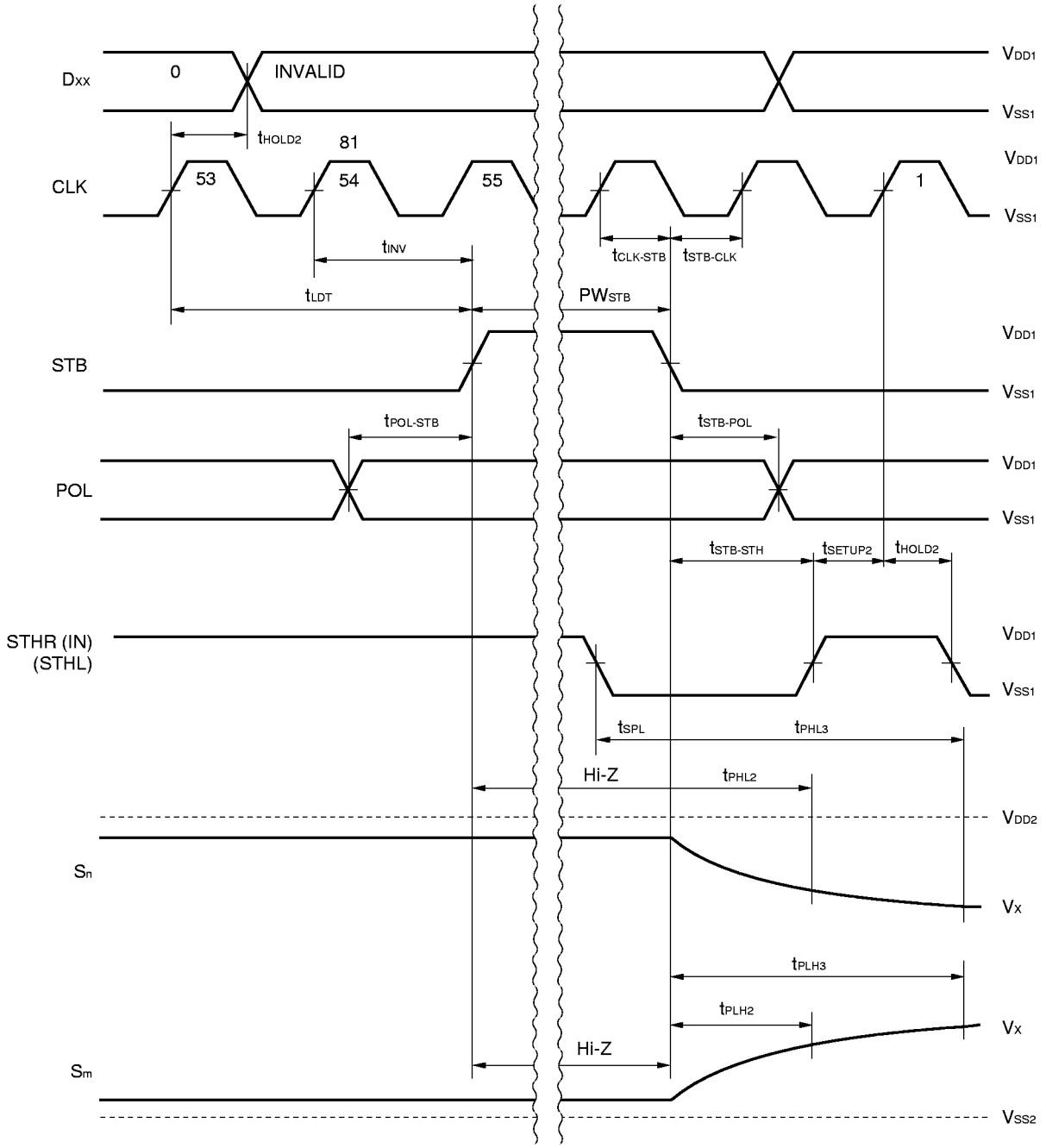
(1) Initial-Stage Driver's Input/Output Waveform



(2) Second- to Final-Stage Drivers's Input/Output Timing



(3) Driver Output Timing



Vx refers to the final output voltage. t_{PLH2} and t_{PHL2} refer to the time required to reach an output precision level of 10 % (0.1 Vx); and t_{PLH3} and t_{PHL3} refer to the time required to reach an output precision level of 6 bits.

RECOMMENDED MOUNTING CONDITIONS

When mounting this product, please make sure that the following recommended conditions are satisfied.

For packaging methods and conditions other than those recommended below, please contact NEC sales personnel.

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350 °C; heating for 2 to 3 seconds; pressure 100 g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100 °C; pressure 3 to 8 kg/cm^2; time 3 to 5 secs. Real bonding 165 to 180 °C; pressure 25 to 45 kg/cm^2; time 30 to 40 secs. (when using the anisotropic conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.

REFERENCE

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades to NEC's Semiconductor Devices (C11531E)