CAT27HC256L/CAT27HC256LI

256K-Bit HIGH SPEED CMOS EPROM

FEATURES

- **Fast Read Access Times:**
  –55/70/90/120ns (Commercial)
  –70/90/120ns (Industrial)
- **Single 5V Supply—Read Mode**
- **Low Power CMOS Dissipation:**
  –Active: 50 mA (Commercial)
  60 mA (Industrial)
  –Standby: 100 μA
- **High Speed Programming: 100 μs/byte**
- **CMOS and TTL Compatible I/O**
- **12.5V Programming Level**
- **JEDEC Standard Pinouts:**
  –28 pin DIP and CERDIP
  –32 pin LCC
  –32 pin PLCC
- **Electronic Signature**

DESCRIPTION

The CAT27HC256L/CAT27HC256LI is a high speed low power 32K x 8 bits UV erasable and electronically reprogrammable EPROM ideally suited for high speed applications. Any byte can be accessed in less than 55ns making this device compatible with high performance microprocessor systems by eliminating the need for speed-robbing wait states.

The Quick-Pulse(1) programming algorithm reduces the time required to program the chip and ensures more reliable programming. The CAT27HC256L/CAT27HC256LI is used in applications where fast turnaround and pattern experimentation are important requirements.

The CAT27HC256L/CAT27HC256LI is manufactured using Catalyst's advanced CMOS floating gate technology. The device is available in JEDEC approved 28 pin DIP and CERDIP, 32 pin LCC and 32 pin PLCC packages. The transparent lid on the 28 pin CERDIP and 32 pin LCC allows the user the option of UV erasing the bit pattern in the device, thus allowing a new pattern to be written in.

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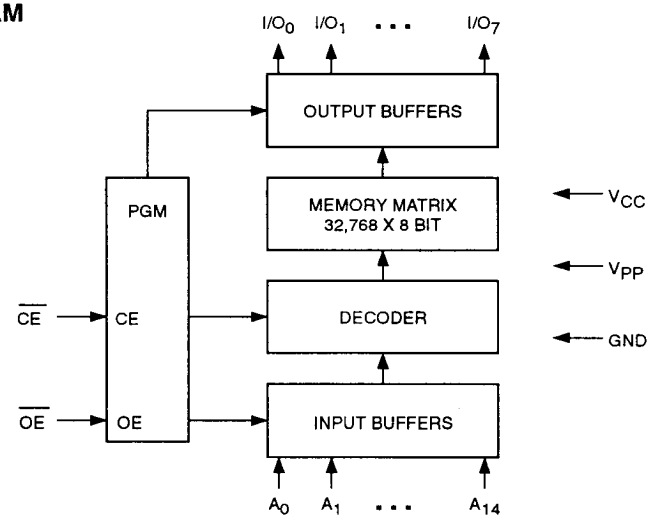
BLOCK DIAGRAM



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Note:
(1) Quick-Pulse is a trademark of Intel Corporation.

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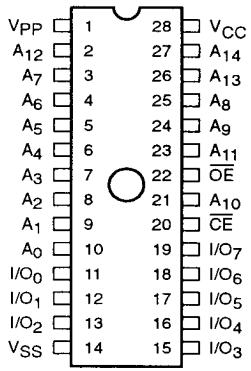
PIN CONFIGURATION

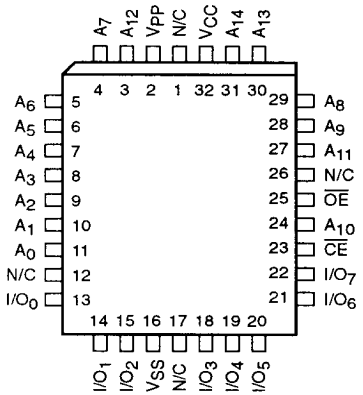
DIP and CERDIP Package



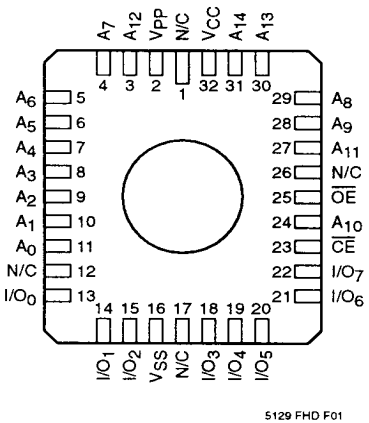
PIN FUNCTIONS

A_0–A_{14}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
I/O_0–I/O_7	Data Inputs/Outputs
NC	No Connect
V_{PP}	Program Supply Voltage
V_{CC}	5V Supply

PLCC Package



LCC Package



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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with
Respect to Ground(3) .....–2.0V to V_{CC} +2.0V

Voltage on Pin A_9 with
Respect to Ground(3) .....–2.0V to +13.5V

V_{PP} with Respect to Ground
during Program/Erase .....–2.0V to +14.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation
Capability (T_A = 25°C) ..... 1.0 W

Lead Soldering Temperature (10 secs) .....300°C

Output Short-Circuit Current(4) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
V_{ZAP}(2)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(2)(5)	Latch-Up	100		mA	JEDEC Standard 17

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V
C_{OUT}(2)	Output Pin Capacitance	10	pF	V_{OUT} = 0V
CV_{PP}(2)	V_{PP} Supply Capacitance	25	pF	V_{PP} = 0V

Note:
(2) This parameter is tested initially and after a design or process change.
(3) The minimum DC input voltage is –0.5. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20 ns.
(4) Output shorted for no more than one second. No more than one output shorted at a time.
(5) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} + 1V.

D.C. OPERATING CHARACTERISTICS, Read Operation

CAT27HC256L T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT27HC256LI T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter		Limits Min.	Typ.	Max.	Units	Test Conditions
I_{CC}[6]	V_{CC} Operating Current (TTL)	Com.			50	mA	$\overline{CE}$ = V_{IL}, f = 5MHz All I/O's Open
		Ind.			60		
I_{CCC}[6]	V_{CC} Operating Current (CMOS)	Com.			50	mA	$\overline{CE}$ = V_{ILC}, f = 5MHz All I/O's Open
		Ind.			60		
I_{SB1}	V_{CC} Standby Current (TTL)	Com.			2	mA	$\overline{CE}$ = V_{IL}
		Ind.			3		
I_{SB2}	V_{CC} Standby Current (CMOS)	Com.			100	µA	$\overline{CE}$ = V_{IL}
		Ind.			100		
I_{LI}	Input Leakage Current				10	µA	V_{IN} = 5.5V
I_{LO}	Output Leakage Current				10	µA	V_{OUT} = 5.5V
I_{PP1}	V_{PP} Leakage Current				10	µA	V_{PP} = 5.5V
V_{IH}	Input High Level TTL		2.0		V_{CC} +0.5	V	
V_{IL}	Input Low Level TTL		–0.5		0.8	V	
V_{OH}	Output Voltage High Level		2.4			V	I_{OH} = –1.0 mA
V_{OL}	Output Voltage Low Level				0.40	V	I_{OL} = 4.0 mA
V_{ILC}	Input Low Level CMOS		–0.5		0.30	V	
V_{IHC}	Input High Level CMOS		V_{CC} – 0.5		V_{CC} +0.5	V	

Note:
(6) The maximum current value is with outputs I/O_0 to I/O_7 unloaded.

A.C. CHARACTERISTICS, Read Operation

CAT27HC256L T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT27HC256LI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	27HC256L-55(7)		27HC256L-70 27HC256LI-70		27HC256L-90 27HC256LI-90		27HC256L-12 27HC256LI-12		Unit
		Min	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address Access Time		55		70		90		120	ns
t_{CE}	$\overline{CE}$ to Output Delay		55		70		90		120	ns
t_{OE}	$\overline{OE}$ to Output Delay		30		35		40		50	ns
t_{OH}(2)(8)	Output Hold A, $\overline{OE}$, $\overline{CE}$	0		0		0		0		ns
t_{DF}(2)(8)	$\overline{OE}$ High to High-Z Output	0	30	0	35	0	40	0	50	ns

Figure 1. A.C. Testing Input/Output Waveform(9)

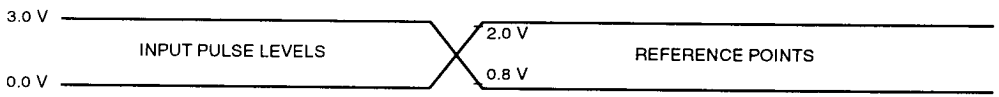

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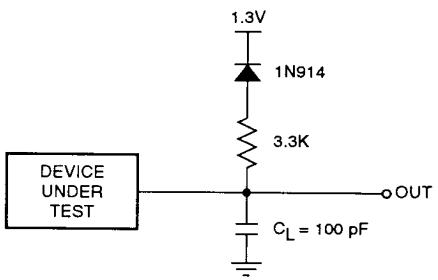
Figure 2. A.C. Testing Load Circuit (example)



C_L INCLUDES JIG CAPACITANCE

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Note:
(2) This parameter is tested initially and after a design or process change.
(7) V_{CC} = 5V ±5% for CAT27HC256L-55.
(8) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
(9) Input rise and fall times (10% to 90%) <10ns.

D.C. CHARACTERISTICS, Programming Operation

CAT27HC256L T_A = 25°C ±5°C
CAT27HC256LI T_A = 25°C ±5°C

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
V_{CC}(11)	Supply Voltage (Quick Pulse Algorithm)	6.0	6.25	6.5	V	
	Supply Voltage (Intelligent Algorithm)	5.75	6.0	6.25	V	
V_{PP}(10)(11)	Programming Voltage (Quick Pulse Algorithm)	12.5	12.75	13.0	V	
	Programming Voltage (Intelligent Algorithm)	12.0	12.5	13.0	V	
I_{CCP}(6)	V_{CC} Supply Current Program and Verify			80	mA	$\overline{CE} = V_{IL}$
I_{PP}(6)	V_{PP} Supply Current Program Operation			40	mA	$\overline{CE} = V_{IL}$
I_{LI}	Input Leakage Current			10	µA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 5.25V
V_{IL}	Input Low-Level TTL	–0.50		0.80	V	
V_{ILC}	Input Low-Level CMOS	–0.50		0.30	V	
V_{IH}	Input High-Level TTL	2.0		V_{CC} + 0.5	V	
V_{IHC}	Input High-Level CMOS	V_{CC} – 0.50		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (Verify)			0.40	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage (Verify)	2.4			V	I_{OH} = 1.0 mA
V_H(6)(10)	A_9 Signature Mode Voltage	11.5		12.5	V	

Note:
(6) The maximum current value is with outputs I/O_0 to I/O_7 unloaded.
(10) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
(11) When programming, a 0.1 µF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.

A.C. CHARACTERISTICS, Programming Operation

CAT27HC256L T_A = 25°C ±5°C
CAT27HC256LI T_A = 25°C ±5°C

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
t_{AS}	Address Setup Time	2			µs	
t_{OES}	$\overline{OE}$ Setup Time	2			µs	
t_{DS}	Data Setup Time	2			µs	
t_{AH}	Address Hold Time	0			µs	
t_{DH}	Data Hold Time	2			µs	
t_{VPS}(10)	V_{PP} Setup Time	2			µs	
t_{VCS}(10)	V_{CC} Setup Time	2			µs	
t_{PW}	$\overline{CE}$ Program Pulse Width (Quick Pulse Algorithm)	95	100	105	µs	
t_{PW}	$\overline{CE}$ Program Pulse Width (Intelligent Algorithm)	0.95	1.0	1.05	ms	
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width (Intelligent Algorithm)	2.85		78.5	ms	
t_{DFP}(2)(8)	$\overline{OE}$ High to Output High-Z	0		130	ns	
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

Note:
(2) This parameter is tested initially and after a design or process change.
(8) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
(10) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

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FUNCTION TABLE

Mode	Pins					
	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	A_0 (10)	A_9 (24)	I/O
Read	V_{IL}	V_{IL}	V_{CC}	X	X	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{CC}	X	X	High-Z
Standby	V_{IH}	X	V_{CC}	X	X	High-Z
Program	V_{IL}	V_{IH}	V_{PP}	X	X	D_{IN}
Program Verify	V_{IH}	V_{IL}	V_{PP}	X	X	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	X	X	High-Z
Signature MFG.	V_{IL}	V_{IL}	V_{CC}	V_{IL}	V_H	31H
Signature Device	V_{IL}	V_{IL}	V_{CC}	V_{IH}	V_H	40H

NOTES ON THE FUNCTION TABLE

Logic Levels: V_{IH} = TTL Logic 1 level
V_{IL} = TTL Logic 0 level
X = Logic "Do not care," V_{IH} or V_{IL}

Supply Voltage: V_{PP} = Programming/High-Voltage
V_{CC} = Read/Low-Voltage
V_H = 12.0V ±0.5V

Read: Read Mode: The content of the addressed memory byte is placed on the I/O pins I/O_0 to I/O_7.

Output Disable: Device is selected (active mode), programming is disabled and I/O_0 to I/O_7 output buffers are tristated (PMOS and NMOS drivers turned-off).

Standby: Device is deselected, low power dissipation.

Program: Byte Programming Mode: Logic zeros in the bit pattern driving the I/O_0 to I/O_7 data input buffers are written into the respective memory cells of the addressed byte.

Program Verify: Following a programming cycle, to verify the cell contents of the memory byte being programmed (not recommended as a normal read operation).

Program Inhibit: $\overline{CE}$ set to logic one and $\overline{OE}$ set to logic one prevents programming and deselects the device.

Signature MFG: Signature mode with all other addresses at V_{IL}, code of IC manufacturer (Catalyst) output on I/O pins I/O_0 to I/O_7.

Signature Device: Signature mode with all other addresses at V_{IL}, code of IC type output on I/O pins I/O_0 to I/O_7.

DEVICE OPERATION

Read Operation and Standby Modes

Memory access for reading an address location is controlled by $\overline{CE}$ and $\overline{OE}$. Chip enable $\overline{CE}$ is used independently of all other input signals as the primary device selection. In the logic zero state (TTL level V_{IL}), $\overline{CE}$ powers up all inputs and enables internal circuitry. In the logic one state (CMOS level V_{IHC}) $\overline{CE}$ places the device in standby mode, all DC paths to ground are shut-off, and the power dissipation is reduced to a minimum. A logic one on Output Enable $\overline{OE}$ disables the output buffers and places the output pads in a high impedance state. Assuming that the address lines A_0 to A_{14} have been stable for a time equal to $t_{ACC} - t_{OE}$, the output data is available after a delay of t_{OE} from the falling edge of $\overline{OE}$.

Signature Mode

The Signature Mode allows one to identify the IC manufacturer and the device type. This mode is entered as a regular Read Mode by driving the $\overline{CE}$ and $\overline{OE}$ inputs low, and additionally driving the A_9 pin to high-voltage (V_H) with all other address lines at V_{IL}.

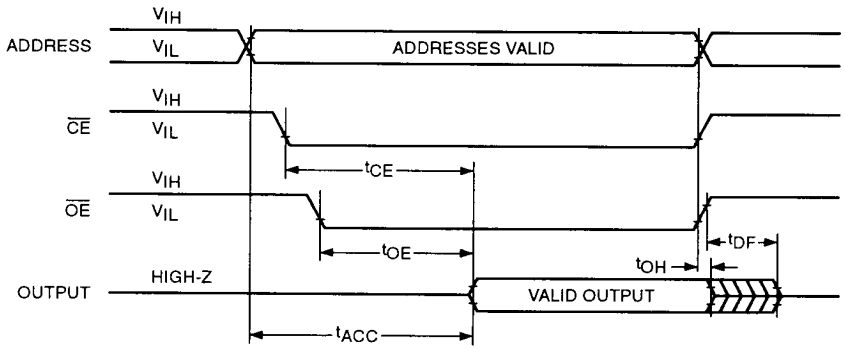
Driving A_0 to V_{IL} with all other addresses at V_{IL}, gives the the binary code of the IC manufacturer on outputs I/O_0 to I/O_7.

CATALYST Code:
0 0 1 1 0 0 0 1 (31H)

Driving A_0 to V_{IH} with all other addresses at V_{IL}, gives the the binary code of the device type on outputs I/O_0 to I/O_7.

27HC256L/27HC256LI Code:
0 1 0 0 0 0 0 0 (40H)

Figure 3. Read Operation Timing



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Programming Mode

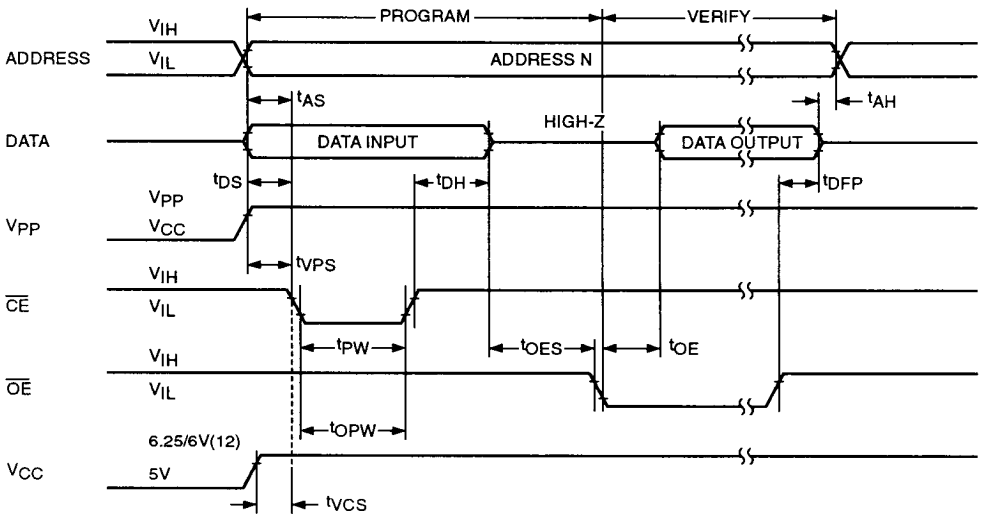
After a proper erase operation, all bits of the EPROM are in the logic one state. The device is programmed by selectively writing logic zeros into the desired bit locations. The programming mode is entered by raising $\overline{CE}$ and $\overline{OE}$ to a high level and bringing the low voltage supply pin (V_{CC}), followed by the high voltage supply pin (V_{PP}), to their respective programming levels.

After the address inputs A_0 to A_{14} and data inputs I/O_0 to I/O_7 are stabilized, $\overline{CE}$ is switched from the logic one to logic zero state to perform the programming. The particular memory cells of the addressed byte, corresponding to the 0's of the input data bits, are then programmed.

A Program Verify cycle is performed after each byte is programmed to ensure that the zero bits have been correctly written. The byte verification cycle is initiated by keeping $\overline{CE}$ at V_{IH} and switching $\overline{OE}$ from V_{IH} to V_{IL}, while all other pin voltages remain unchanged. In most cases a single 100µs programming cycle is sufficient to set a memory cell in the logic zero state. The Quick Pulse algorithm is recommended as the preferred device programming operation. The CAT27HC256L/CAT27HC256LI is also compatible with Intelligent Programming(13).

The flow charts for both the algorithms are given in Figures 5 and 6.

Figure 4. Programming Operation Timing



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Note:
(12) V_{CC} = 6.25V ±0.25V for Quick Pulse algorithm; 6.0V ±0.25V for Intelligent Programming algorithm.
(13) Intelligent is a trademark of Intel Corporation.

U.V. ERASURE OPERATION FOR CERDIP EPROMS

Direct exposure to fluorescent lamps such as those used in room light fixtures, can erase the CAT27HC256L/ CAT27HC256LI EPROM in less than three years. When exposed to direct sun light the EPROM can be erased in less than a week.

The recommended erasure procedure is to expose the CAT27HC256L/CAT27HC256LI EPROM to a standard ultraviolet light with a wavelength of 2537 Angstroms. The integrated dose for proper erasure is 15 Wsec/cm^2.

The erasure time with this dosage is approximately 15 to 60 minutes using an ultraviolet lamp with a 1200 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes.

The maximum integrated dose a CAT27HC256L/ CAT27HC256LI EPROM can be exposed to is 7258 Wsec/cm^2 (one week at 1200 uW/cm^2). Exposure of the device to higher U.V. doses may cause permanent damage and loss of functionality.

Figure 5. Quick Pulse Algorithm

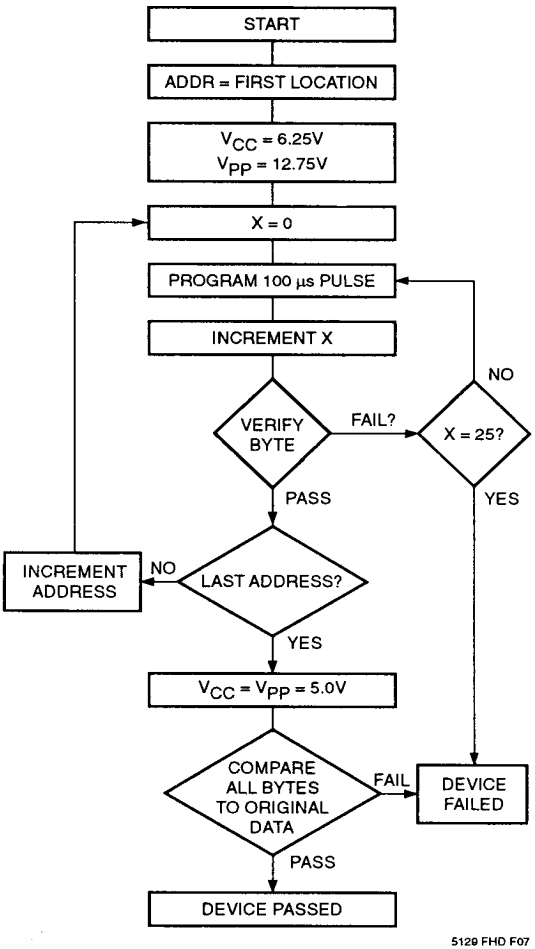

Figure 6. Intelligent Programming Algorithm