MOS INTEGRATED CIRCUIT
μPD1701C-015

PLL FREQUENCY SYNTHESIZER AND CONTROLLER FOR FM AND AM RADIO

The μPD1701C-015 is a CMOS LSI with built-in PLL synthesizer capable of receiving FM/AM in U.S.A. and Japan. In combination with a dedicated prescalar (μPB553AC), the μPB553AC can be used to construct high fidelity FM/AM digital synthesizer tuners for car audio and home stereo systems.

The device used in the display driver stage may be either μPD6320G or μPD6321G designed for FIP or LCD static display.

FEATURES

- 12-hour clock function
- Built-in PLL, swallow counter, and controller
- Reference frequency increased to 25 kHz due to use of pulse swallow method for FM
- Reception of Japanese traffic information (522 to 1629 kHz)
- U.S.A. and Japanese FM and AM band selectable by initializing switch
- U.S.A. FM channel space selectable by initializing switch (100/200 kHz)
- FIP or LCD static display (with μPD6320G/μPD6321G) μPD6320G and μPD6321G differ in display of the number "7" ("¯|" and " |").
- Built-in seek and scan functions (UP tuning only)
- Low-consumption current: 500 μA (TYP.) (clock operation only when CE pin at low level)
- Small 28-pin plastic DIP package (400 mil width) which occupies less circuit board space
- 5 V ±10 % single power supply

FUNCTION

Receiving frequency, channel spacing, reference frequency, intermediate frequency

COUNTRY	BAND	FREQUENCY RANGE	CHANNEL SPACE	REFERENCE FREQUENCY	INTERMEDIATE FREQUENCY
U.S.A.	AM	531 to 1 602 kHz	9 kHz	9 kHz	455 kHz
		530 to 1 620 kHz	10 kHz	10 kHz	455 kHz
	FM	87.9 to 107.9 MHz	100 kHz	25 kHz	10.7 MHz
		87.9 to 107.9 MHz	200 kHz	25 kHz	10.7 MHz
JAPAN	AM	531 to 1 629 kHz	9 kHz	9 kHz	455 kHz
	FM	76.1 to 89.9 MHz	100 kHz	25 kHz	−10.7 MHz

Tuning functions

(1) Auto tuning (UP direction sawtooth wave mode)
- Scan ..... Reception for five seconds at a time with frequency display flashing ON and OFF during reception.
- Seek ..... Station held once it has been tuned

(2) Manual tuning (sawtooth wave mode)
- Manual UP (MU), Manual Down (MD) ..... Stepwise increment/decrement by momentary switch, or if depressed for more than 0.5 seconds, rapid scanning until switch is released.

(3) Preset station memory call ..... Six stations in each band
- Preset station display ..... Dot display (LED) or 7-segment numerical display (FIP/LCD) selected by setting the DOT/$\overline{SEG}$ pin (pin 32) of μPD6320G/μPD6321G to high or low level.

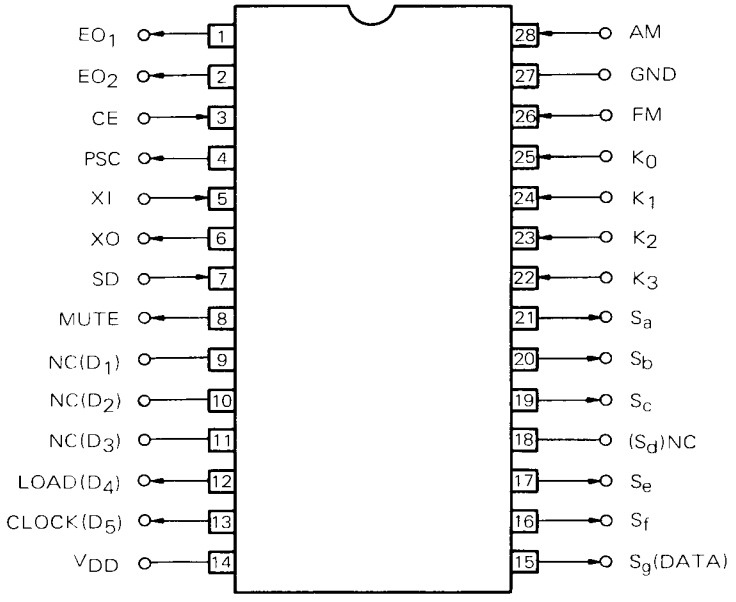
(4) Last station memory ..... One station in each band

Clock functions

(1) 12-hour display (with AM/PM display)

(2) Hour and minute setting functions

PIN CONFIGURATION (Top View)



NC (No Connection)

PIN DESCRIPTION

PIN NO.	PIN SYMBOL	PIN NAME	DESCRIPTION
1 2	EO_1 EO_2	E ror out	PLL phase detector charge pump outputs. A high level output obtained from these pins if the frequency obtained by dividing the oscillator frequency is higher than the reference frequency, and a low level output is obtained if the divided oscillator frequency is lower. Since the same output signal is obtained from both EO_1 and EO_2, either pin may be connected to the L.P.F.
3	CE	Chip enable	Device selector signal input pin. Pin is set to high level for normal device operation, and to low level when device is not being used. High level . . . . . Normal operation Low level . . . . . Display OFF, PLL operation halted, clock operation continued, memory maintained Note that neither high nor low level pulses of less than 134 μs are accepted.
4	PSC	Pulse swallow control	Output of signal for switching the prescalar frequency division factor for FM reception where pulse swallow is used as the frequency division method. Connect to PSC pin of the μPB553AC dedicated prescalar via capacitor and resistor elements. The switchable μPB553AC frequency division factors are 1/16 and 1/17.
5 6	XI XO	X'tal	Crystal oscillator connector pins. Connect to a 4.5 MHz crystal oscillator.
7	SD	Station detector	Stop signal input pin used in auto tuning. Apply a high level input signal with 45 msec after locking the PLL.
8	MUTE	MUTE output	Active high output pin used to eliminate shock noise when the PLL lock is disrupted. See the MUTE output timing chart for details.
9 to 11	NC (D_1 to D_3)	(Digit out)	Make no connections to these pins since they are not used in μPD1701C-015.
12	LOAD (D_4)	LOAD	Display data latch output to the μPD6320G/μPD6321G display driver. Connect directly to the μPD6320G/μPD6321G LOAD pin. See the section on display data for details.
13	CLOCK (D_5)	Clock out	Clock signal output used in transfer of display data to the μPD6320G/μPD6321G display driver. Connect directly to the μPD6320G/μPD6321G CLOCK pin. Data passed to μPD6320G/μPD6321G is shifted at the leading edge of this clock signal.
14	V_{DD}	V_{DD}	Device power supply pin (+5 V ±10 %). The V_{DD} rise time must be less than 500 ms. The device may not be correctly initialized if the rise time is very long.
15 to 21	S_a to S_g	Key source	Signal source for key matrix scanning (active high). In addition to key matrix scanning, the S_g pin also supplies display data to the μPD6320G/μPD6321G display driver. See the section on display data for details. Note that S_d is not used.

PIN NO.	PIN SYMBOL	PIN NAME	DESCRIPTION
22 to 25	K_0 to K_3	Key return signal input	Input pins for key return signals from external key matrix. (See section on key matrix configuration on page 8.)
26	FM	FM VCO signal input	Input of the μPB553AC prescalar outputs obtained by dividing the FM local oscillator frequency by 16 or 17. Because of the built-in AC amplifier, eliminate the DC components of the input by capacitor.
27	GND	GND	Connect to system ground.
28	AM	AM VCO signal input	Input of the AM local oscillator output. Because of the built-in AC amplifier, eliminate the DC components of the input by capacitor.

CONTENTS

1. KEY MATRIX

1.1 CONFIGURATION OF KEY MATRIX

OUTPUT \ INPUT	K_0 (25)	K_1 (24)	K_2 (23)	K_3 (22)
S_a (21)	RCAL	ME (TIME SET)	MD (HOUR)	MU (MINUTE)
S_b (20)	M4	M3	M2	M1
S_c (19)	M6	M5	SEEK	SCAN
S_d (18)				
S_e (17)	AM/FM		B	A
S_f (16)		9 k/10 k		P
S_g (15)	100 k/200 k	JPN/USA		

Figures in parentheses indicate pin nos.

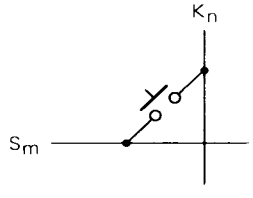
: Momentary switch

: Alternate switch

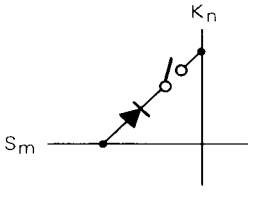
: Initialization diode matrix (shorted or opened by diode)

1.2 SWITCH CONNECTIONS

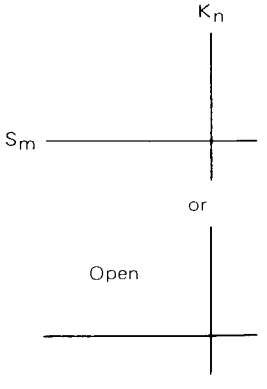
Momentary switch



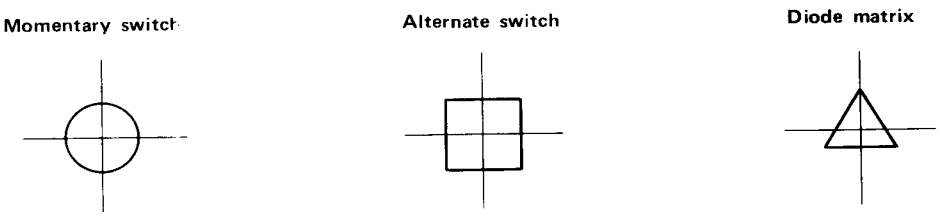
Alternate switch

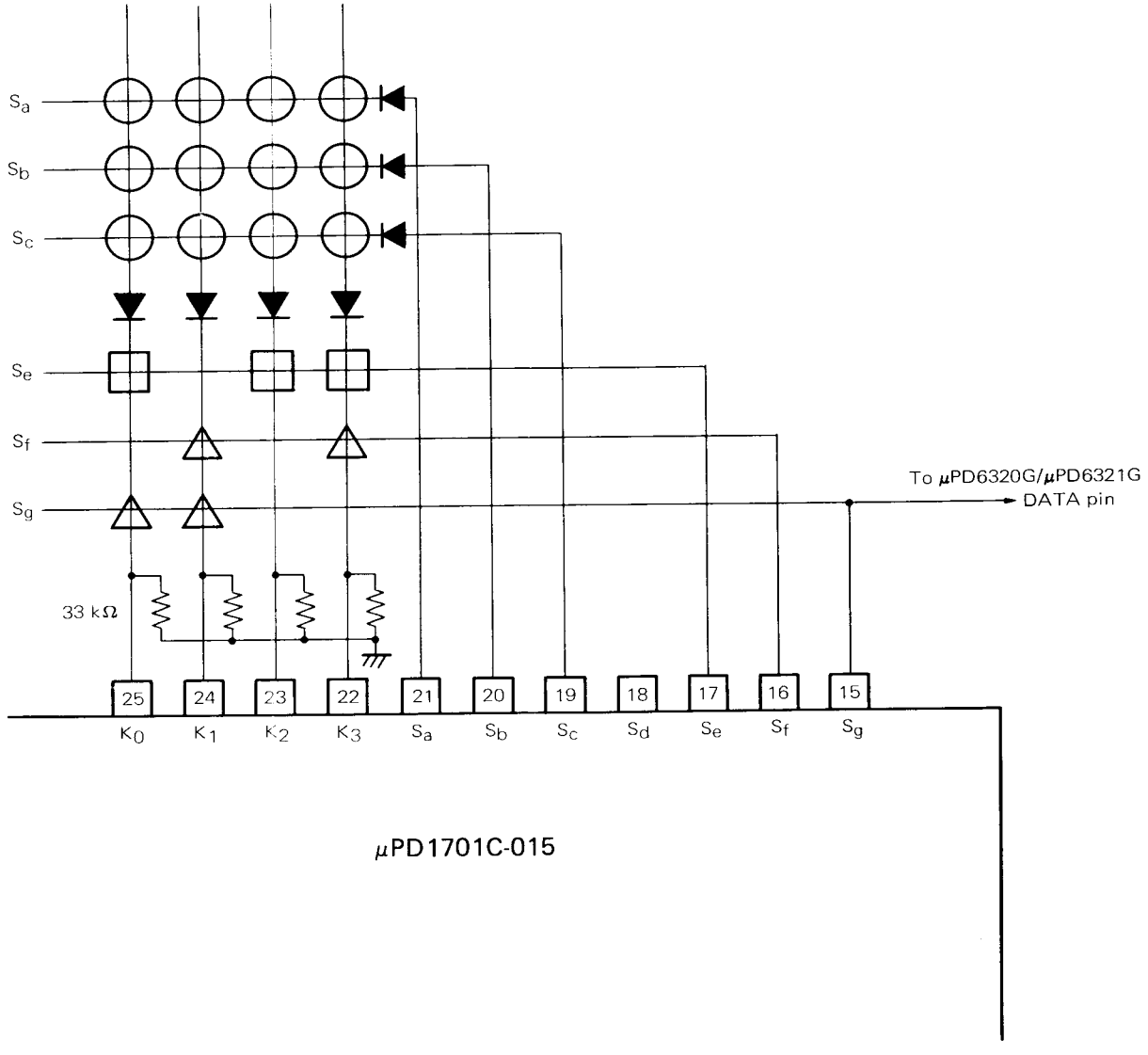


Diode matrix



1.3 EXAMPLES OF KEY MATRIX CONNECTIONS





μPD1701C-015

2. DESCRIPTION OF KEY MATRIX

2.1 INITIALIZATION DIODE MATRIX

The initialization diode matrix status is read only when the power is switched on and when the CE pin status is changed from low to high level. The matrix status is disregarded at all other times. This status is set by shorting or opening matrix intersections by diode.

(In the following table, "1" denotes diode short and "0" denotes open.)

<table>
<tr><th>SYMBOL</th><th>FUNCTION</th></tr>
<tr><td>P</td><td>P (Priority) is the display priority selector switch. Priority can be set when the display mode setting switch A is ON and switch B is OFF. The display reverts to the priority display five seconds after the display change is made.
<table>
<tr><td>A</td><td>B</td><td>P</td><td>Order of priority</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">0</td><td>1</td><td>Frequency priority</td></tr>
<tr><td>0</td><td>Clock priority</td></tr>
</table></td></tr>
<tr><td>JPN/USA</td><td>Selector switch for area setting. This switch is set in combination with the following band setting switches.
<table>
<tr><td>JPN/USA</td><td>Area</td></tr>
<tr><td>1</td><td>Japan</td></tr>
<tr><td>0</td><td>U.S.A.</td></tr>
</table></td></tr>
<tr><td>9 k/10 k</td><td>AM channel band space setting switch when used in the U.S.A. If the area selector switch is set to JPN, the channel space is 9 kHz irrespective of the position of this switch.
<table>
<tr><td>JPN/USA</td><td>9 k/10 k</td><td>Frequency range</td><td>Channel spacing</td><td>Reference frequency</td><td>Intermediate frequency</td></tr>
<tr><td>1</td><td>—</td><td>531 to 1 629 kHz</td><td>9 kHz</td><td>9 kHz</td><td>455 kHz</td></tr>
<tr><td rowspan="2">0</td><td>1</td><td>531 to 1 602 kHz</td><td>9 kHz</td><td>9 kHz</td><td>455 kHz</td></tr>
<tr><td>0</td><td>530 to 1 620 kHz</td><td>10 kHz</td><td>10 kHz</td><td>455 kHz</td></tr>
</table></td></tr>
<tr><td>100 k/200 k</td><td>FM channel band space setting switch when used in the U.S.A. If the country selector switch is set to JPN, the channel space is 100 kHz irrespective of the position of this switch.
<table>
<tr><td>JPN/USA</td><td>100 k/200 k</td><td>Frequency range</td><td>Channel spacing</td><td>Reference frequency</td><td>Intermediate frequency</td></tr>
<tr><td>1</td><td>—</td><td>76.1 to 89.9 MHz</td><td>100 kHz</td><td>25 kHz</td><td>−10.7 MHz</td></tr>
<tr><td rowspan="2">0</td><td>1</td><td>87.9 to 107.9 MHz</td><td>100 kHz</td><td>25 kHz</td><td>10.7 MHz</td></tr>
<tr><td>0</td><td>87.9 to 107.9 MHz</td><td>200 kHz</td><td>25 kHz</td><td>10.7 MHz</td></tr>
</table></td></tr>
</table>

2.2 ALTERNATE SWITCHES

AM/FM

Band selector switch

AM/FM	Reception band
1	AM band
0	FM band

A, B

Display mode setting switches. The four modes are set by combined setting of the A and B switches.

A	B	Display mode	Display priority	Operation	Input enabled switches
0	0	Clock only	—	Clock, memory hold	Time adjustment (ME, MD, MU). A and B switches
1	0	Frequency and clock	Priority display restored after five seconds. (Note 1) Priority determined by P.	All functions operatable	All switches
0	1	Display OFF	—	Clock, memory hold	A and B switches
1	1	Frequency and clock	No priority (Note 2)	All functions operatable	All switches

Note 1.

- Frequency is normally displayed when in frequency priority display mode, but clock time is displayed for five seconds when the [RCAL] key is pressed. Frequency display is restored when the five seconds has elapsed. If the [RCAL] key is pressed a second time or if one of the tuning keys is pressed before the end of the five second interval, the frequency display is restored immediately.
- When in clock time priority display mode, the frequency is displayed for only five seconds if the [RCAL] key is pressed. When scanning frequencies during auto or manual tuning operations, however, the frequency display is maintained for five seconds after completing that tuning operation. And if the [RCAL] key is pressed during a frequency display, the clock time is displayed immediately.

Note 2.

- The five-second timer is disconnected from display switching, the display being changed only when the RCAL or a tuning key, or the AM/FM selector switch is used.

[RCAL] key ..... Display is changed from frequency to clock time, or from clock time to frequency each time this key is pressed.

Tuning key, [AM/FM] ..... If clock time is displayed when one of these keys is pressed, the display is changed to frequency immediately.

Tuning keys include the [MU], [MD], [SCAN], [SEEK], and [M1] to [M6] keys.

2.3 MOMENTARY SWITCHES

SYMBOL	FUNCTION
MU MD	Manual tuning switches MU ..... Manual Up MD ..... Manual Down Frequency is increased/decreased by one channel each time, the MU or MD key is pressed. And if either key is pressed for more than 0.5 second, the frequency is changed at a rate of 45 ms per step until the key is released. And pressing either key together with the ME key enables the time to be adjusted.
M1 to M6	Preset memory switches Each key is equipped with an independent memory for FM and AM. Frequencies preset in these memories can be called by pressing one of the Preset memory keys. And if M keys is pressed within five seconds after pressing the ME key, the current corresponding memory.
ME	When in frequency display mode The ME key is used to store a frequency in one of the preset memories. After tuning to the desired frequency by using the tuning keys (such as MU and MD, press the ME key. Then press one of the M1 to M6 keys within five seconds to store that frequency in the corresponding memory. When in clock display mode The clock time is advanced by one hour each time the MD key is pressed while the ME key is depressed. And if the MD key is pressed for more than 0.5 second, the time is advanced rapidly (4 hours per second). Likewise, the time is advanced by one minute each time the MU key is pressed while the ME key is depressed. If the MU key is pressed for more than 0.5 second, the time is advanced rapidly (4 minutes per second). Note that during this time adjustment, advancing the minutes column does not result in advancement of the hour column, and that the internal seconds counter is reset to zero each time the minutes column is adjusted.
SCAN	The SCAN key is an auto tuning key used in sawtooth wavemode. When this key is pressed, scanning is commenced in the UP direction only. If a high level input is applied to the SD pin during scanning, the frequency at that point is held for five seconds with the frequency display flashing ON and OFF. If the SCAN key is pressed again during that five second interval, the frequency remains held. If on the other hand, no switch at all is pressed during that five second interval, scanning is recommended. If another key is pressed during scanning, the scanning is stopped and the operation specified by the pressed key is commenced.
SEEK	The SEEK key is an auto tuning key used in sawtooth wave mode. When this key is pressed, seeking is commenced in the UP direction only. The only point in which the seek operation differs from scanning is that held when a high level input is applied to the SD pin during auto tuning.
RCAL	The RCAL key is used to change frequency and clock displays. The display is changed each time the key is pressed.

3. DISPLAY

3.1 DISPLAY DATA

The μPD1701C-015 device s only used in static displays. The DATA output signal is obtained from the S_9 pin, the CLOCK output signal is obtained from the D_5 pin, and the LOAD signal is obtained from the D_4 pin. These three outputs are connected to the respective DATA, CLOCK, and LOAD pins of the μPD6320G/μPD6321G (FIP/LCD static display driver (see the circuit diagram examples).

The DATA signal output is obtained serially one bit at a time in the sequence indicated in Table 1.

Table 1 DATA signal output ranking and display contents

Output ranking	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Bit weight	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1
Display data	*	:	DP	kHz	‖	**	MHz	ME	AM	FM	PM	AM	7-segment decoder 10 MHz (FM) 100 kHz (AM)				7-segment decoder 1 MHz (FM) 10 kHz (AM)				7-segment decoder 0.1 MHz (FM) 1 kHz (AM)				Preset station display (7-segment display)				Preset station display (LED dot display)			

* Flag D_{12} at output ranking 1 is the bit used to select the "blank display determining data" for the preset station display (7-segment display) at output rankings 25 to 28.

"1" . . . Blank when DATA is 0000B (display is 1 to F)

"0" . . . Blank when DATA is 1111B (display is 0 to E)

Since μPD1701C-015 passes "1" data to flag D_{12}, the blank display is set by 0000B.

The same output data is passed to the LED dot (output ranking 29 to 32) and 7-segment (output ranking 25 to 28) preset station displays. The display type is selected by the μPD6320G/μPD6321G DOT/$\overline{SEG}$ pin.

** Flag D_7 of output ranking 6 is not used. Due to output of 0 data, the display is blank.

CLOCK signal outputs are generated for each bit of DATA signal, and data is shifted into the μPD6320G/μPD6321G internal register synchronized with CLOCK signal rising edges. A LOAD signal output is generated after 32 bits of data have been transferred, and the μPD6320G/μPD6321G shift register contents are latched to the display buffer. The timing for this data transfer is outlined in Figure 2.

Data is transferred from μPD7701C-015 to the μPD6320G/μPD6321G display driver in the following seven cases.

- When the clock minute column is increased (unless in frequency display mode)
- When the display mode is switched by A/B switch
- When in NORMAL status (with no key operation) (5 seconds/time)
- When display is changed by key operation
- When frequency (division factor) is changed
- When SD signal is applied during scanning resulting in the scanning being halted and the display flashed ON and OFF (0.5 second/time)
- When there is no display with mode setting switch A OFF and B ON (125 msec/time)

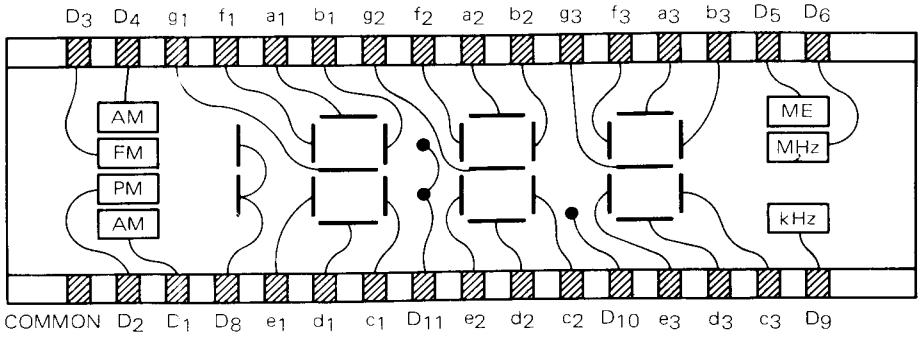


Fig. 1 Display pattern and connection diagram

* Pin names are μPD6320G/μPD6321G pin names.

Refer to the μPD6320G and μPD6321G catalogs for details on the display driver.

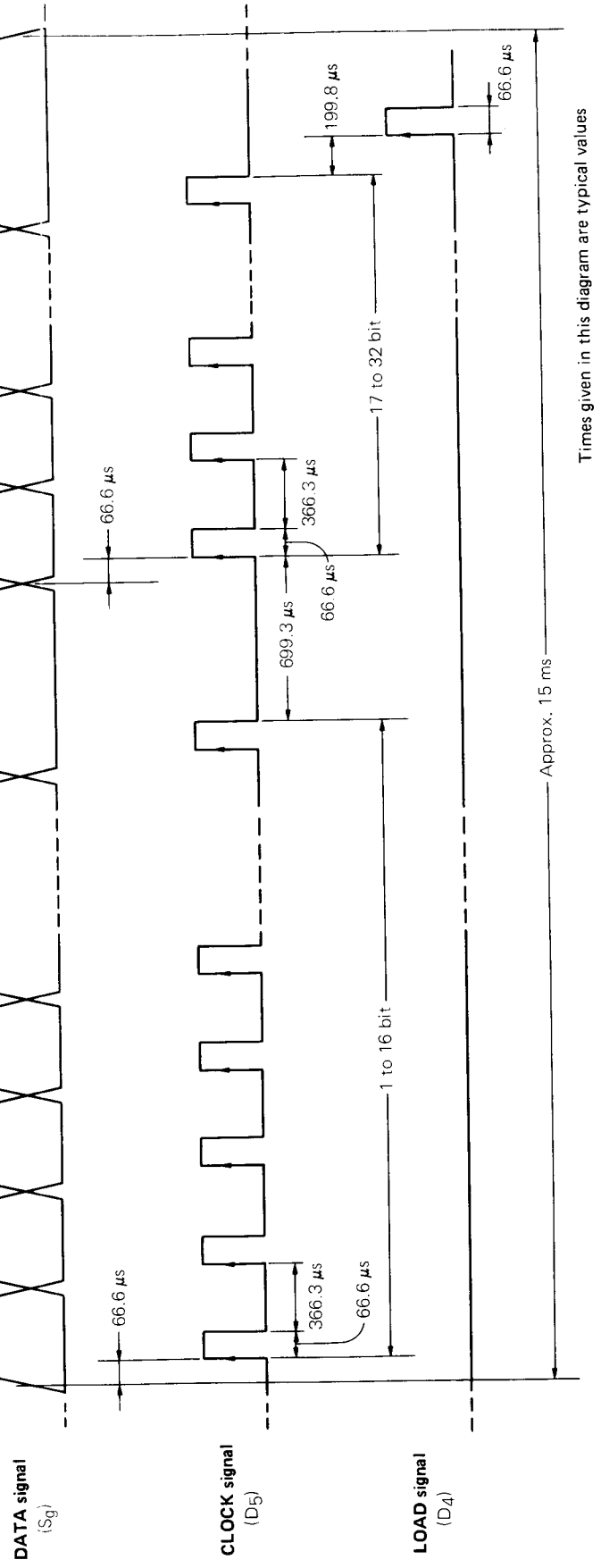


Fig. 2 Static display data transfer timing

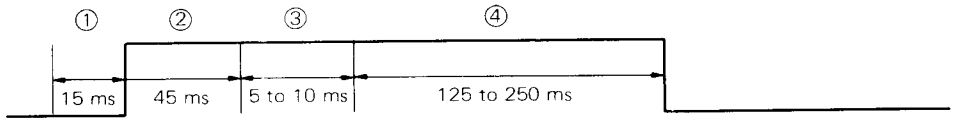
4. TIMING CHARTS

4.1 MUTE OUTPUT TIMING CHART

① Key chattering suppression interval (when key switched on)
② MUTE "first out" interval
③ Change in the frequency division factor setting and display contents
④ MUTE "last out" interval
⑤ Scan time
⑥ PLL Lock time

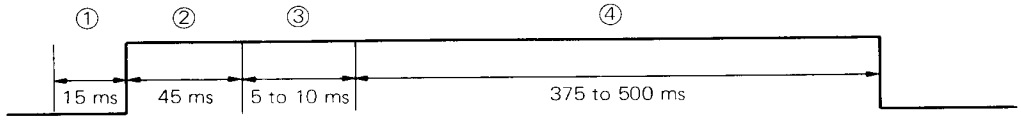
(1) Manual Up and Manual Down

(i) When key is released within 0.5 sec. (except when at edge of band)

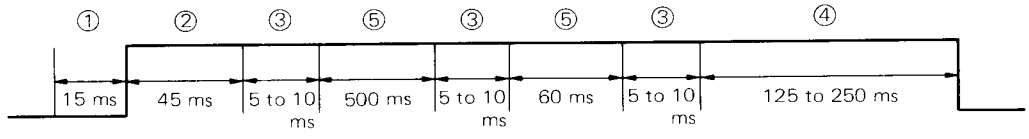


Interval ④ commenced after key is released

(ii) When key is released within 0.5 sec. (at edge of band: High frequency switched to low frequency)



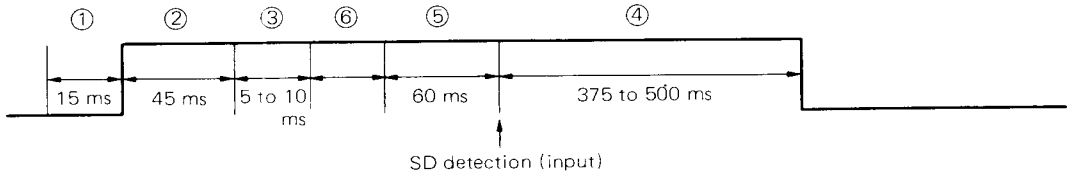
(iii) Key depressed for more than 0.5 sec.



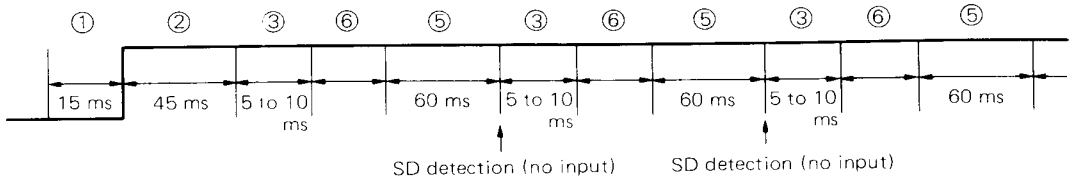
Interval ⑤ becomes 375 to 500 msec. if edge of band is reached.

(2) Seek Up

(i) When SD signal is applied

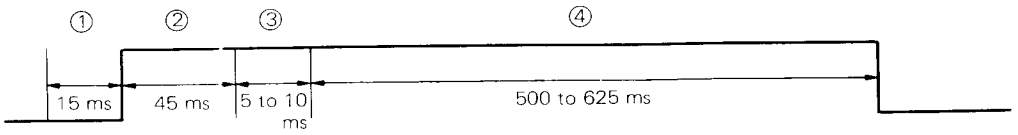


(ii) When SD signal is not applied

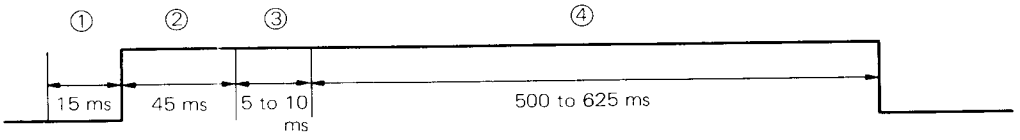


Interval ⑤ becomes 375 to 500 msec. if edge of band is reached.

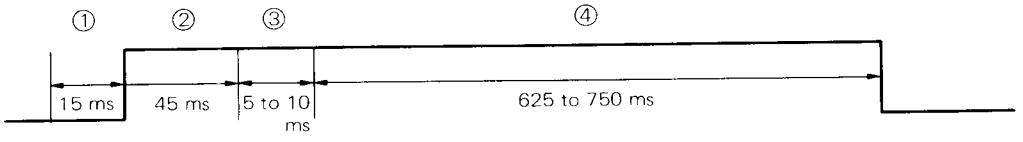
(3) Preset memory call



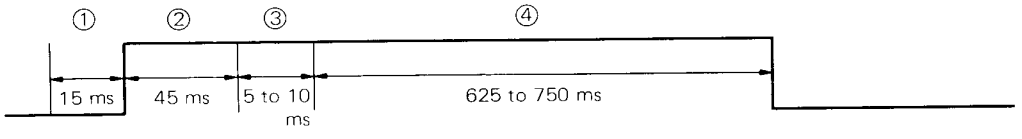
(4) Band switching



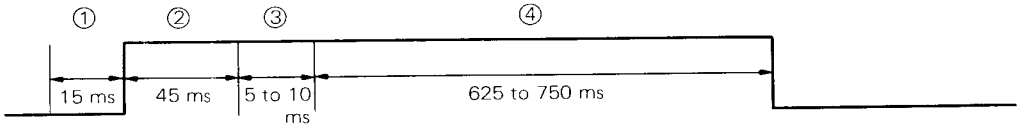
(5) Mode switching



(6) Power ON (CE: Low → High)

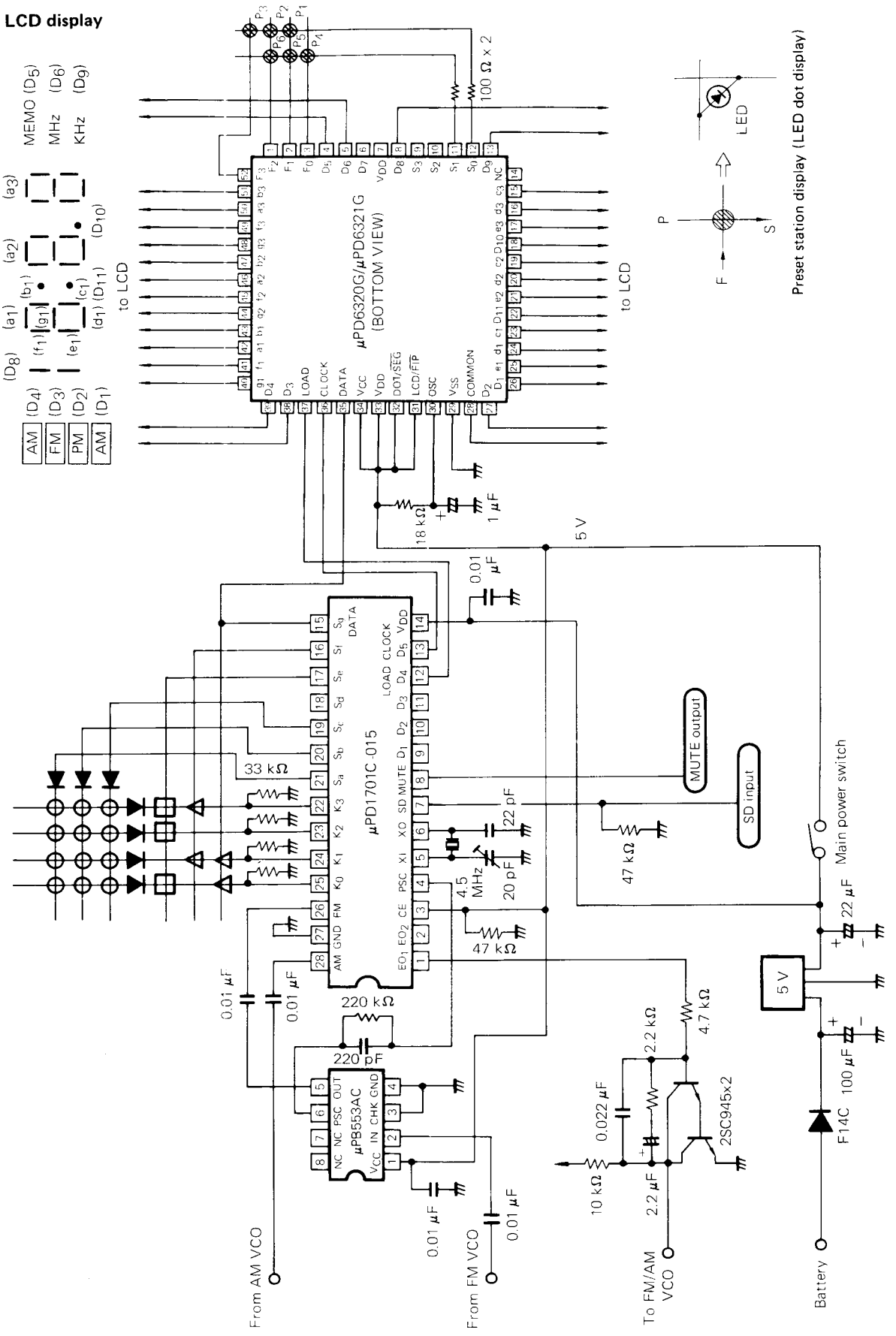


(7) Chip Enable (CE) change from low to high level

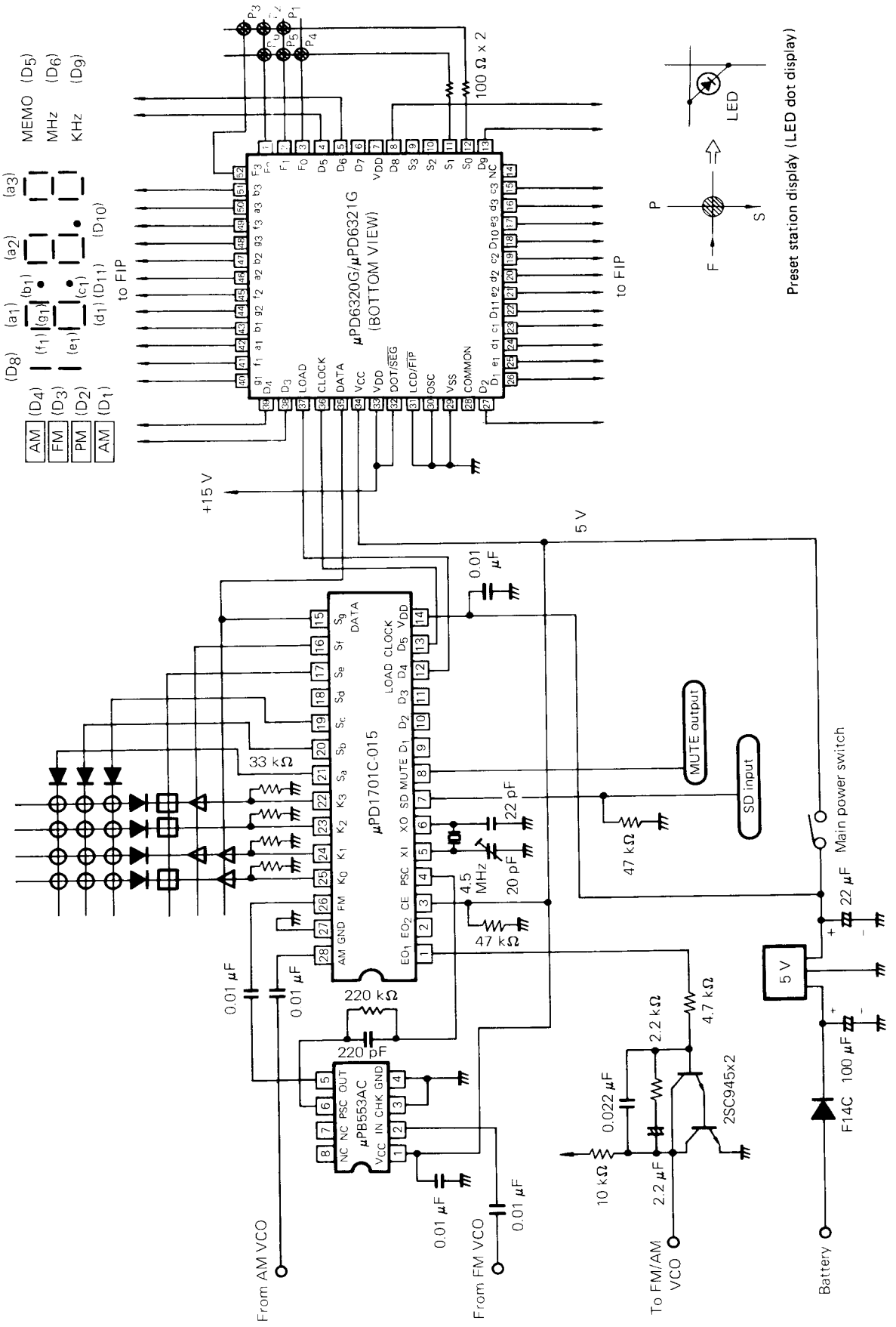


5. APPLICATION CIRCUIT

For LCD display



For FIP display



The practical circuits and circuit constants shown in this manual have not be designed for mass production (where deviation between parts and temperature characteristics must also be considered).

Also note that NEC bears no responsibility in respect to patents related to these circuits.

6. ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Power supply voltage	V_{DD}	−0.3 to +6.0	V
Input voltage	V_I	−0.3 to +V_{DD}	V
Output voltage	V_O	−0.3 to +V_{DD}	V
Output current	I_{OH}	−10	mA
Storage temperature	T_{stg}	−55 to +125	°C

6.2 DC CHARACTERISTICS

(Measuring conditions V_{DD} = 4.5 to 5.5 V, T_a = −35 to +75 °C unless specified otherwise)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
High level input voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	SD pin
High level input voltage	V_{IH2}	0.7 V_{DD}		V_{DD}	V	CE pin
High level input voltage	V_{IH3}	0.6 V_{DD}		V_{DD}	V	K_0 to K_3 pins
Low level input voltage	V_{IL1}	0		0.3 V_{DD}	V	CE pin
Low level input voltage	V_{IL2}	0		0.2 V_{DD}	V	SD and K_0 to K_3 pins
High level output voltage	V_{OH1}	4.0			V	PSC pin, I_{OH} = −0.2 mA
High level output voltage	V_{OH2}	4.0			V	EO_1, EO_2, MUTE D_4 & D_5 pins, I_{OH} = −0.5 mA
High level output voltage	V_{OH3}	4.0			V	S_a to S_g pins, I_{OH} = −1.0 mA
Low level output voltage	V_{OL1}			0.5	V	EO_1, EO_2 pins, I_{OL} = 0.5 mA
Low level output voltage	V_{OL2}			0.5	V	MUTE, D_1 to D_5 PSC, S_a to S_g pins, I_{OL} = 0.2 mA
High level input current	I_{IH}	5.0	25	100	μA	K_0 to K_3 pins, V_1 = V_{DD} = 5 V
AC input voltage	V_{in}	1.0		V_{DD}	V_{p-p}	VCOL and VCOH pins
Power supply voltage rise time	t_r			0.5	s	V_{DD} pin, V_{DD}: 0 → 4.5 V
Operating current	I_{DD}		0.5	2.0	mA	Display OFF, PLL operation OFF, clock only operating, V_{DD} = 5 V

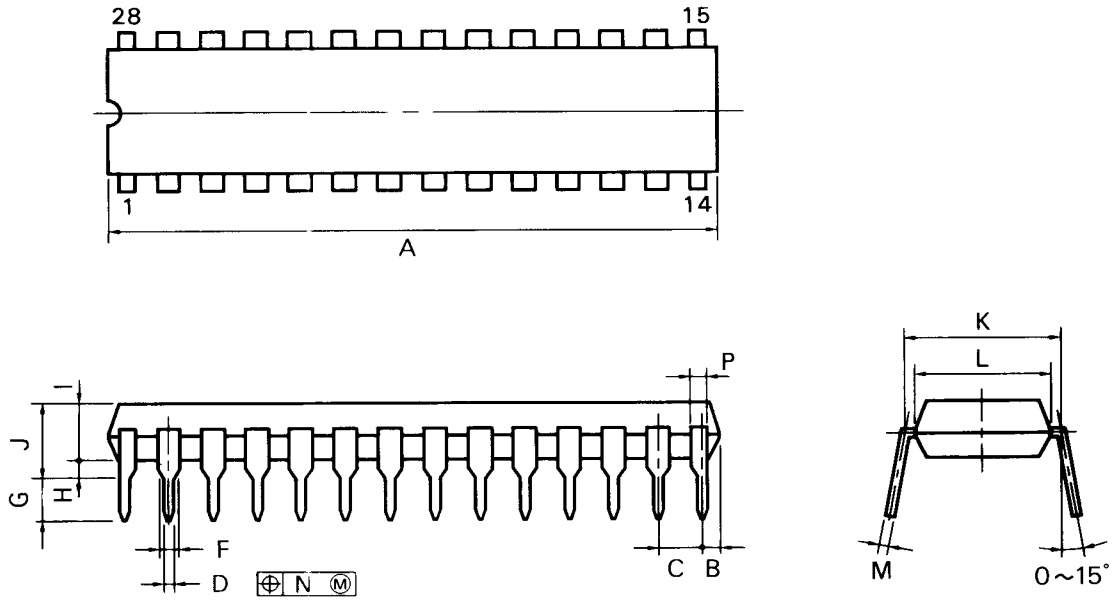
6.3 AC CHARACTERISTICS

(Measuring conditions V_{DD} = 4.5 to 5.5 V, T_a = −35 to +75 °C unless specified otherwise)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Operating frequency	f_{in1}	0.5		2.5	MHz	V_{in} = 1 V_{p-p}, AM pin, DC cut, sine wave
Operating frequency	f_{in2}	0.5		8.8	MHz	V_{in} = 0.8 V_{p-p}, FM pin, DC cut, square wave

7. PACKAGE DIMENSIONS (unit: mm)

28PIN PLASTIC DIP (400 mil)



P28C-100-400

NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	35.56 MAX.	1.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	3.5 ± 0.3	0.138 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.