NEC

MOS INTEGRATED CIRCUIT
μPD23C128000L

128M-BIT MASK-PROGRAMMABLE ROM
16M-WORD BY 8-BIT (BYTE MODE) / 8M-WORD BY 16-BIT (WORD MODE)

Description

The μPD23C128000L is a 134,217,728 bits mask-programmable ROM. The word organization is selectable (BYTE mode: 16,777,216 words by 8 bits, WORD mode: 8,388,608 words by 16 bits).

The active levels of OE (Output Enable Input) can be selected with mask-option.

The μPD23C128000L is packed in 48-pin plastic TSOP(I).

Features

- Word organization
  - 16,777,216 words by 8 bits (BYTE mode)
  - 8,388,608 words by 16 bits (WORD mode)
- Operating supply voltage : 2.7 to 3.6 V

★

Operating supply voltage V_{CC}	Access time ns (MAX.)	Power supply current (Active mode) mA(MAX.)	Standby current (CMOS level input) μA(MAX.)
3.3 V ± 0.3 V	110	55	30
3.0 V ± 0.3 V	120	50	30

Ordering Information

Part Number	Package
μPD23C128000LGY-xxx-MJH	48-pin Plastic TSOP(I)(12 x 18 mm)(Normal bent)
μPD23C128000LGY-xxx-MKH	48-pin Plastic TSOP(I)(12 x 18 mm)(Reverse bent)

(xxx: ROM code suffix No.)

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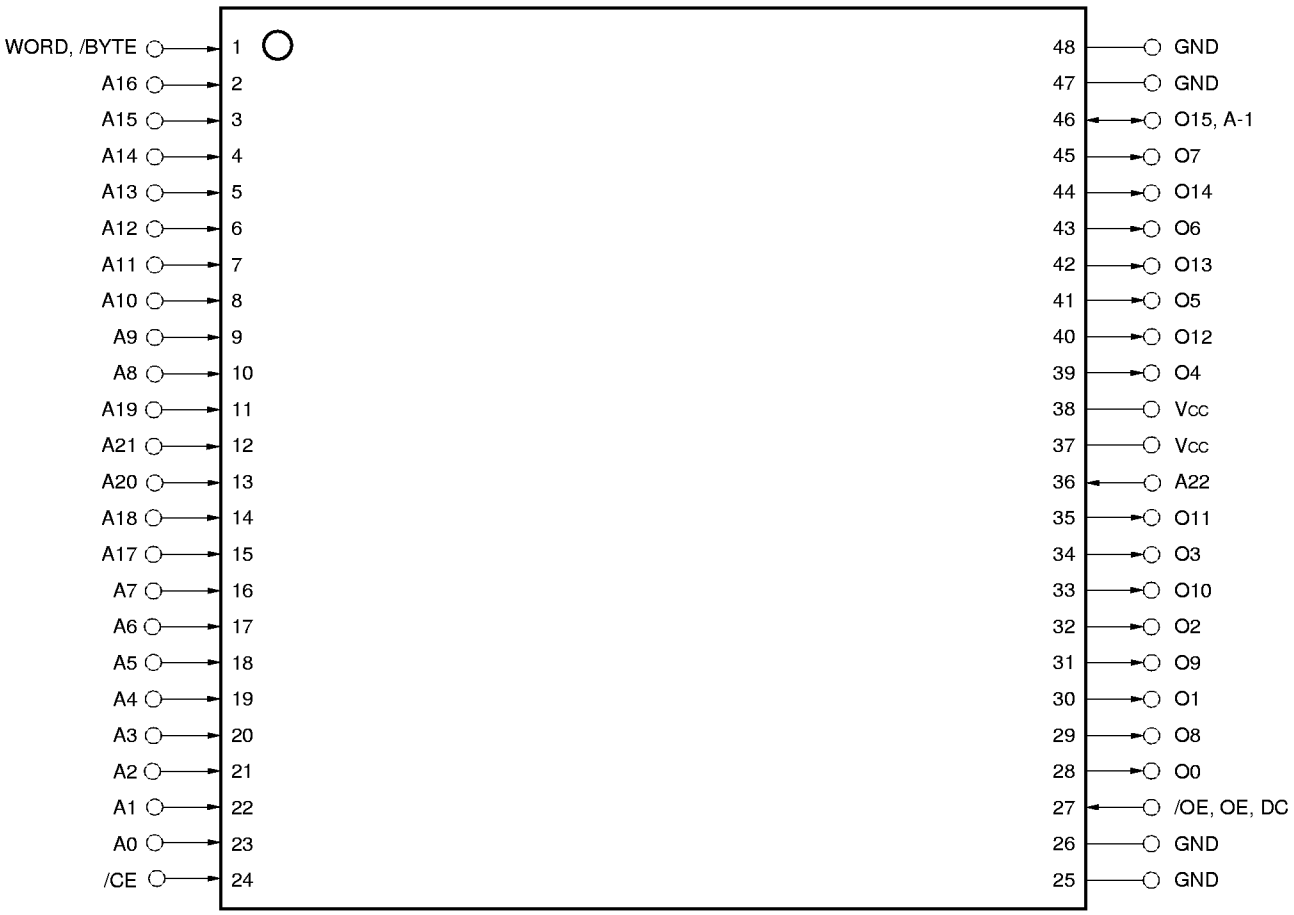
The mark ★ shows major revised points.

Pin Configuration (Marking Side)

/xxx indicates active low signal.

48-pin plastic TSOP(I) (12 x 18 mm) (Normal bent)

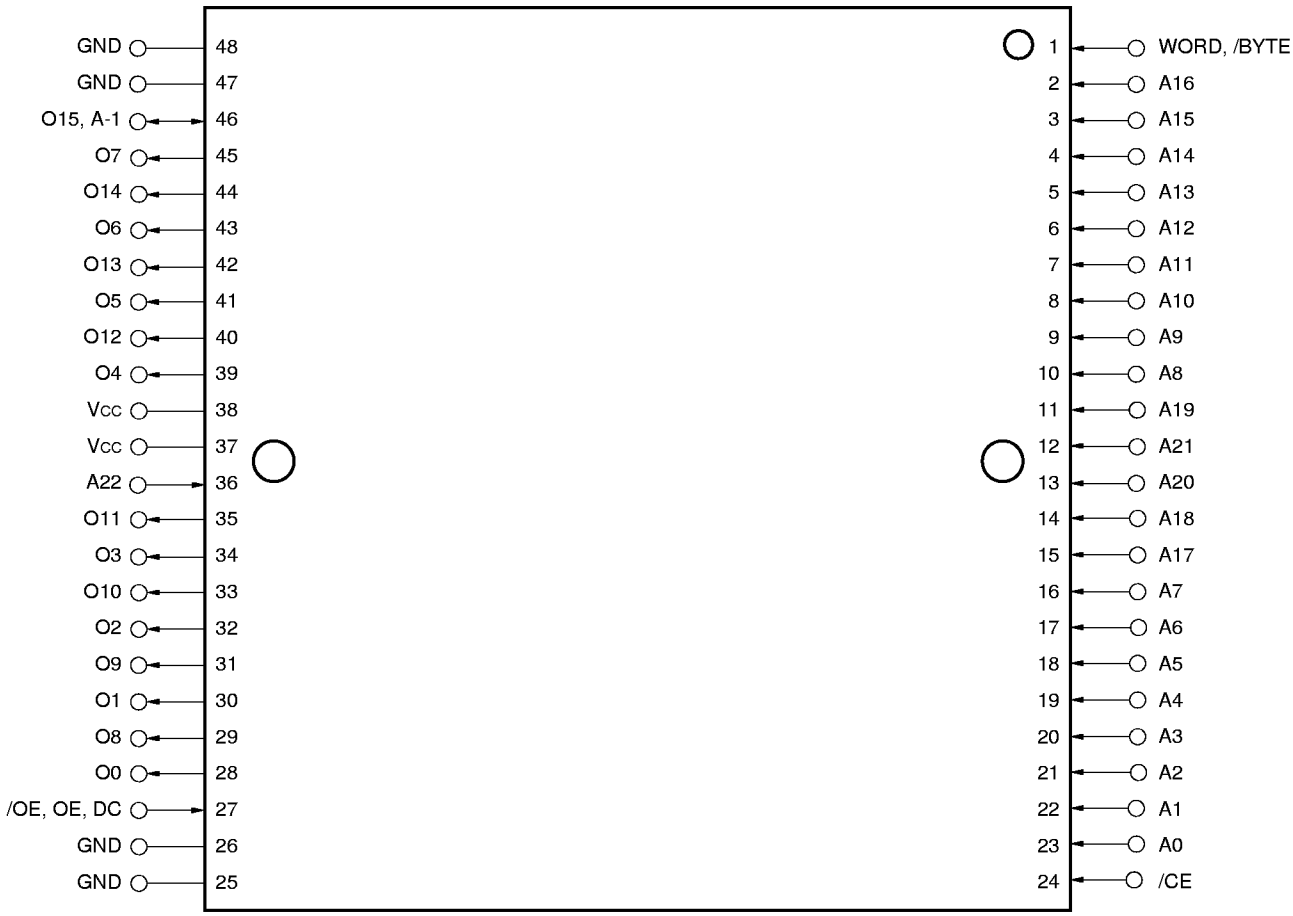
[μPD23C128000LGY-xxx-MJH]



A0 - A22	:	Address inputs
O0 - O7, O8 - O14	:	Data outputs
O15, A–1	:	Data 15 output(WORD mode), LSB address input(BYTE mode)
WORD, /BYTE	:	Mode select
/CE	:	Chip Enable
/OE, OE	:	Output Enable
Vcc	:	Supply voltage
GND	:	Ground
DC	:	Don't Care

48-pin plastic TSOP(I) (12 x 18 mm) (Reverse bent)

[μPD23C128000LGY-xxx-MKH]

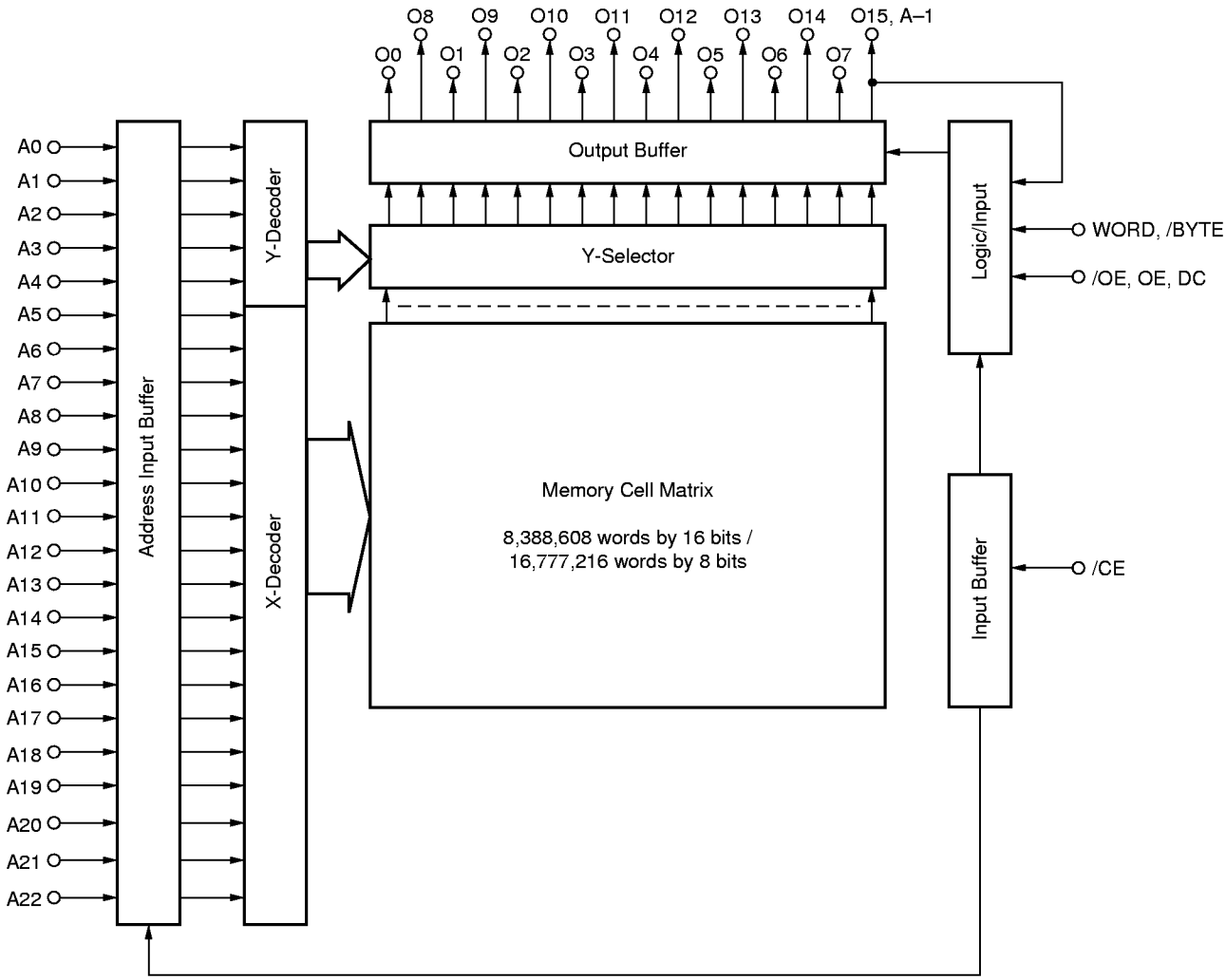


A0 - A22	:	Address inputs
O0 - O7, O8 - O14	:	Data outputs
O15, A–1	:	Data 15 output(WORD mode), LSB address input(BYTE mode)
WORD, /BYTE	:	Mode select
/CE	:	Chip Enable
/OE, OE	:	Output Enable
VCC	:	Supply voltage
GND	:	Ground
DC	:	Don't Care

Input/Output Pin Functions

Pin name	Input/Output	Function
WORD, /BYTE	Input	The pin for switching BYTE mode and WORD mode. **High level** : WORD mode (8M-word by 16-bit) **Low level** : BYTE mode (16M-word by 8-bit)
★ A0 to A22 (Address inputs)		Address input pin. A0 to A22 are used differently in the WORD mode and the BYTE mode. **WORD mode (8M-word by 16-bit)** A0 to A22 are used as 23 bits address signals. **BYTE mode (16M-word by 8-bit)** A0 to A22 are used as the upper 23 bits of total 24 bits of address signal. (The least significant bit (A–1) is combined to O15.)
★ O0 to O7, O8 to O14 (Data output)	Output	Data output pin. O0 to O7, O8 to O14 are used differently in the WORD mode and the BYTE mode. **WORD mode (8M-word by 16-bit)** The lower 15 bits of 16 bits data outputs to O0 to O14. (The most significant bit (O15) combined to A–1.) **BYTE mode (16M-word by 8-bit)** 8 bits data outputs to O0 to O7 and also O8 to O14 are high impedance.
O15, A–1 (Data output 15) , (LSB Address input)	Output, Input	O15, A–1 are used differently in the WORD mode and the BYTE mode. **WORD mode (8M-word by 16-bit)** The most significant output data bus (O15). **BYTE mode (16M-word by 8-bit)** The least significant address bus (A–1).
/CE (Chip Enable)	Input	Chip activating signal. When the OE is active, output states are following. **High level** : High impedance **Low level** : Data out
/OE, OE, DC (Output Enable)	Input	Output enable signal. The active level of OE is mask option. The active level of OE can be selected from high active, low active and Don't care at order.
V_{CC}	–	Supply voltage
GND	–	Ground

Block Diagram



Mask Option

The active levels of output enable pin (/OE, OE, DC) are mask programmable and optional, and can be selected from among " 0 " " 1 " " x " shown in the table below.

Option	/OE, OE, DC	OE active level
0	/OE	L
1	OE	H
x	DC	Don't care

Operation modes for each option are shown in the tables below.

Operation mode (Option: 0)

/CE	/OE	Mode	Output state
L	L	Active	Data out
	H		High impedance
H	H or L	Standby	High impedance

Operation mode (Option: 1)

/CE	OE	Mode	Output state
L	L	Active	High impedance
	H		Data out
H	H or L	Standby	High impedance

Operation mode (Option: x)

/CE	DC	Mode	Output state
L	H or L	Active	Data out
H	H or L	Standby	High impedance

Remark L: Low level input
H: High level input

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.3 to +4.6	V
Input voltage	V_I		–0.3 to V_{CC}+0.3	V
Output voltage	V_O		–0.3 to V_{CC}+0.3	V
Operating ambient temperature	T_A		–10 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Capacitance (T_A = 25 °C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz			10	pF
Output capacitance	C_O				12	pF

DC Characteristics (T_A = –10 to +70 °C, V_{CC} = 2.7 to 3.6 V)

	Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
★	High level input voltage	V_{IH}			2.2		V_{CC} + 0.3	V
	Low level input voltage	V_{IL}	V_{CC} = 3.0 V ± 0.3 V		–0.3		+0.5	V
			V_{CC} = 3.3 V ± 0.3 V		–0.3		+0.8	
	High level output voltage	V_{OH}	I_{OH} = –100 μA		2.4			V
	Low level output voltage	V_{OL}	I_{OL} = 2.1 mA				0.4	V
	Input leakage current	I_{LI}	V_I = 0 V to V_{CC}		–10		+10	μA
	Output leakage current	I_{LO}	V_O = 0 V to V_{CC}, Chip deselected		–10		+10	μA
★	Power supply current	I_{CC1}	/CE = V_{IL} (Active mode),	V_{CC} = 3.0 V ± 0.3 V			50	mA
			I_O = 0 mA	V_{CC} = 3.3 V ± 0.3 V			55	
	Standby current	I_{CC3}	/CE = V_{CC} – 0.2 V (Standby mode)				30	μA

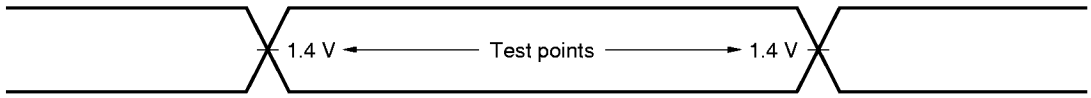
AC Characteristics (T_A = –10 to +70 °C, V_{CC} = 2.7 to 3.6 V)

	Parameter	Symbol	Test condition	V_{CC} = 3.0 V ± 0.3 V			V_{CC} = 3.3 V ± 0.3 V			Unit
				MIN.	TYP.	MAX.	MIN	TYP.	MAX.	
★	Address access time	t_{ACC}				120			110	ns
★	Chip enable access time	t_{CE}				120			110	ns
	Output enable access time	t_{OE}				40			30	ns
	Output hold time	t_{OH}		0			0			ns
	Output disable time	t_{DF}		0		30	0		25	ns
★	WORD, /BYTE access time	t_{WB}				120			110	ns

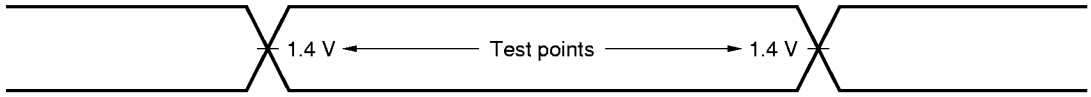
Remark t_{DF} is the time from inactivation of /CE or /OE, OE to high-impedance state output.

AC Test Conditions

Input waveform (Rise/Fall time ≤ 5 ns)



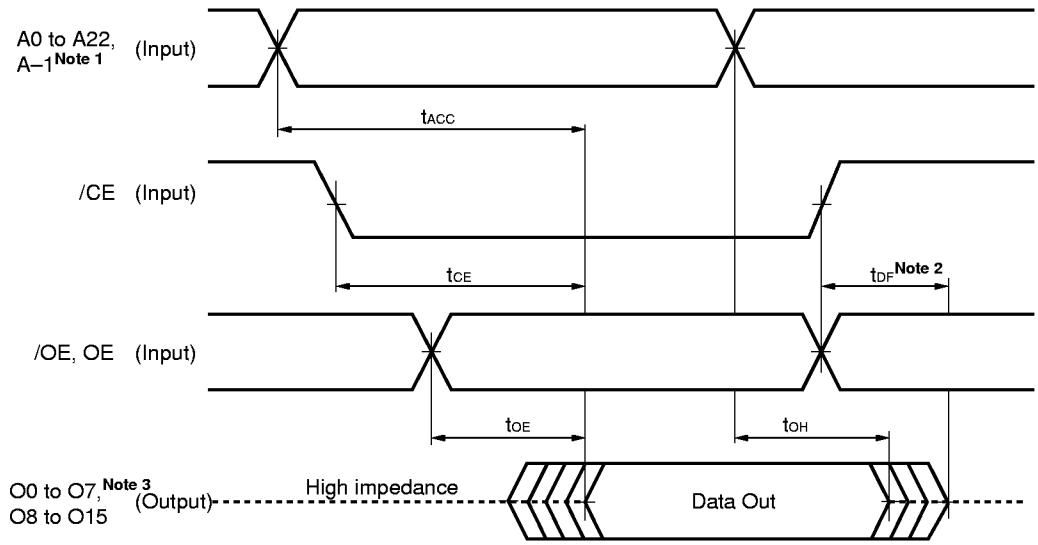
Output waveform



Output load

1TTL + 100 pF

Read Cycle Timing Chart

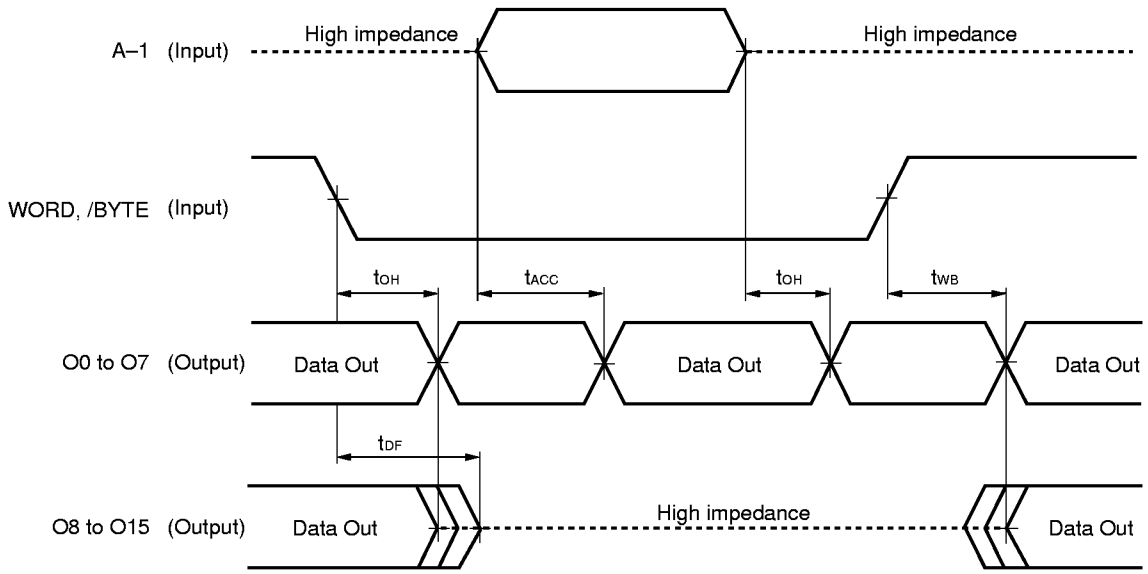


Notes 1. During WORD mode, A–1 is O15.

2. t_{DF} is specified when one of /CE, /OE, OE is inactivated.

3. During BYTE mode, O8 to O14 are high impedance and O15 is A–1.

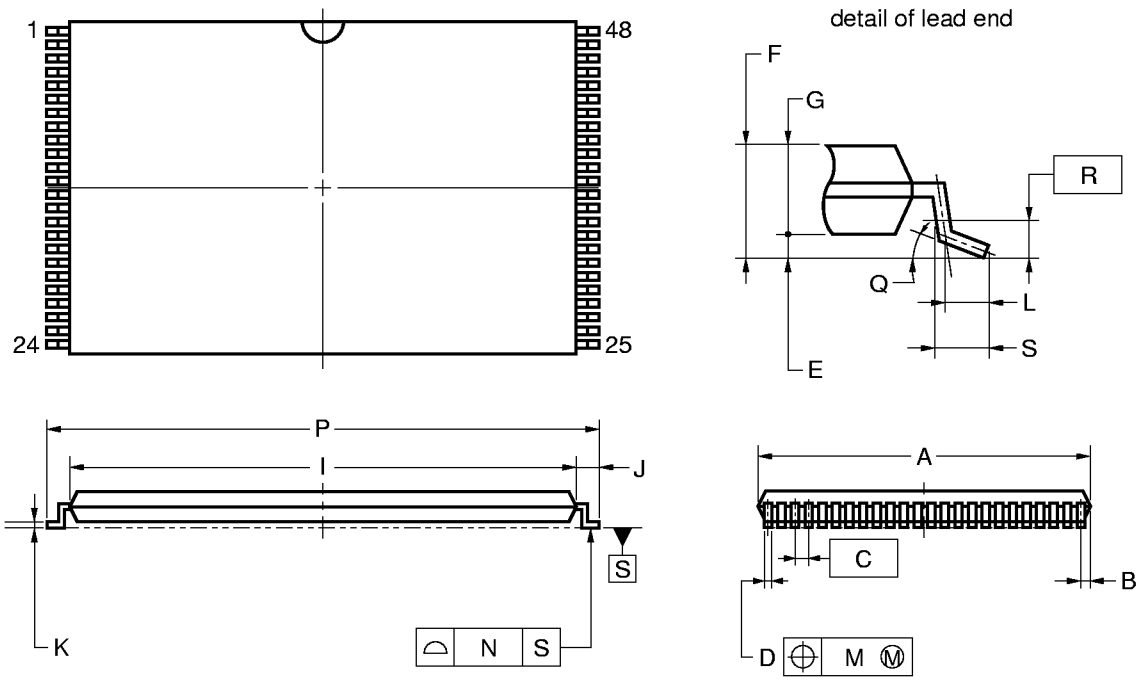
WORD, /BYTE Switch Timing Chart



Remark /OE, OE and /CE : Active.

Package Drawings

48 PIN PLASTIC TSOP (I) (12×18)



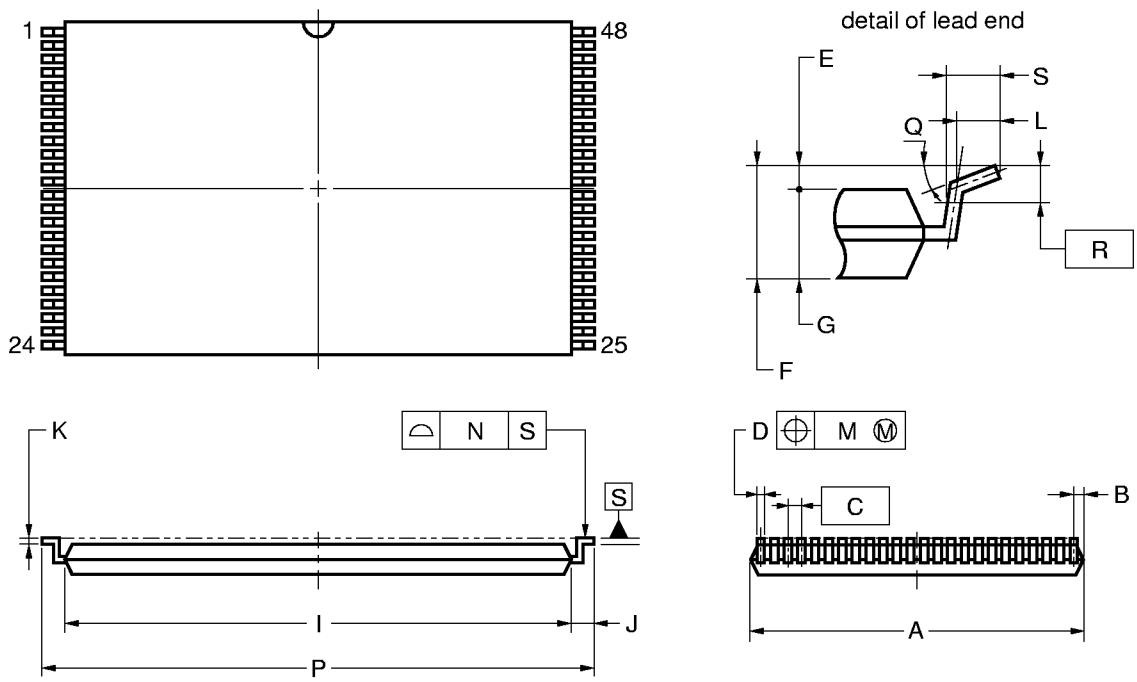
NOTES

1. Controlling dimension —— Millimeter.
2. Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.
3. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX. <0.489 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	12.0±0.1	$0.472^{+0.005}_{-0.004}$
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.22±0.05	$0.009^{+0.002}_{-0.003}$
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	1.0±0.05	$0.039^{+0.003}_{-0.002}$
I	16.4±0.1	$0.646^{+0.004}_{-0.005}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	0.145±0.05	$0.006^{+0.002}_{-0.003}$
L	0.5	0.020
M	0.10	0.004
N	0.10	0.004
P	18.0±0.2	$0.709^{+0.008}_{-0.009}$
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25	0.010
S	0.60±0.15	$0.024^{+0.006}_{-0.007}$

S48GY-50-MJH1

48 PIN PLASTIC TSOP (I) (12×18)



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R	0.25	0.010
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S48GY-50-MKH1

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD23C128000L.

Types of Surface Mount Device

μPD23C128000LGY-MJH : 48-pin plastic TSOP(I)(12 x 18 mm)(Normal bent)

μPD23C128000LGY-MKH : 48-pin plastic TSOP(I)(12 x 18 mm)(Reverse bent)