

### 128M-BIT MASK-PROGRAMMABLE ROM 16M-WORD BY 8-BIT (BYTE MODE) / 8M-WORD BY 16-BIT (WORD MODE) PAGE ACCESS MODE

#### Description

The  $\mu$ PD23C128040L is a 134,217,728 bits mask-programmable ROM. The word organization is selectable (BYTE mode : 16,777,216 words by 8 bits, WORD mode : 8,388,608 words by 16 bits).

The active levels of OE (Output Enable Input) can be selected with mask-option.

The  $\mu$ PD23C128040L is packed in 48-pin plastic TSOP(I).

#### Features

- Word organization  
16,777,216 words by 8 bits (BYTE mode)  
8,388,608 words by 16 bits (WORD mode)
- Page access mode  
BYTE mode : 8 byte random page access  
WORD mode : 4 word random page access
- Operating supply voltage :  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

Operating supply voltage $V_{CC}$	Access time / Page access time ns (MAX.)	Power supply current (Active mode) mA (MAX.)	Standby current (CMOS level input) $\mu$ A (MAX.)
3.3 V $\pm$ 0.3 V	100 / 30	70	30

#### Ordering Information

Part Number	Package
$\mu$ PD23C128040LGY-xxx-MJH	48-pin Plastic TSOP(I) (12 x 18) (Normal bent)
$\mu$ PD23C128040LGY-xxx-MKH	48-pin Plastic TSOP(I) (12 x 18) (Reverse bent)

(xxx : ROM code suffix No.)

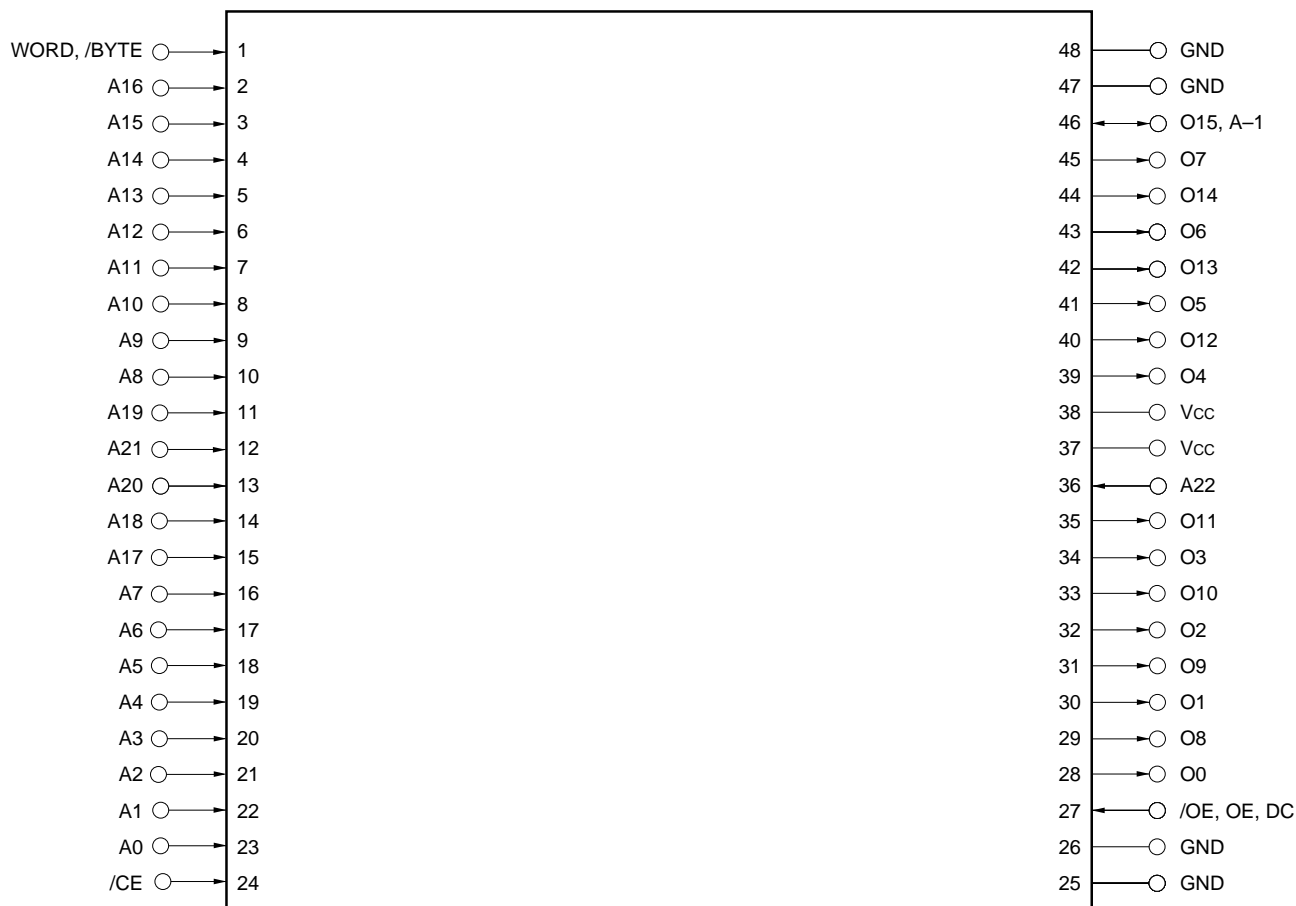
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★ Pin Configurations (Marking Side)

/xxx indicates active low signal.

48-pin plastic TSOP(I) (12 x 18) (Normal bent)

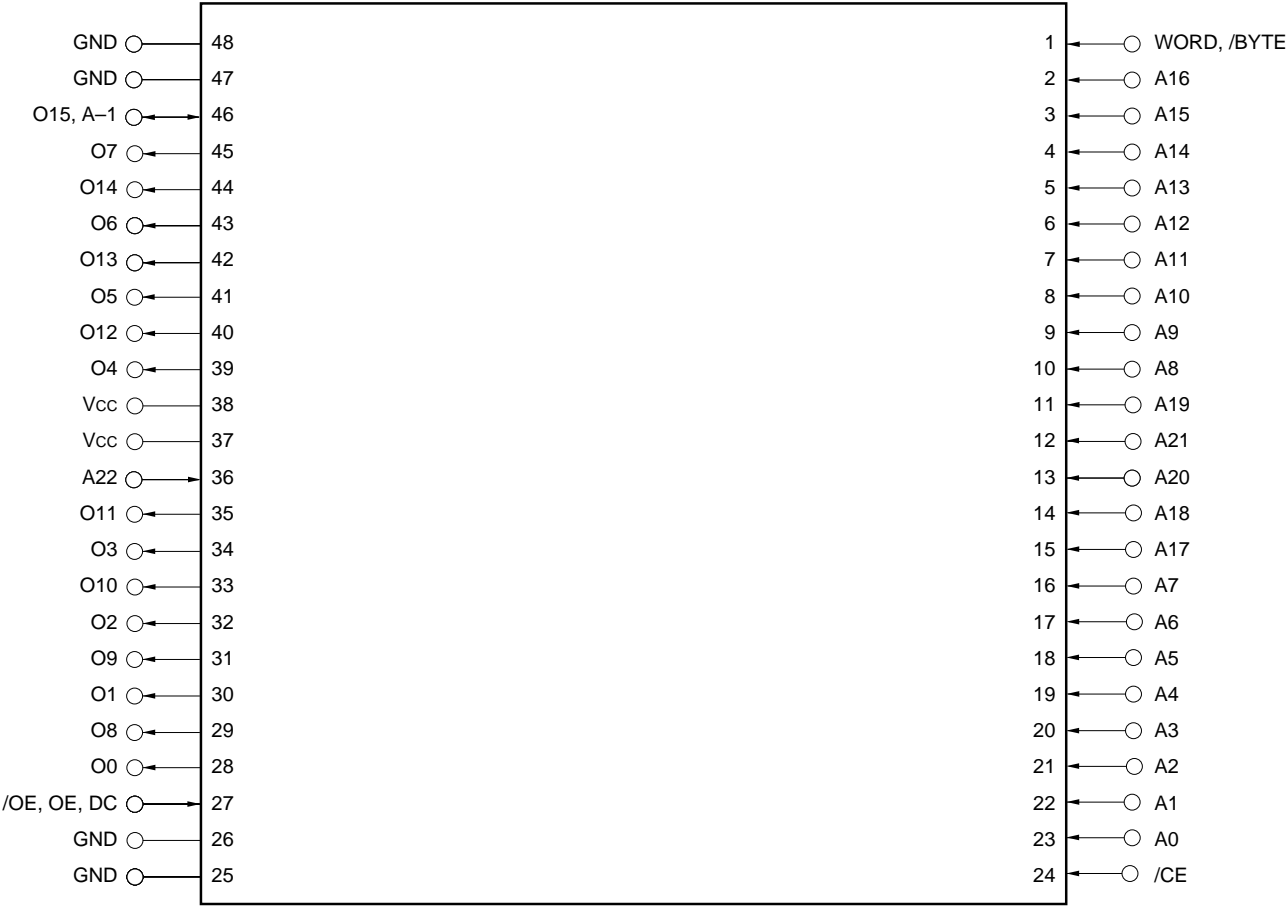
[ μPD23C128040LGY-xxx-MJH ]



A0 - A22	: Address inputs
O0 - O7, O8 - O14	: Data outputs
O15, A-1	: Data output 15 (WORD mode), LSB Address input (BYTE mode)
WORD, /BYTE	: Mode select
/CE	: Chip Enable
/OE, OE	: Output Enable
Vcc	: Supply voltage
GND	: Ground
DC	: Don't Care

**Remark** Refer to **Package Drawings** for the 1-pin index mark.

48-pin plastic TSOP(I) (12 x 18) (Reverse bent)  
[ μPD23C128040LGY-xxx-MKH ]



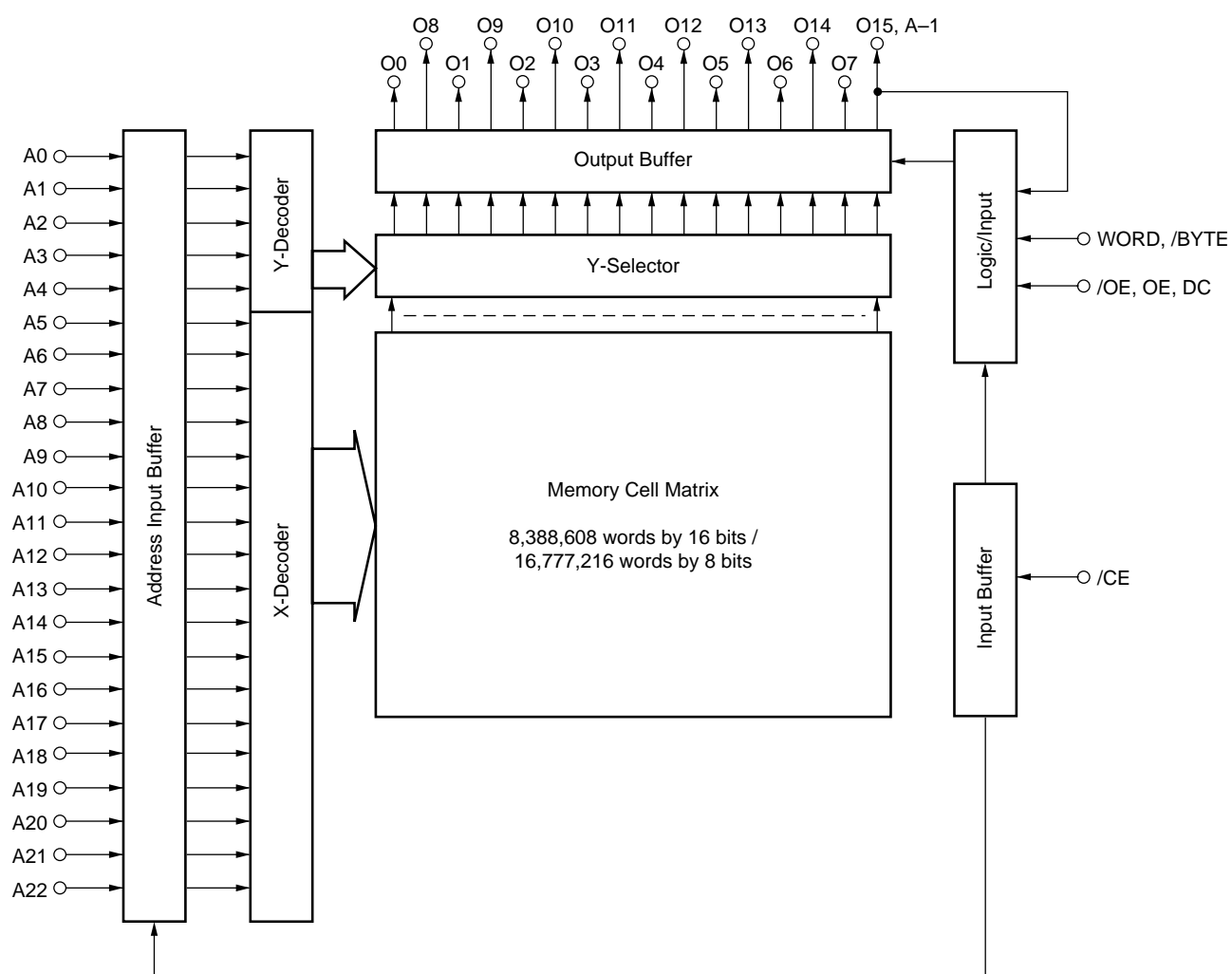
- A0 - A22 : Address inputs
- O0 - O7, O8 - O14 : Data outputs
- O15, A-1 : Data output 15 (WORD mode),  
LSB Address input (BYTE mode)
- WORD, /BYTE : Mode select
- /CE : Chip Enable
- /OE, OE : Output Enable
- Vcc : Supply voltage
- GND : Ground
- DC : Don't Care

**Remark** Refer to **Package Drawings** for the 1-pin index mark.

# Input / Output Pin Functions

Pin name	Input / Output	Function
WORD, /BYTE	Input	The pin for switching WORD mode and BYTE mode. <b>High level</b> : WORD mode (8M-word by 16-bit) <b>Low level</b> : BYTE mode (16M-word by 8-bit)
A0 to A22 (Address inputs)	Input	Address input pins. A0 to A22 are used differently in the WORD mode and the BYTE mode. <b>WORD mode (8M-word by 16-bit)</b> A0 to A22 are used as 23 bits address signals. <b>BYTE mode (16M-word by 8-bit)</b> A0 to A22 are used as the upper 23 bits of total 24 bits of address signal. (The least significant bit (A-1) is combined to O15.)
O0 to O7, O8 to O14 (Data outputs)	Output	Data output pins. O0 to O7, O8 to O14 are used differently in the WORD mode and the BYTE mode. <b>WORD mode (8M-word by 16-bit)</b> The lower 15 bits of 16 bits data outputs to O0 to O14. (The most significant bit (O15) combined to A-1.) <b>BYTE mode (16M-word by 8-bit)</b> 8 bits data outputs to O0 to O7 and also O8 to O14 are high impedance.
O15, A-1 (Data output 15, LSB Address input)	Output, Input	O15, A-1 are used differently in the WORD mode and the BYTE mode. <b>WORD mode (8M-word by 16-bit)</b> The most significant output data bus (O15). <b>BYTE mode (16M-word by 8-bit)</b> The least significant address bus (A-1).
/CE (Chip Enable)	Input	Chip activating signal. When the OE is active, output states are following. <b>High level</b> : High impedance <b>Low level</b> : Data out
/OE, OE, DC (Output Enable, Don't Care)	Input	Output enable signal. The active level of OE is mask option. The active level of OE can be selected from high active, low active and Don't care at order.
Vcc	—	Supply voltage
GND	—	Ground

# Block Diagram



## Mask Option

The active levels of output enable pin (/OE, OE, DC) are mask programmable and optional, and can be selected from among "0" "1" "x" shown in the table below.

Option	/OE, OE, DC	OE active level
0	/OE	L
1	OE	H
x	DC	Don't care

Operation modes for each option are shown in the tables below.

Operation mode (Option : 0)

/CE	/OE	Mode	Output state
L	L	Active	Data out
	H		High impedance
H	H or L	Standby	High impedance

Operation mode (Option : 1)

/CE	OE	Mode	Output state
L	L	Active	High impedance
	H		Data out
H	H or L	Standby	High impedance

Operation mode (Option : x)

/CE	DC	Mode	Output state
L	H or L	Active	Data out
H	H or L	Standby	High impedance

**Remark** L : Low level input

H : High level input

## Electrical Specifications

### Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	$V_{CC}$		-0.3 to +4.6	V
Input voltage	$V_I$		-0.3 to $V_{CC}+0.3$	V
Output voltage	$V_O$		-0.3 to $V_{CC}+0.3$	V
Operating ambient temperature	$T_A$		-10 to +70	°C
Storage temperature	$T_{stg}$		-65 to +150	°C

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### Capacitance ( $T_A = 25^\circ\text{C}$ )

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	$C_I$	$f = 1 \text{ MHz}$			10	pF
Output capacitance	$C_O$				12	pF

### DC Characteristics ( $T_A = -10$ to $+70^\circ\text{C}$ , $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ )

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
High level input voltage	$V_{IH}$		2.2		$V_{CC} + 0.3$	V
Low level input voltage	$V_{IL}$		-0.3		+0.8	V
High level output voltage	$V_{OH}$	$I_{OH} = -100 \mu\text{A}$	2.4			V
Low level output voltage	$V_{OL}$	$I_{OL} = 2.1 \text{ mA}$			0.4	V
Input leakage current	$I_{LI}$	$V_I = 0 \text{ V to } V_{CC}$	-10		+10	$\mu\text{A}$
Output leakage current	$I_{LO}$	$V_O = 0 \text{ V to } V_{CC}$ , Chip deselected	-10		+10	$\mu\text{A}$
Power supply current	$I_{CC1}$	$/\text{CE} = V_{IL}$ (Active mode), $I_O = 0 \text{ mA}$			70	mA
Standby current	$I_{CC3}$	$/\text{CE} = V_{CC} - 0.2 \text{ V}$ (Standby mode)			30	$\mu\text{A}$

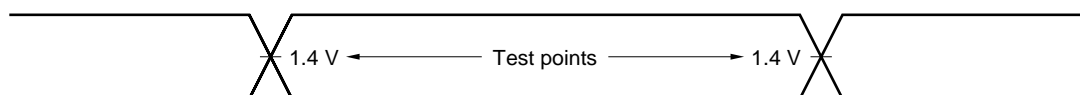
**AC Characteristics ( $T_A = -10$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ )**

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Address access time	$t_{ACC}$				100	ns
Page access time	$t_{PAC}$				30	ns
Chip enable access time	$t_{CE}$				100	ns
Output enable access time	$t_{OE}$				30	ns
Output hold time	$t_{OH}$		0			ns
Output disable time	$t_{DF}$		0		25	ns
WORD, /BYTE access time	$t_{WB}$				100	ns

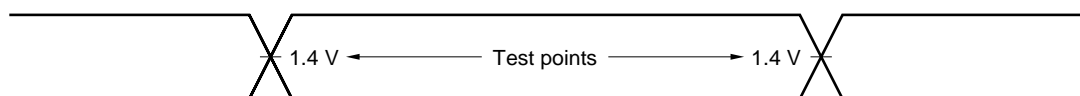
**Remark**  $t_{DF}$  is the time from inactivation of /CE or /OE, OE to high-impedance state output.

**AC Test Conditions**

**Input waveform (Rise / Fall time  $\leq 5\text{ ns}$ )**



**Output waveform**

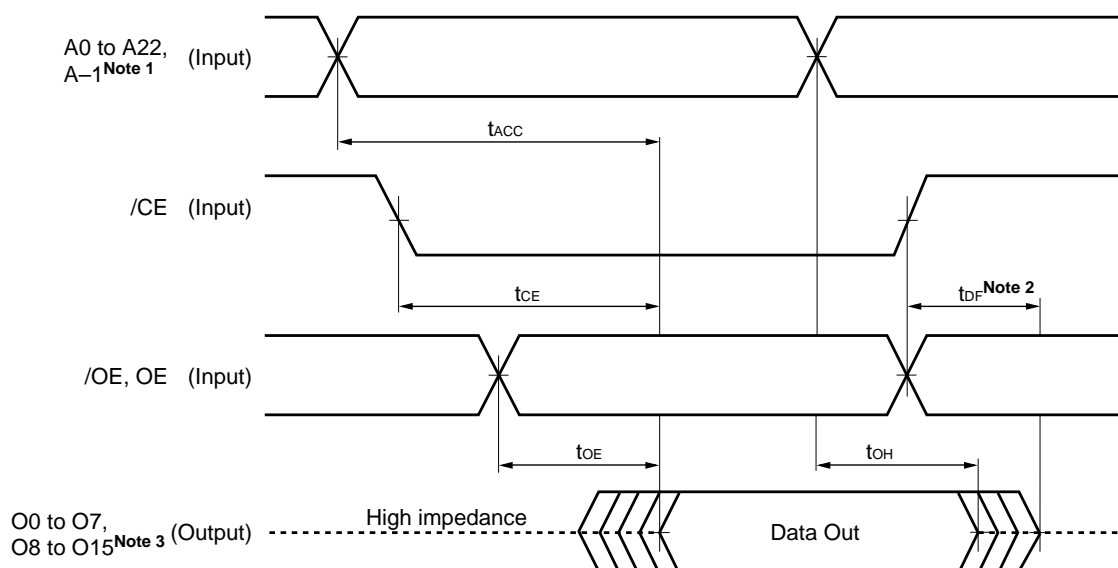


**Output load**

1TTL + 100 pF

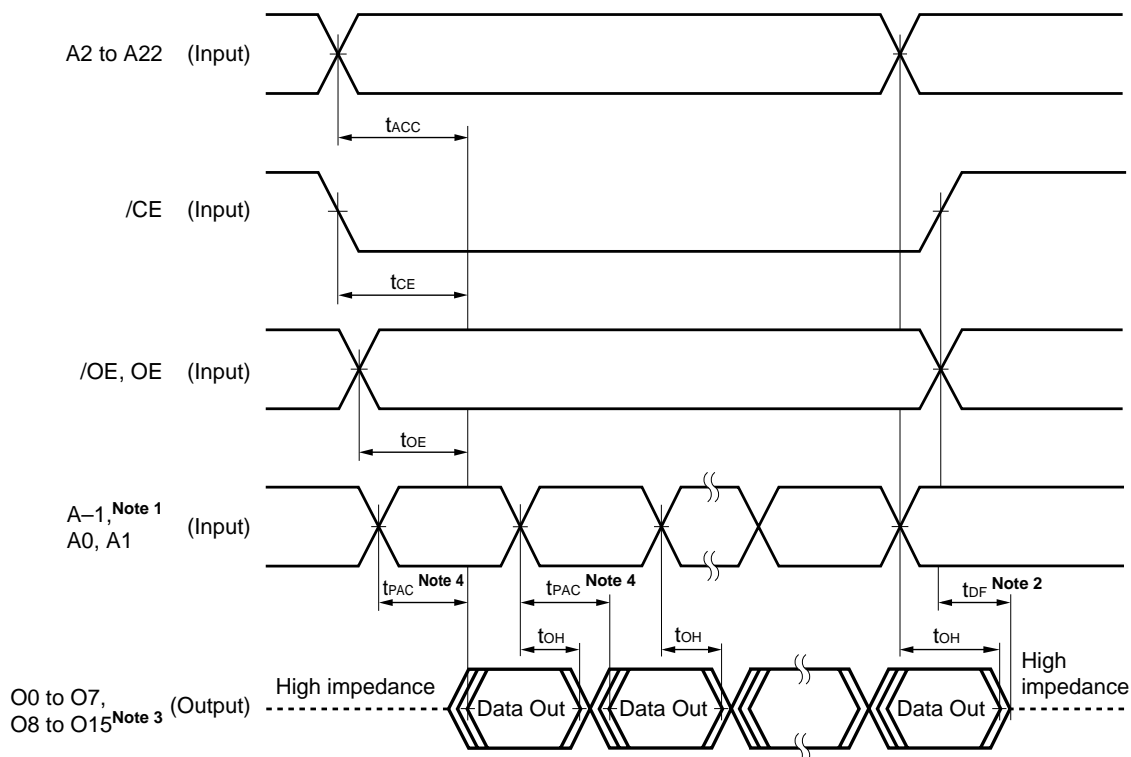


Read Cycle Timing Chart 1



- Notes**
1. During WORD mode, A-1 is O15.
  2.  $t_{DF}$  is specified when one of /CE, /OE, OE is inactivated.
  3. During BYTE mode, O8 to O14 are high impedance and O15 is A-1.

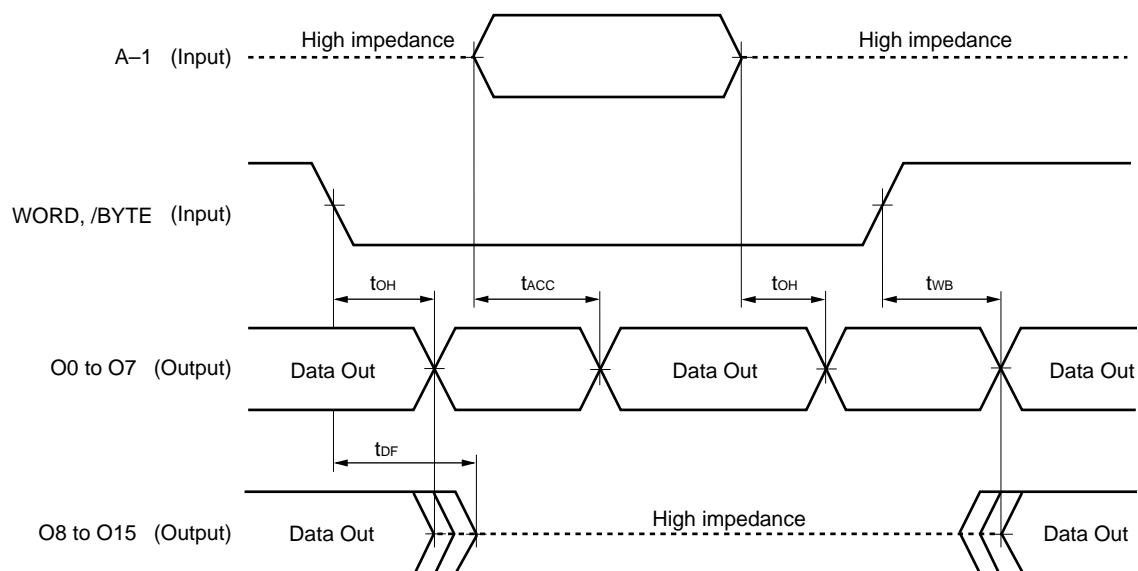
★ Read Cycle Timing Chart 2 (Page Access Mode)



- Notes**
- During WORD mode, A-1 is O15.
  - $t_{DF}$  is specified when one of  $/CE$ ,  $/OE$ , OE is inactivated.
  - During BYTE mode, O8 to O14 are high impedance and O15 is A-1.
  - The definition of page access time is as follows.

Page access time	Upper address (A2 to A22) inputs condition	/CE input condition	/OE, OE input condition
$t_{PAC}$	Before $t_{ACC} - t_{PAC}$	Before $t_{CE} - t_{PAC}$	Before stabilizing of page address (A-1, A0, A1)

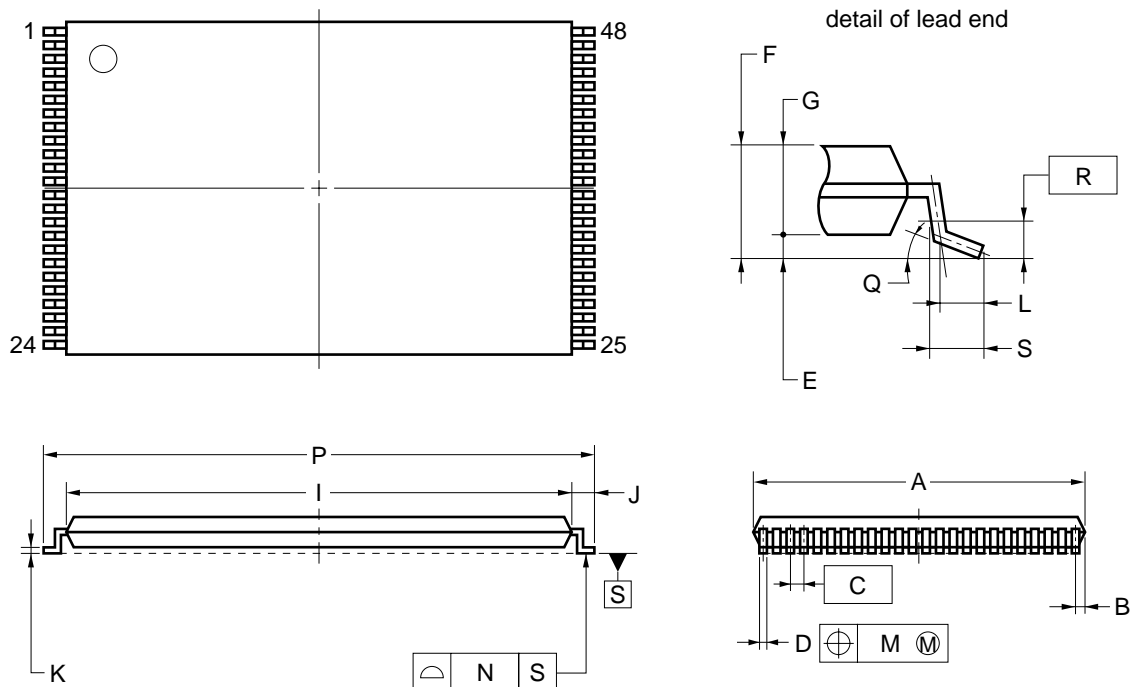
**WORD, /BYTE Switch Timing Chart**



**Remark** /OE, OE and /CE : Active.

★ Package Drawings

48-PIN PLASTIC TSOP(I) (12x18)



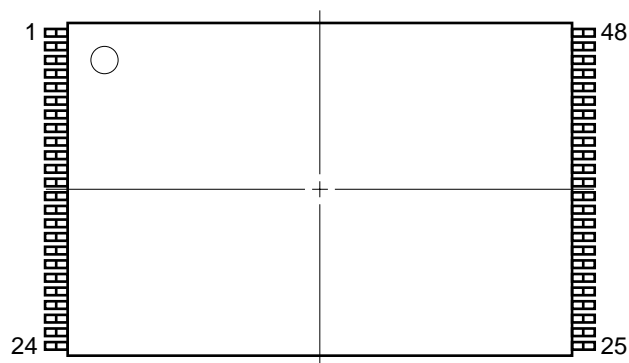
NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX.)

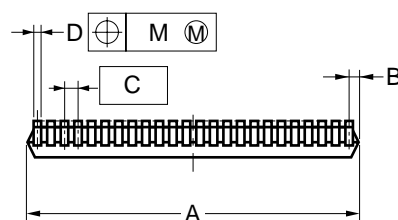
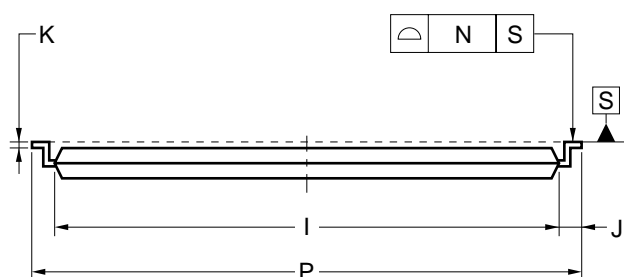
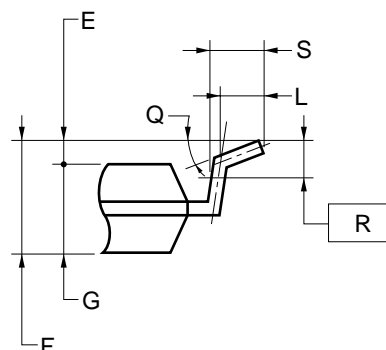
ITEM	MILLIMETERS
A	12.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
I	16.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	18.0±0.2
Q	3°+5° -3°
R	0.25
S	0.60±0.15

S48GY-50-MJH1-1

# 48-PIN PLASTIC TSOP(I) (12x18)



detail of lead end



## NOTES

- Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
- "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX.)

ITEM	MILLIMETERS
A	12.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
I	16.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	18.0±0.2
Q	3°+5° -3°
R	0.25
S	0.60±0.15

S48GY-50-MKH1-1

### Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the  $\mu$ PD23C128040L.

### Types of Surface Mount Device

$\mu$ PD23C128040LGY-MJH : 48-pin plastic TSOP(I) (12 x 18) (Normal bent)

$\mu$ PD23C128040LGY-MKH : 48-pin plastic TSOP(I) (12 x 18) (Reverse bent)

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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