NEC
NEC Electronics Inc.

μPD28C05 512 x 8-BIT CMOS EEPROM

Description

The μPD28C05 is an electrically erasable and programmable read-only memory (EEPROM) organized as 512 words by 8 bits. The device operates from a +5-volt power supply and is fabricated with an advanced CMOS process for high performance and low power consumption.

The device offers an $\overline{\text{ALE}}$ pin to control the latching of addresses and a $\overline{\text{DATA}}$ polling function to indicate the precise end of write cycles. Additional features include chip erase, auto erase and programming. The μPD28C05 is available in standard 24-pin plastic DIP or miniflat packaging.

Features

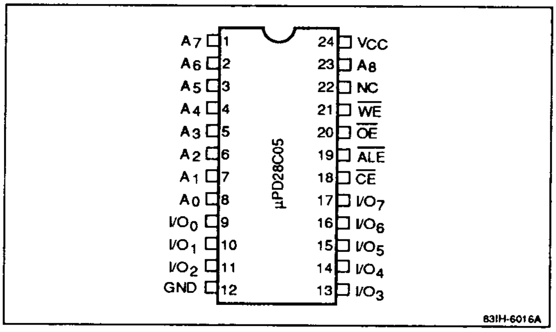
- 512-word by 8-bit organization
- Single +5-volt power supply
- Fast access times of 200 and 250 ns maximum
- Chip erase feature
- Auto erase and programming: 10 ms maximum
- $\overline{\text{DATA}}$ polling feature
- Address latching by means of $\overline{\text{ALE}}$ pin
- Low power dissipation
  - 50 mA max (active)
  - 100 μA max (standby)
- Endurance: 100,000 erase/write cycles per byte
- TTL-compatible inputs and outputs
- Three-state outputs
- Advanced CMOS technology
- 24-pin plastic DIP or miniflat packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD28C05C-20	200 ns	24-pin plastic DIP
C-25	250 ns	
μPD28C05G-20	200 ns	24-pin plastic miniflat
G-25	250 ns	

Pin Configuration

24-Pin Plastic DIP or Miniflat



27b

Pin Identification

Symbol	Function
A_0 - A_8	Address inputs
I/O_0 - I/O_7	Data inputs and outputs
$\overline{\text{CE}}$	Chip enable
$\overline{\text{OE}}$	Output enable
$\overline{\text{WE}}$	Write enable
$\overline{\text{ALE}}$	Address latch enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.6 to +7.0 V
Input voltage, V_{I1}	−0.6 to +7.0 V
Input voltage, V_{I2} ($\overline{OE}$)	−0.6 to +16.5 V
Output voltage, V_{OUT}	−0.6 to +7.0 V
Operating temperature, T_{OPT}	−10 to +85°C
Storage temperature, T_{STG}	−65 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Operating temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_I		12	pF
Output capacitance	C_O		10	pF

Truth Table

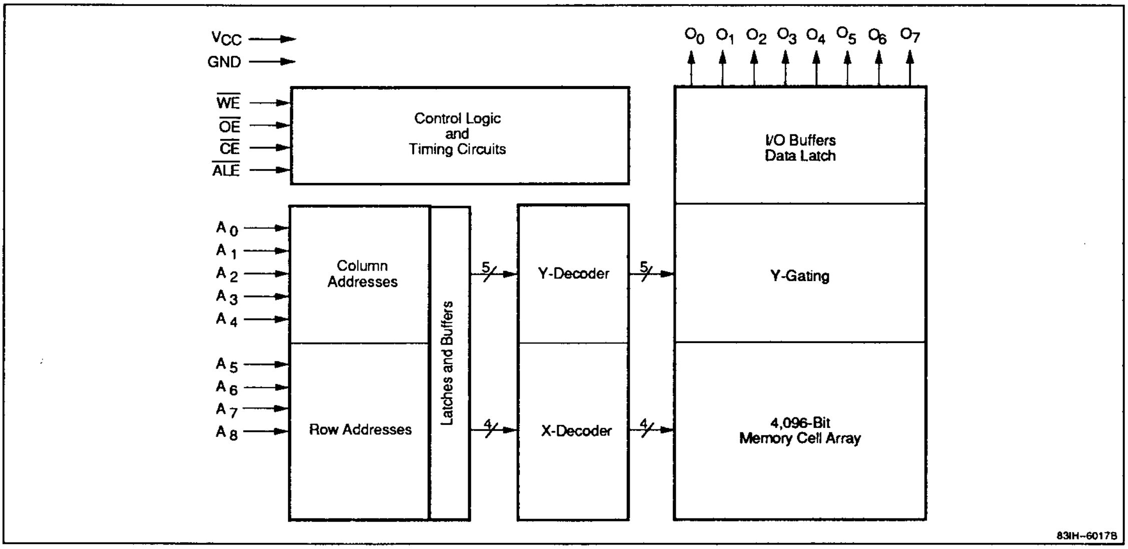
Function	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{ALE}$	I/O	I_{CC}
Read	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}	Active
Standby and write inhibit	V_{IH}	X	X	X	High-Z	Standby
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{IN}	Active
Chip erase	V_{IL}	V_{IHH}	V_{IL}	V_{IH}	D_{IN} = V_{IH}	Active
Write Inhibit	X	V_{IL}	X	X	—	—
	X	X	V_{IH}	X	—	—

Notes:

(1) X can be either V_{IL} or V_{IH}.

(2) V_{IHH} = +15 ±0.5 V.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = −400 µA
	V_{OH2}	V_{CC} − 0.7			V	I_{OH} = −100 µA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output leakage current	I_{LO}			10	µA	V_{OUT} = 0 V to V_{CC} (max)
Input leakage current	I_{LI}			10	µA	V_{IN} = 0 V to V_{CC} (max)
V_{CC} current (active)	I_{CCA1}			20	mA	$\overline{CE}$ = V_{IL}; V_{IN} = V_{IH}
	I_{CCA2}			50	mA	f = 5 MHz; I_{OUT} = 0 mA
V_{CC} current (standby)	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH}
	I_{CCS2}			100	µA	$\overline{CE}$ = V_{CC}; V_{IN} = 0 V to V_{CC}

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

27b

		µPD28C05-20		µPD28C05-25			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Read Cycle							
Address to output delay	t_{ACC}		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; $\overline{ALE}$ = $\overline{WE}$ = V_{IH}
Address hold time from $\overline{ALE}$	t_{AHL}	20		30		ns	$\overline{WE}$ = V_{IH}
$\overline{ALE}$ to output delay	t_{ALE}		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
Address setup time to $\overline{ALE}$	t_{ASL}	15		20		ns	$\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}		200		250	ns	$\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{CE}$ setup time to $\overline{ALE}$	t_{CSL}	20		20		ns	$\overline{WE}$ = V_{IH}
$\overline{CE}$ high to output float	t_{DFC}	0	60	0	80	ns	$\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{OE}$ high to output float	t_{DFO}	0	60	0	80	ns	$\overline{CE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{ALE}$ high-level pulse width	t_{LL}	40		40		ns	$\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	75	10	100	ns	$\overline{CE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
Output hold time from address change	t_{OHA}	0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; $\overline{ALE}$ = $\overline{WE}$ = V_{IH} (Note 2)
Output hold time from rising edge of $\overline{CE}$	t_{OHC}	0		0		ns	$\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH} (Note 2)
Output hold time from rising edge of $\overline{ALE}$	t_{OHL}	0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH} (Note 2)
Output hold time from rising edge of $\overline{OE}$	t_{OHO}	0		0		ns	$\overline{CE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{WE}$ hold time from rising edge of $\overline{OE}$	t_{WHO}	10		10		ns	$\overline{OE}$ = V_{IH}
$\overline{WE}$ setup time to $\overline{CE}$	t_{WSC}	10		10		ns	$\overline{CE}$ = V_{IH}
$\overline{WE}$ setup time to $\overline{OE}$	t_{WSO}	10		10		ns	$\overline{OE}$ = V_{IH}

AC Characteristics (cont)

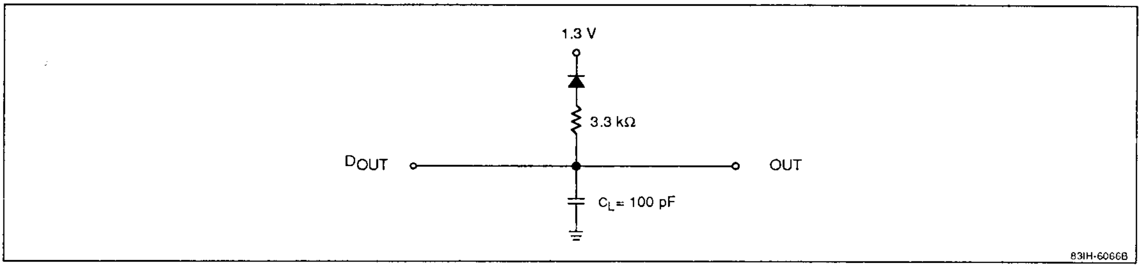
Parameter	Symbol	μPD28C05-20 Min	μPD28C05-20 Max	μPD28C05-25 Min	μPD28C05-25 Max	Unit	Test Conditions
Write Cycle							
Address hold time from $\overline{WE}$	t_{AH}	200		200		ns	
Address setup time to $\overline{WE}$	t_{AS}	10		10		ns	
$\overline{CE}$ high after $\overline{CE}$-controlled write cycle	t_{CEH}	9.9		9.9		ms	
$\overline{CE}$ hold time from $\overline{WE}$ high	t_{CH}	0		0		ns	
$\overline{CE}$ setup time to $\overline{WE}$	t_{CS}	0		0		ns	
$\overline{CE}$ pulse width	t_{CW}	150		150		ns	
Data hold time	t_{DH}	20		20		ns	
Data setup time	t_{DS}	100		100		ns	
$\overline{OE}$ high hold time	t_{OEH}	10		10		ns	
$\overline{OE}$ high setup time	t_{OES}	10		10		ns	
Write cycle time	t_{WC}	10		10		ms	
$\overline{WE}$ high after $\overline{WE}$-controlled write cycle	t_{WEH}	9.9		9.9		ms	
$\overline{WE}$ pulse width	t_{WP}	150		150		ns	
Chip Erase Cycle							
$\overline{CE}$ hold time	t_{ECH}	5		5		μs	
$\overline{CE}$ setup time	t_{ECS}	500		500		ns	
Data hold time	t_{EDH}	100		100		ns	
Data setup time	t_{EDS}	500		500		ns	
$\overline{OE}$ hold time	t_{EOEH}	$t_{ECH} + 3$		$t_{ECH} + 3$		μs	
$\overline{OE}$ setup time	t_{EOES}	500		500		ns	
$\overline{WE}$ pulse width	t_{EWP}	10		10		ms	

Notes:

(1) Input rise and fall time ≤ 20 ns; input pulse levels = 0.45 and 2.4 V; timing measurement reference levels = 0.8 and 2.0 V for both inputs and outputs. See figure 1 for output load.

(2) Output hold time is specified either from the address, or from the $\overline{ALE}$, $\overline{OE}$ or $\overline{CE}$ pins, whichever goes invalid first.

Figure 1. Output Load



Read Cycles

$\overline{CE}$ and $\overline{OE}$ must both be at V_{IL} for read cycles to be executed. If either of these inputs rise to V_{IH} while the device is reading stored data, the outputs will be placed in a state of high impedance. This two-line output control eliminates bus contention in the system application.

Byte Write Cycles

Low logic levels on $\overline{CE}$ and $\overline{WE}$ and high logic levels on $\overline{OE}$ and $\overline{ALE}$ place the μPD28C05 in write operation. The write address inputs are latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs later. The data inputs are latched by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier. Once byte write operation has begun, the internal circuitry assumes all timing control and the byte being addressed in automatically erased and then programmed. The operation completes within the write cycle time (t_{WC}) of 10 ms.

Chip Erase Cycles

All bytes of the μPD28C05 can be erased simultaneously by making $\overline{CE}$ and $\overline{WE}$ fall to V_{IL} and $\overline{ALE}$ rise to V_{IH} after $\overline{OE}$ has been increased to V_{IHH} (+15 ± 0.5 V). The address inputs are "don't care," but the data inputs must all be driven to V_{IH} before the chip erase cycle begins.

$\overline{DATA}$ Polling Feature

This feature supports system software by indicating the precise end of byte write cycles and can be used to reduce the total programming time of the μPD28C05 to a minimum value, which varies with the system environment.

While internal automatic write cycles are being executed, any attempt to read data at the last externally supplied address location will result in inverted data on pin I/O_7. For example, if write data = 1xxx xxxx, then read data = 0xxx xxxx. Once write cycles have finished executing, the execution of a subsequent read cycle will result in true data being output on I/O_7.

Write Protection Features

Three features protect against invalid write cycles:

- Noise immunity, where write operation is inhibited when the $\overline{WE}$ pulse width is 20 ns or less;
- Supply voltage-level detection, where write operation is inhibited when V_{CC} is 2.5 volts or less; and
- Write protection logic, where write operation is inhibited if $\overline{OE}$ is held low or $\overline{CE}$ or $\overline{WE}$ is held high during power-on or off of the V_{CC} supply voltage.

27b

Truth Table

Function	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{ALE}$	I/O_0 - I/O_7	I_{CC}
Read	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}	Active
Standby and write inhibit	V_{IH}	X	X	X	High-Z	Standby
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{IN}	Active
Chip erase	V_{IL}	V_{IHH}	V_{IL}	V_{IH}	$D_{IN} = V_{IH}$	Active
Write inhibit	X	V_{IL}	X	X	—	—
	X	X	V_{IH}	X		

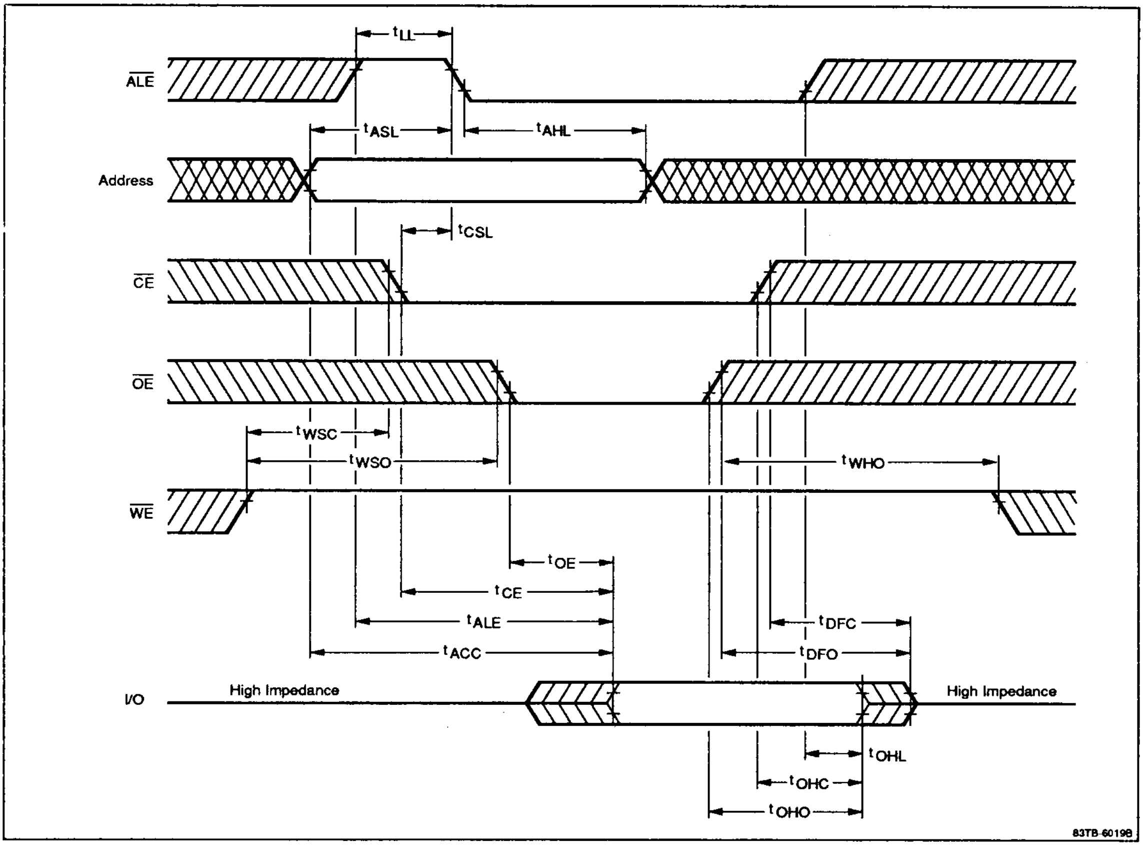
Notes:

(1) X can be either V_{IL} or V_{IH}.

(2) V_{IHH} = +15 ± 0.5 V.

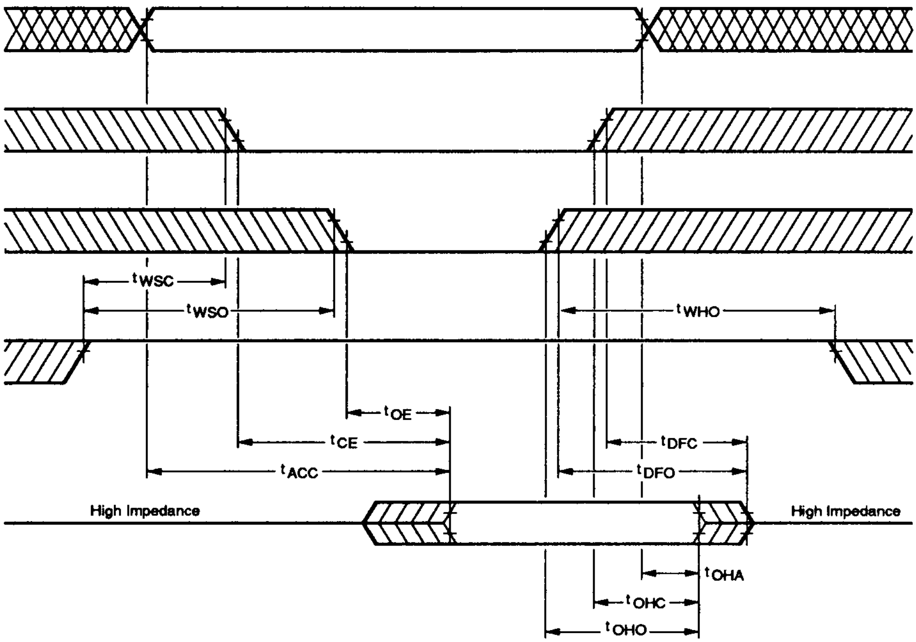
Timing Waveforms

Synchronous Read Cycle ($\overline{ALE}$-Controlled)



Timing Waveforms (cont)

Asynchronous Read Cycle



Note:

[1] $\overline{ALE}$ = V_{IH}.

[2] Use t_{DFC} if $\overline{CE}$ transitions to V_{IH} before $\overline{OE}$ transitions to V_{IH}.

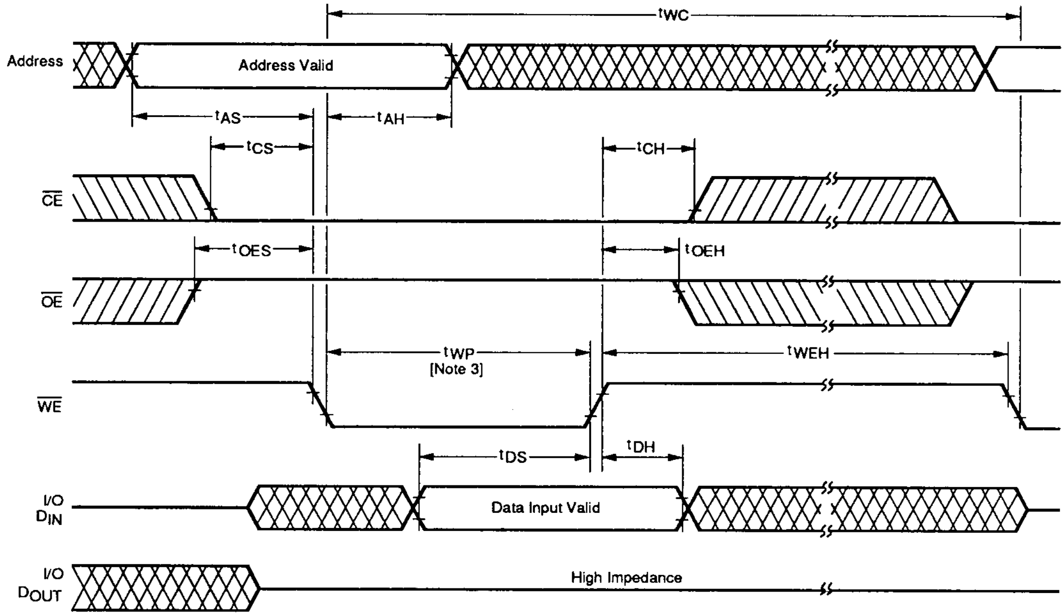
[3] Use t_{DFO} if $\overline{OE}$ transitions to V_{IH} before $\overline{CE}$ transitions to V_{IH}.

83TB-6020B

27b

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

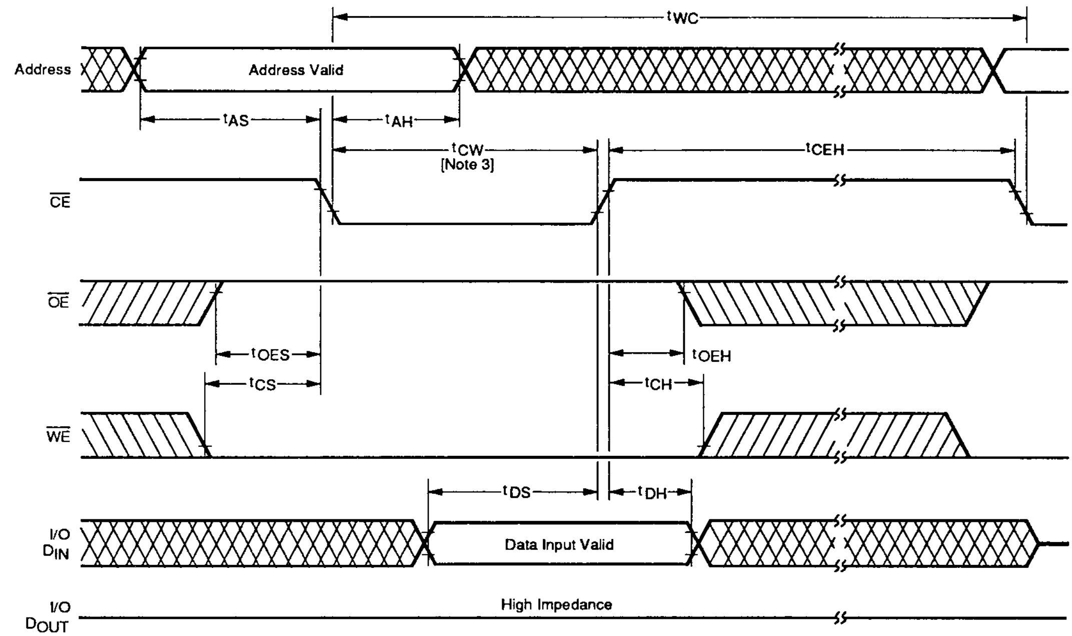
[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameter t_{WP} is defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

83IH-6223B

Timing Waveforms (cont)

$\overline{CE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameter t_{CW} is defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

83IH-6224B

27b

Timing Waveforms (cont)

Chip Erase Cycle