

DATA SHEET

NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT μ PD35H73

2 048-BIT CCD LINEAR IMAGE SENSOR

The μ PD35H73 is a 2048-bit linear image sensor consisting of charge coupled devices (CCDs), which converts light to voltage. This product is made up of a 2048-bit photosensor array, charge transfer register with a pair of 1024-bit CCDs, and sample and hold circuit. The photosensor has a 14 μ m pitch.

FEATURES

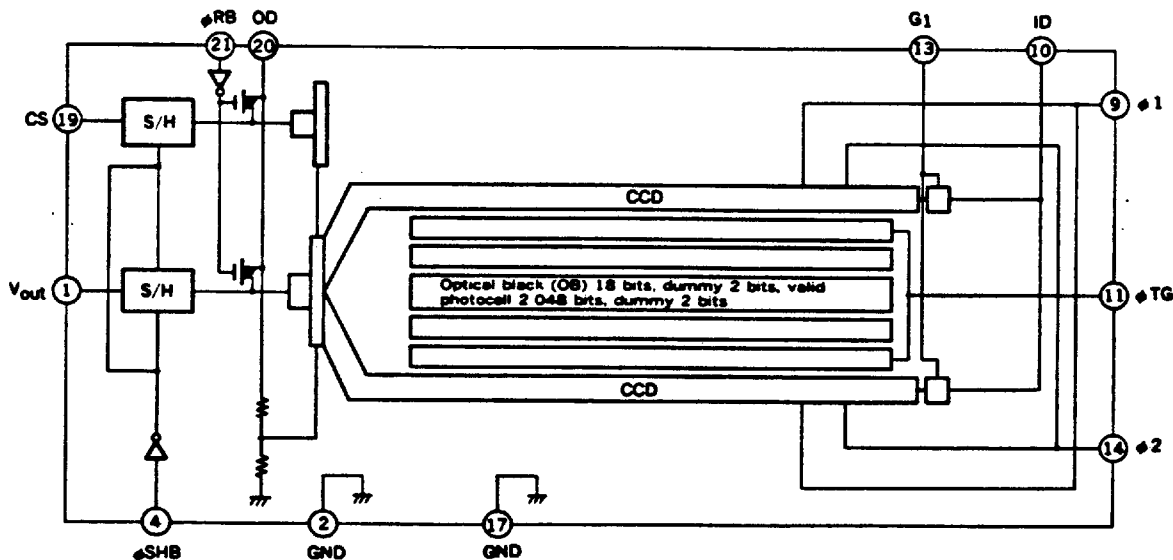
- Incorporates a sample and hold circuit.
- High response sensitivity: Providing a response two times better than the existing equivalent NEC product (μ PD3573D) to the light from a white fluorescent lamp
- Peak response wavelength: 550 nm green
- Reads the shorter side of a B4-size sheet at a resolution of 8 dot/mm
- Driven by a 12 V single power supply
- All signal clock input: drive by CMOS 5 V

ORDERING INFORMATION

Part Number	Package	Quality Grade
μ PD35H73D	22-pin ceramic DIP (CERDIP) (400 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

BLOCK DIAGRAM



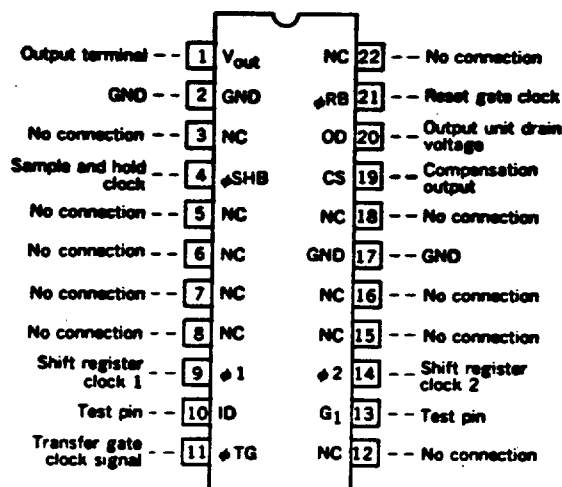
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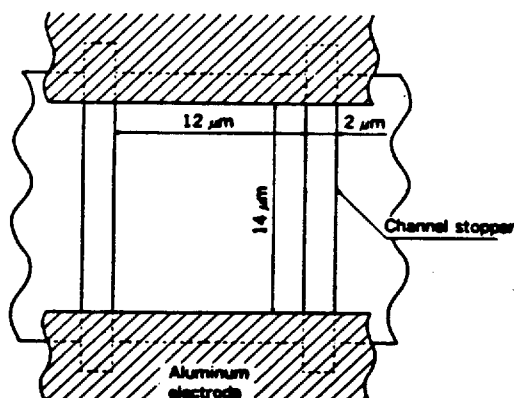
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PIN CONNECTION DIAGRAM (Top View)



PHOTOELEMENT STRUCTURE DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Output unit drain voltage	V _{OD}	-0.3 to +15	V
Test pin ID voltage	V _{ID}	-0.3 to +15	V
Shift register clock signal voltage	V _{φ1}	-0.3 to +15	V
	V _{φ2}	-0.3 to +15	V
Reset signal voltage	V _{φRB}	-0.3 to +15	V
Transfer gate signal voltage	V _{φTG}	-0.3 to +15	V
Sample and hold signal voltage	V _{φSHB}	-0.3 to +15	V
Operating ambient temperature	T _{opt}	-25 to +60	°C
Storage temperature	T _{stg}	-40 to +100	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -25$ to $+60$ °C)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Output unit drain voltage	V_{OD}	11.4	12.0	12.6	V
Test pin G_1 voltage	G_1		0		V
Test pin ID voltage	V_{ID}	11.4	12.0	12.6	V
Shift register clock 1 signal high level	$V_{\phi 1H}$	4.5 ($V_{OD}-3$)	5.0 (V_{OD})	5.5 ($V_{OD}+0.5$)	V
Shift register clock 1 signal low level	$V_{\phi 1L}$	-0.3 (-0.3)	0 (0)	0.5 (0.5)	V
Shift register clock 2 signal high level	$V_{\phi 2H}$	4.5 ($V_{OD}-3$)	5.0 (V_{OD})	5.5 ($V_{OD}+0.5$)	V
Shift register clock 2 signal low level	$V_{\phi 2L}$	-0.3 (-0.3)	0 (0)	0.5 (0.5)	V
Reset signal RBH high level	$V_{\phi RBH}$	4.5	5.0	5.5	V
Reset signal RBL low level	$V_{\phi RBL}$	-0.3	0	0.5	V
Transfer gate signal high level	$V_{\phi TGH}$	4.5 ($V_{OD}-3$)	$V_{\phi 1H}$	$V_{\phi 1H}$	V
Transfer gate signal low level	$V_{\phi TGL}$	-0.3 (-0.3)	0 (0)	0.5 (0.5)	V
Sample and hold signal high level	$V_{\phi SHBH}$	4.5	5.0	5.5	V
Sample and hold signal low level	$V_{\phi SHBL}$	-0.3	0	0.5	V
Data rate	$f_{\phi R}$	0.2	1	10	MHz

Remark: () is the case of input signal clock 12 V.

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ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$, $V_{OD} = 12.0\text{ V}$, $f_{\phi 1} = 0.5\text{ MHz}$, data rate = 1 MHz, storage time = 10 ms,
light source: 3 200 K Halogen-lamp + C500 (Cut-filter of infrared light),
Input signal clock = 5 V_{p-p})

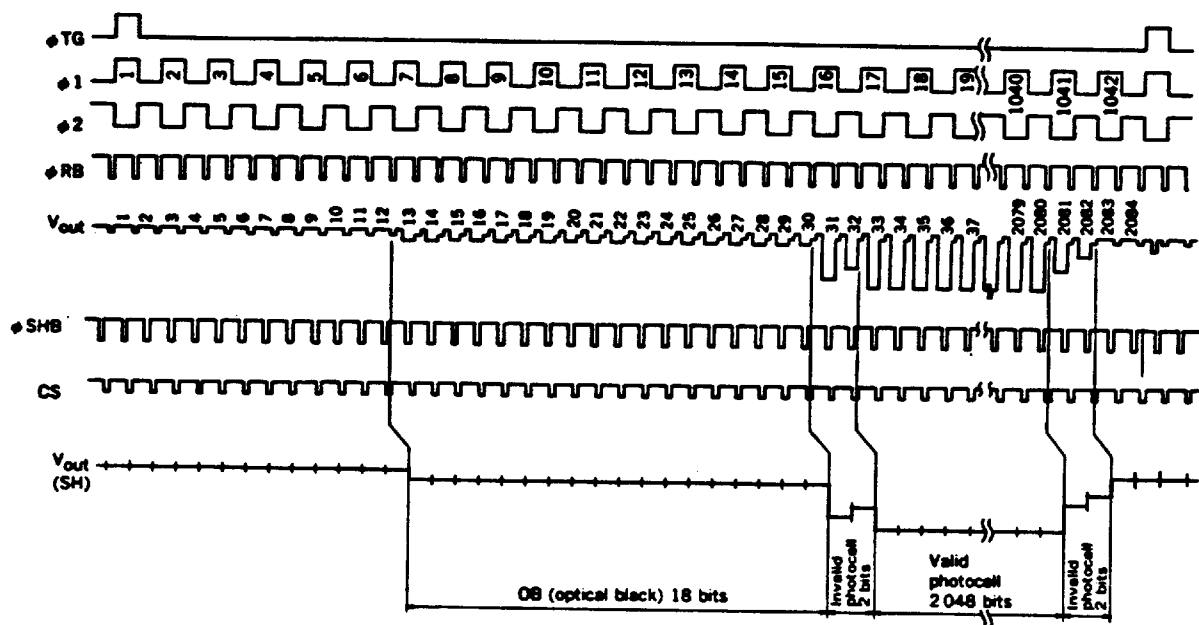
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Saturation voltage	V_{sat}	1.5	2.0		V	
Saturation exposure	SE		0.16		LXS	white fluorescent lamp
Photo response non-uniformity	PRNU		± 2	± 8	%	$V_{out} = 500\text{ mV}$
Average dark signal	ADS		0.1	5	mV	light shielding
Dark signal non-uniformity	DSNU	-5	0.5	+5	mV	light shielding
Power consumption	P_W		80	150	mW	
Output impedance	Z_O		0.5	1	k Ω	
Response	R_F	8.4	12.0	15.6	V/LXS	white fluorescent lamp
	R_W		48.0			W lamp
Response peak wavelength			550		nm	
Image lag	IL		2	5	%	$V_{out} = 500\text{ mV}$
Offset level	V_{OS}	5.0	7.0	9.0	V	
Input capacity of shift register clock pin	$C_{\phi 1}$		500		pF	
	$C_{\phi 2}$		350			
Reset pin input capacity	$C_{\phi RB}$		5		pF	
Input capacity of sample and hold pin	$C_{\phi SHB}$		5		pF	
Input capacity of transfer gate signal pin	$C_{\phi TG}$		100		pF	
Output rise delay time	t_d		20		ns	
Register in-balance	RI			3	%	$V_{out} = 500\text{ mV}$
Transfer efficiency	TTE	92			%	$V_{out} = 500\text{ mV}$ $f_{\phi R} = 10\text{ MHz}$
Dynamic range	DR		4000		times	$V_{sat}/DSNU$
Reset field-through noise	RFSN	-300	-100	200	mV	
Sample hold noise	SHSN	20	50	100	mV	
AC-voltage of compensation output	V_{CSOF}	5.0	7.0	9.0	V	
AC-voltage of off-set level to compensation output	$ V_{OS}-V_{CSOF} $			300	mV	

Remark:

RFSN is changed by V_{OD} . The change ratio: $\frac{\Delta RFSN}{\Delta V_{OD}} = \frac{90\text{ mV}}{0.8\text{ V}}$

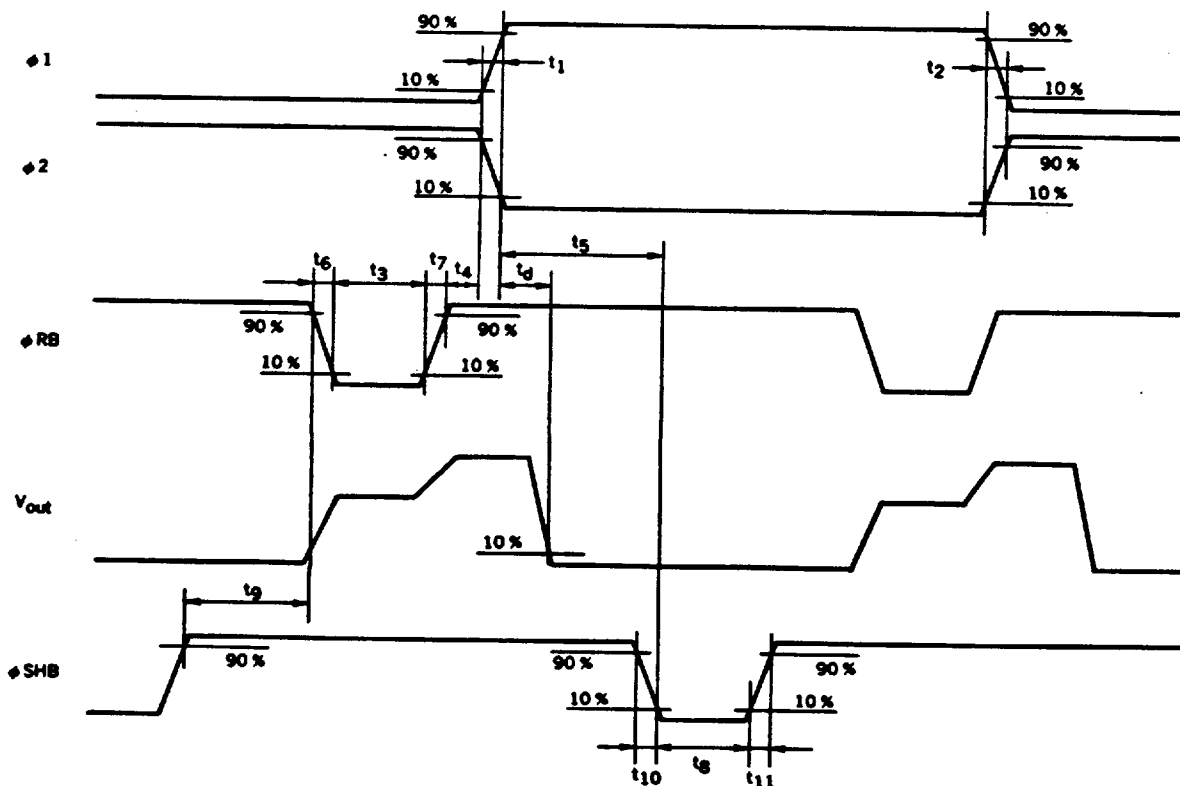
Therefore within recommended operating condition ($V_{OD} = 12\text{ V} \pm 0.8\text{ V}$), RFSN's dispersion has -390 mV to +290 mV.

TIMING CHART



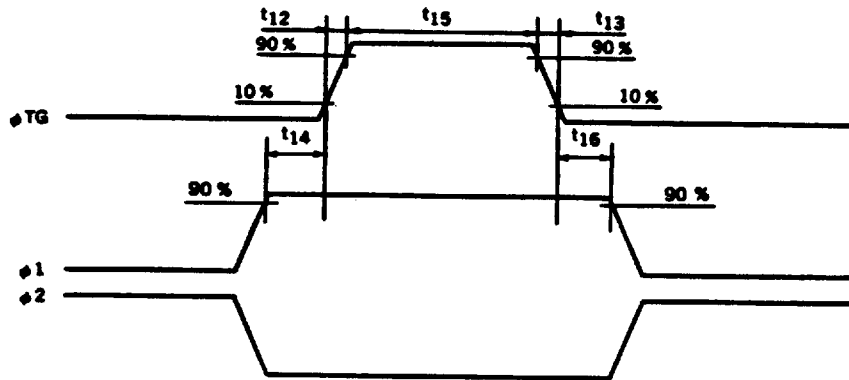
Remark: V_{out} = Output unused ϕSHB (Please input same of the signal clock ϕTG to ϕSHB)
 $V_{out}(SH)$ = Output used ϕSHB

Timing chart for $\phi 1$, $\phi 2$, ϕR , ϕSH , and V_{out}

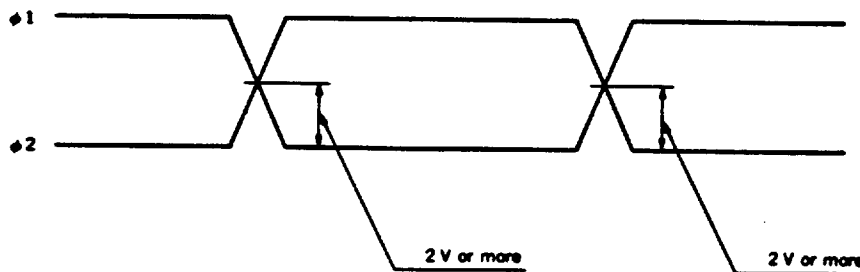


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Timing chart for φTG, φ1, φ2



Cross points φ1, φ2



Remark: Please adjust input-resistance of terminal φ1 and φ2 about cross-point between φ1 to φ2.

ITEM	MIN.	TYP.	MAX.
t1, t2	0	50	150
t3	20	100	(500)
t4	20	100	(500)
t5	30	300	(500)
t6, t7	0	50	50
t8	20	150	(500)
t9	20	100	(50)
t10, t11	0	50	100
t12, t13	0	50	100
t14, t16	0	100	(500)
t15	500	1000	(5000)

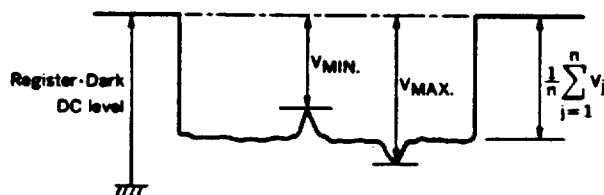
(ns)

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage: V_{sat}
The point at which the response linearity is lost.
2. Saturation exposure: SE
Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs
3. Photo response non-uniformity: PRNU
Expressed by the following expressing with the peak/bottom ratio to the average output voltage of all the valid bits.

$$PRNU(\%) = \left(\frac{V_{MAX. \text{ or } V_{MIN.}}}{\frac{1}{n} \sum_{j=1}^n V_j} - 1 \right) \times 100$$

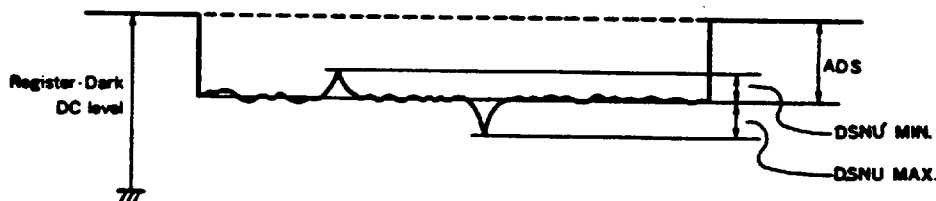
n : Number of valid bits
 V_j : Output voltage of each bit



4. Average dark signal: ADS
Output average voltage in light shielding

$$ADS(mV) = \frac{1}{n} \sum_{j=1}^n V_j$$

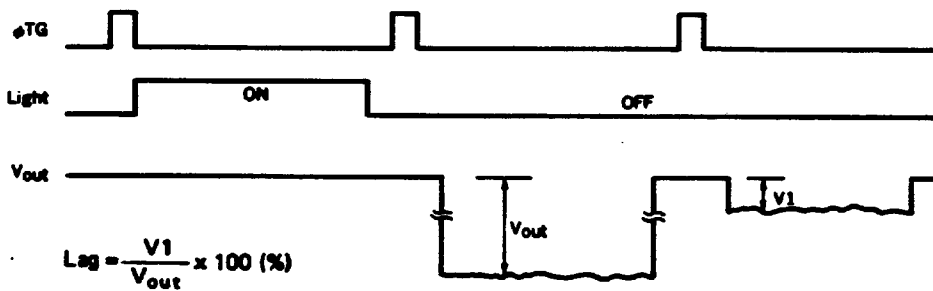
5. Dark signal non-uniformity: DSNU
The difference between peak or bottom output voltage in light shielding and ADS.



6. Output impedance: Z_o
Output pin impedance when viewed externally
7. Response: R
Output voltage divided by exposure (lx-s).
Note that the response varies with the light source.

8. Image Lag: IL

The rate between the last output voltage and the next one after read out the data of one line.

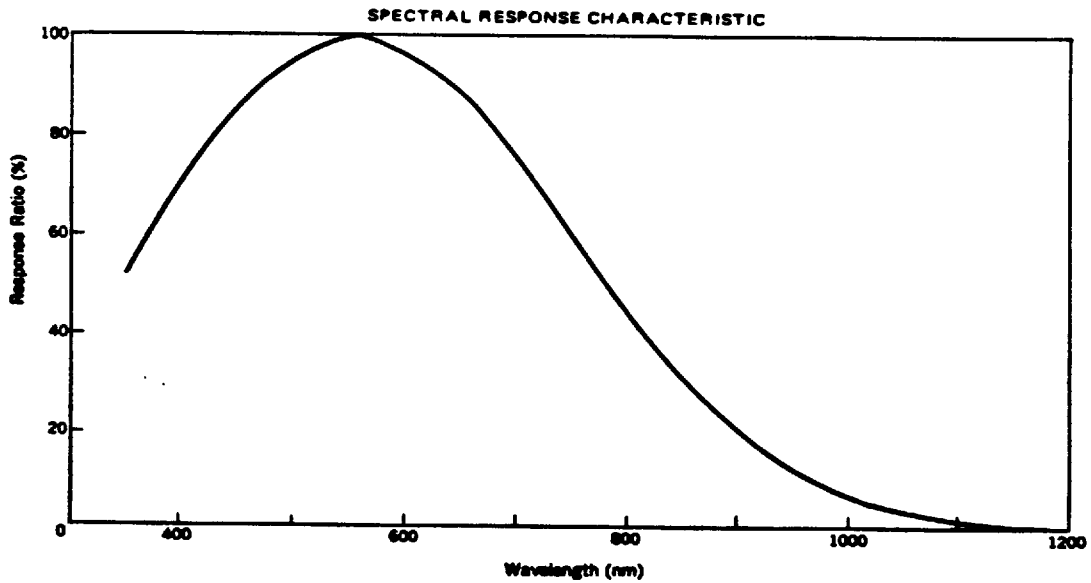
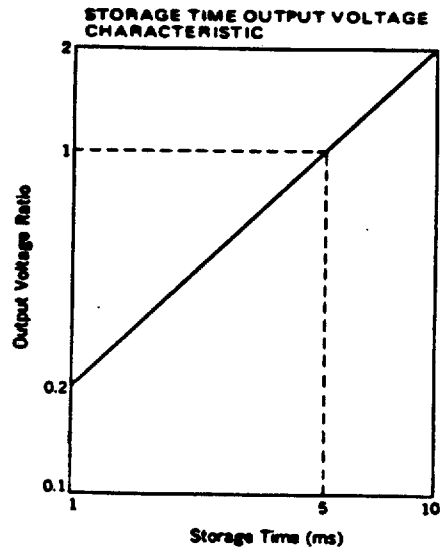
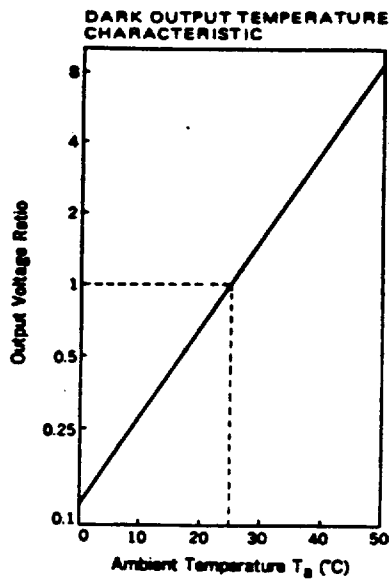


9. Register Imbalance: RI

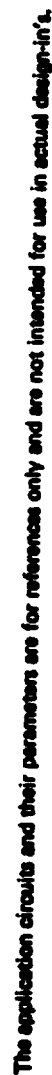
The rate between the average output voltage which is the difference between the output voltage from Odd and Even bits, and the average output voltage of all the valid bits.

$$RI = \frac{\frac{1}{n} \sum_{j=1}^n |V_j - V_{j+1}|}{\frac{1}{n} \sum_{j=1}^n V_j} \times 100 (\%)$$

STANDARD CHARACTERISTIC CURVES ($T_a = 25^\circ\text{C}$)

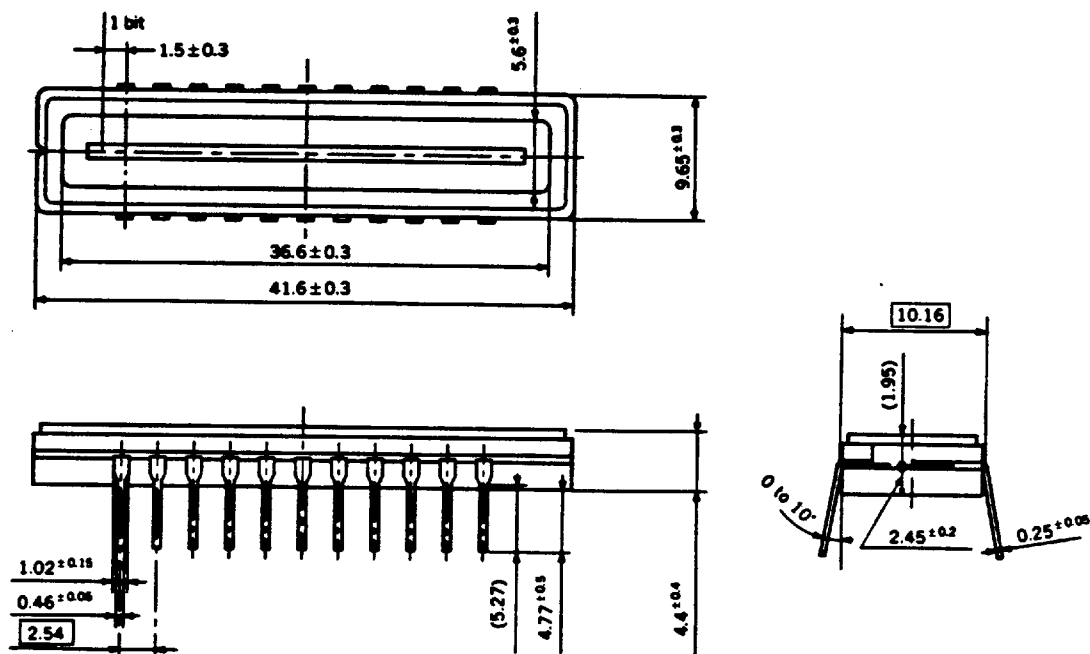


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PACKAGE DIMENSIONS (Unit: mm)



Name	Dimensions	Refractive index
Glass cap	$39.5 \times 9.0 \times 0.7$	1.5